

Feasibility Study and DSP Considerations for 400G/lane PAM4 Co-Packaged Optics

802.3 400GPL Study Group

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400G optical signaling architectures

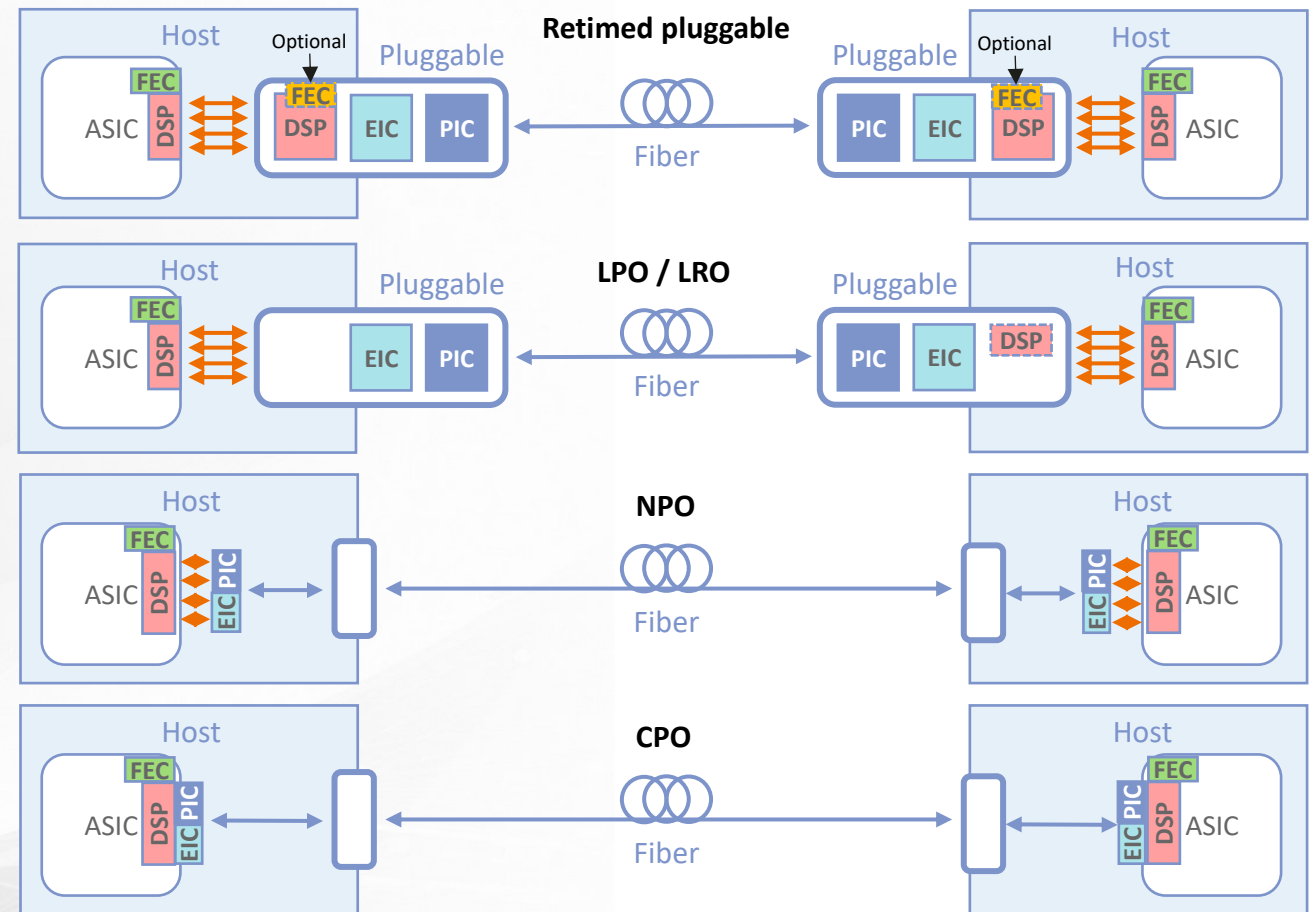
Retimed & linear drive needs to be supported by PAM4

Optical modulation

- PAM4 is the preferred choice due to higher SNR, MPI tolerance and lower error floor
- Industry-first 400G PAM4 DSP presented at OFC 2026 for retimed applications
- KP4 FEC is the desired path forward

Architectures

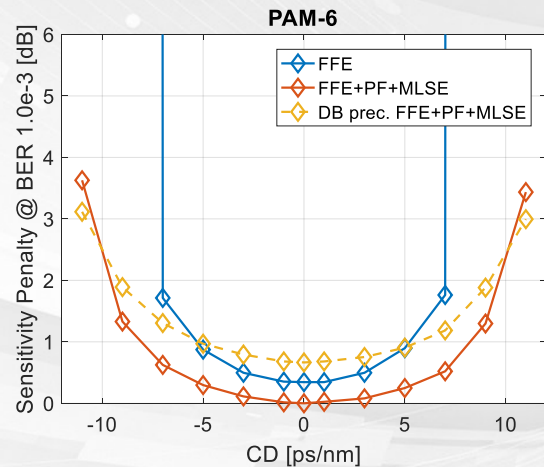
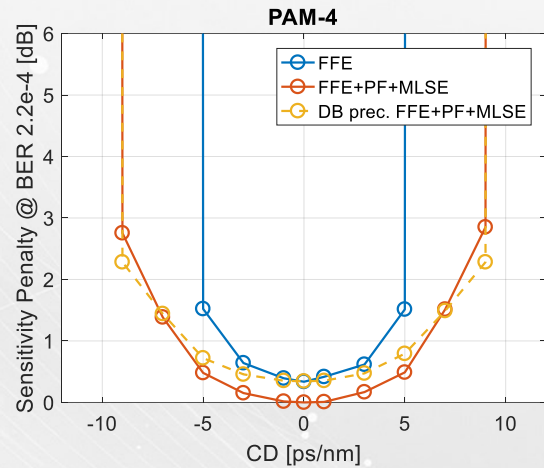
- E2E PAM4 signaling required for linear drive architectures
- Technical feasibility of CPO and E/O/E channels using advanced analog and digital equalization techniques is of interest



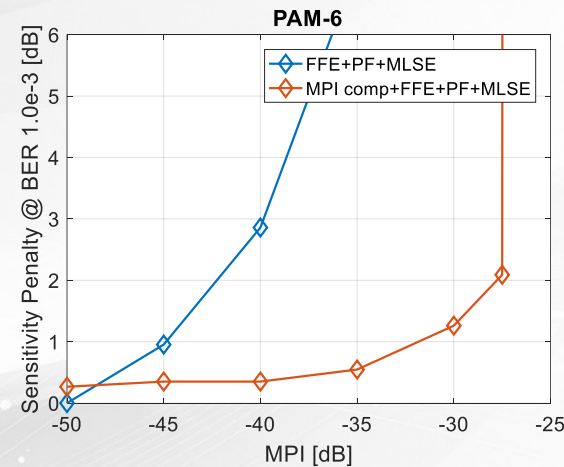
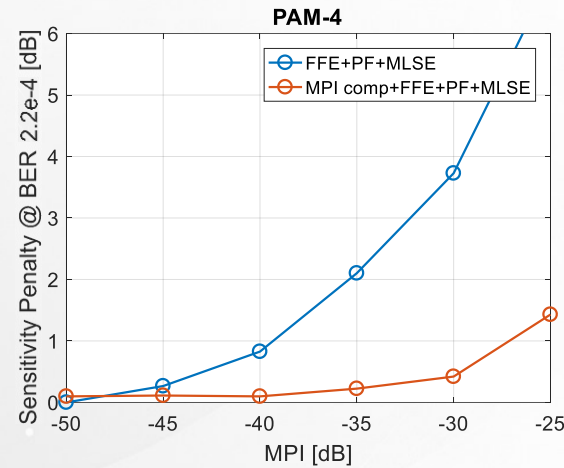
400G PAM4 vs. PAM6

Does the electrical channel advantage of PAM6 translate to the optical domain?

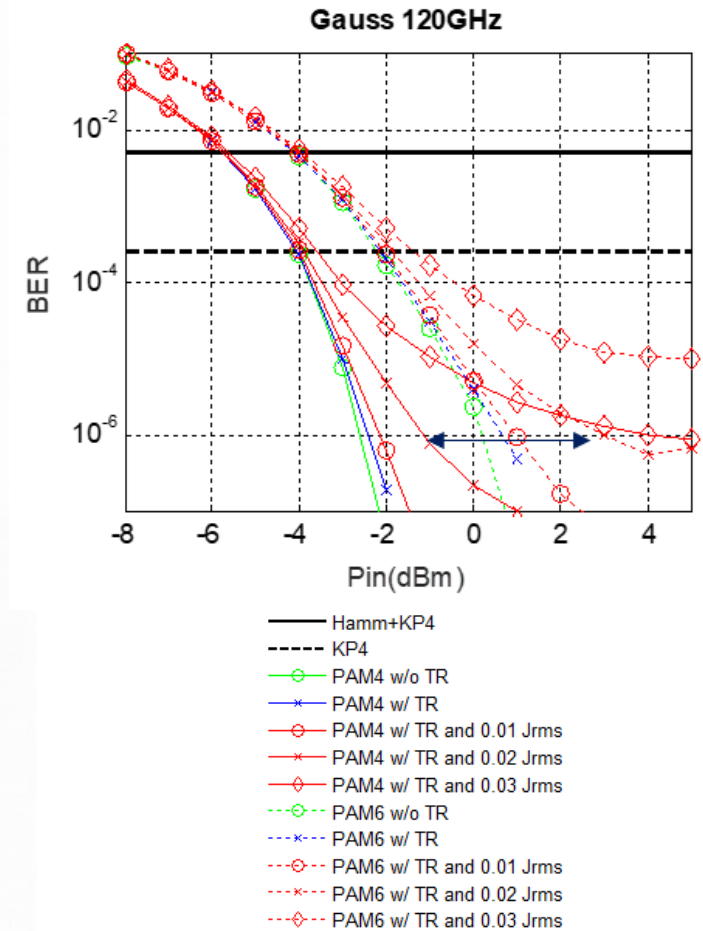
CD – both only support LWDM



MPI – Higher tolerance to link flaps for PAM4

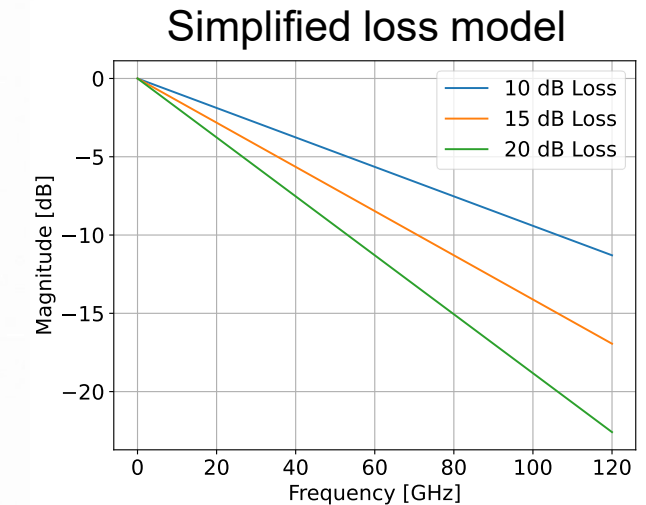
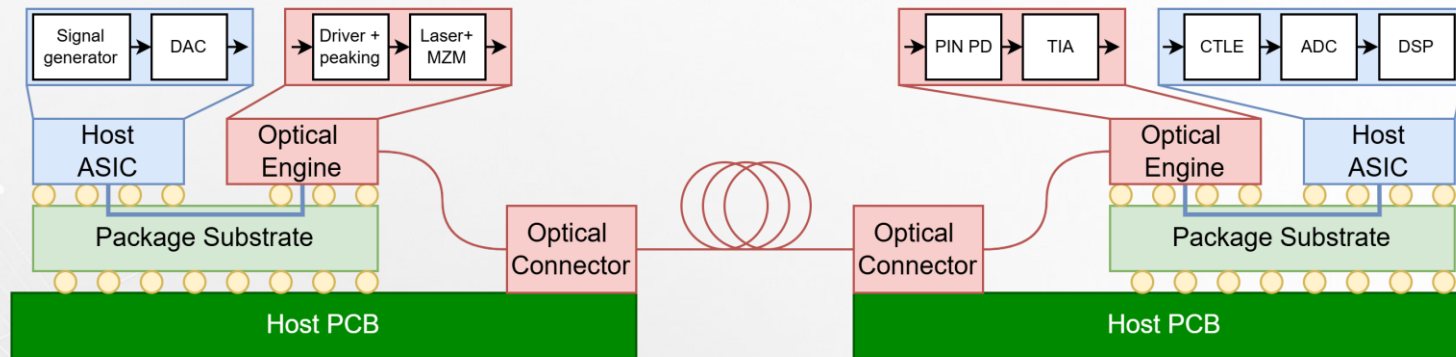


Clock jitter tolerance – PAM6 with higher error floor



Overview

400G CPO/NPO simulation system

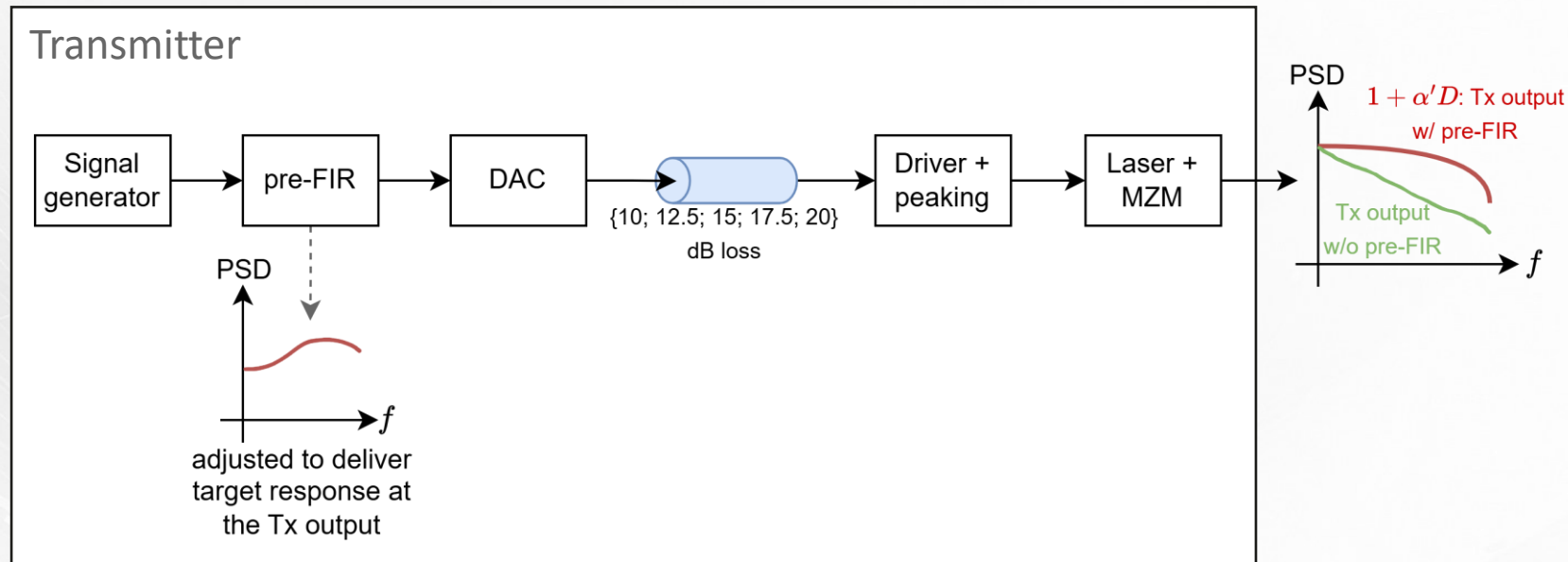


- 400 Gb/s/lane CPO/NPO feasibility for next-gen optical systems
 - Key parameters currently remain open.
 - Minimizing PCB trace insertion loss (Host ASIC ↔ Optical Engine) is critical for feasibility.
- Scope of investigation
 - Feasibility dependence on Tx digital and analog equalization techniques.
 - Interaction with Rx DSP

Component	Key parameters in simulation
Tx DSP	pre-FIR 7 taps
DAC	1 sps, ENOB 5.0
Tx PCB	10 – 20 dB link loss @ Nyquist
Driver Peaking	{0; 5; 10} dB
Laser	-152 dB/Hz RIN, 10 MHz linewidth
Tx Bandwidth	110 GHz 4th order Bessel
Fiber	<500 m; no CD, DGD, MPI
PD + TIA	Responsivity 0.5 A/W, 25 pA/√Hz noise
Rx PCB	10 – 20 dB link loss @ Nyquist
Rx CTLE	10 dB
ADC	1 sps, ENOB 6.0
Rx Bandwidth	110 GHz 4th order Bessel
Rx DSP	FFE 41 taps, optional 2 tap noise whitening filter + memory 1 MLSE

Tx Pre-FIR Calibration

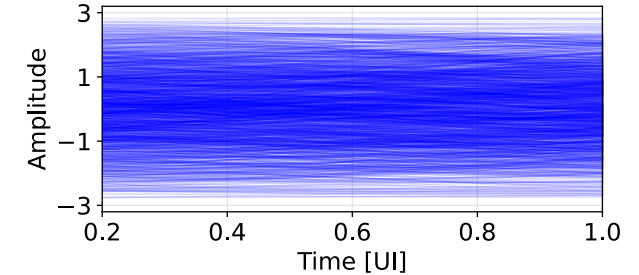
Controlling the tradeoff between emphasis and PAPR



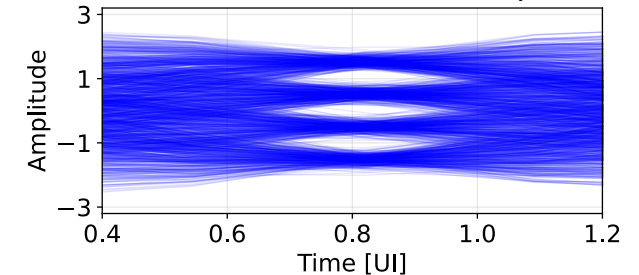
- Pre-FIR optimization: Target is a partial response (PR) of the type $1 + \alpha'D$ at the output of the transmitter.
 - Degree of freedom for optimization
 - $\alpha' = 0$: inversion of the Tx electrical link (including driver peaking)
 - $\alpha' > 0$: Intentional residual ISI allocated to Rx DSP. Reduces pre-FIR emphasis, lowering DAC quantization noise.

MZM input eye diagrams

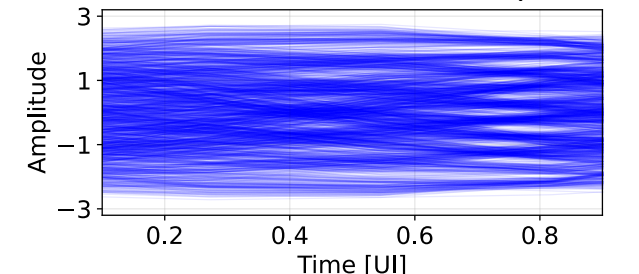
15 dB el. link loss, w/o pre-FIR



15 dB el. link loss, $\alpha' = 0.0$ pre-FIR

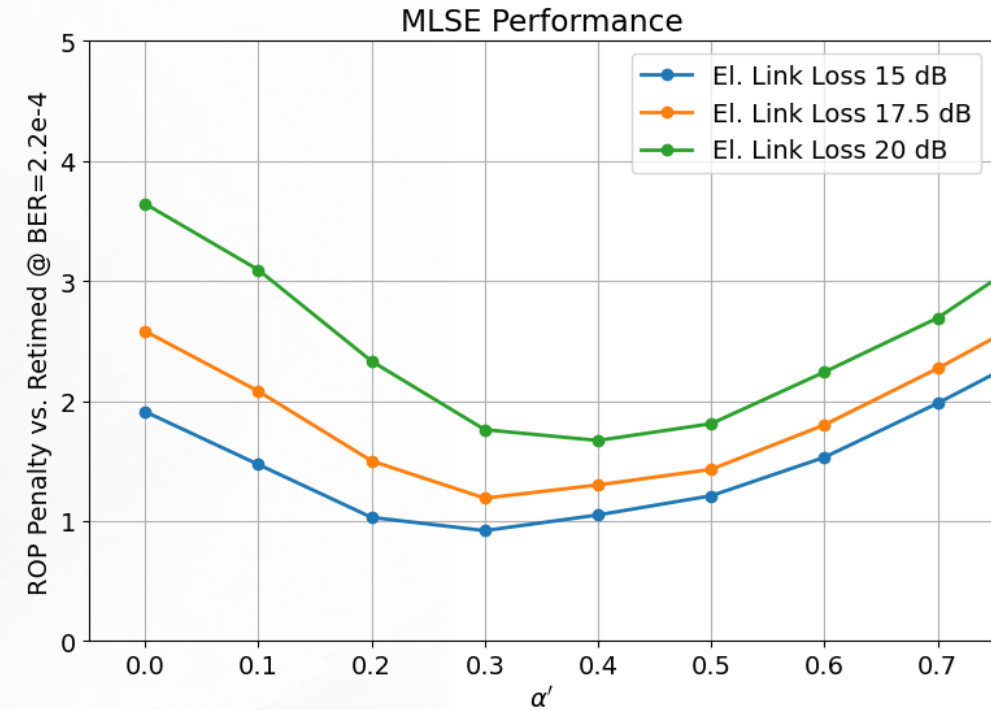
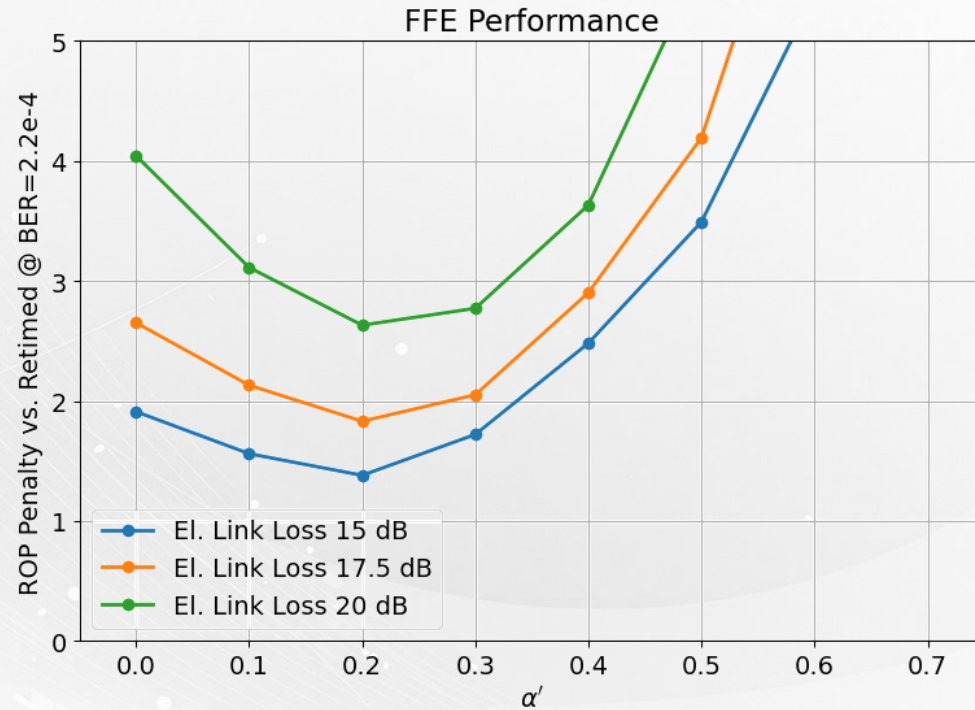


15 dB el. link loss, $\alpha' = 0.4$ pre-FIR



Tx Pre-FIR Sweep Curves w/ 5 dB Tx Driver Peaking

Optimization depends on Rx DSP



- Rx DSP performance after full CPO system (parameters in page 4): Comparison of FFE and MLSE
 - ROP penalty vs. pre-FIR parameter α' dependent on the electrical link loss.
- Pre-FIR requirements: Optimization varies by Rx DSP type.
 - FFE performance is optimal at $\alpha' = 0.2$ for various electrical links losses.
 - MLSE performance is optimal at $\alpha' = 0.3$ and $\alpha' = 0.4$.

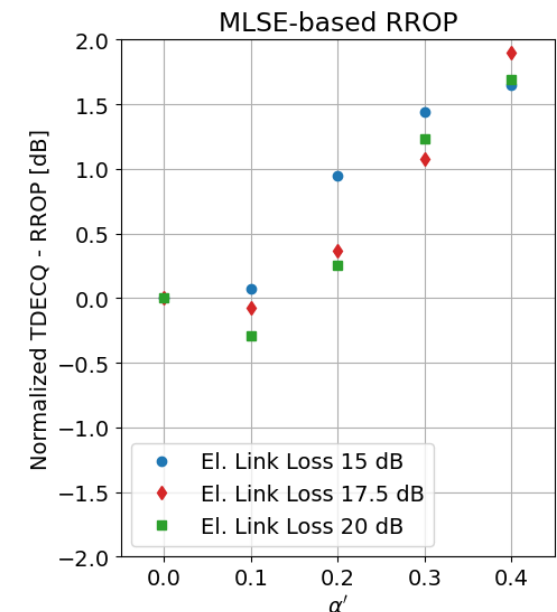
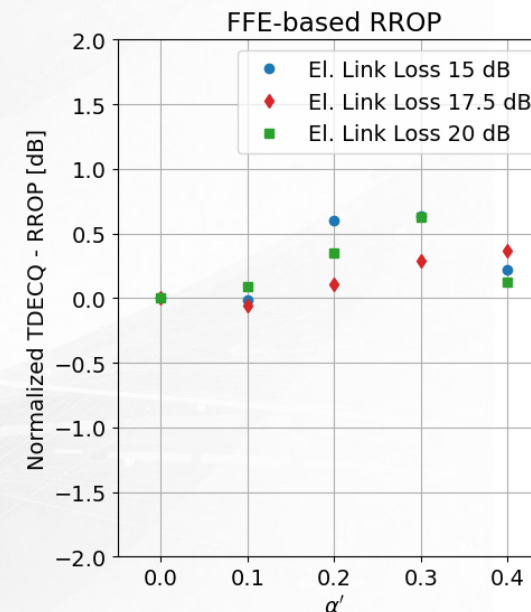
TDECQ Analysis w/ 5 dB Tx Driver Peaking

Conflict with MLSE performance optimization

Metric validity and optimization conflict

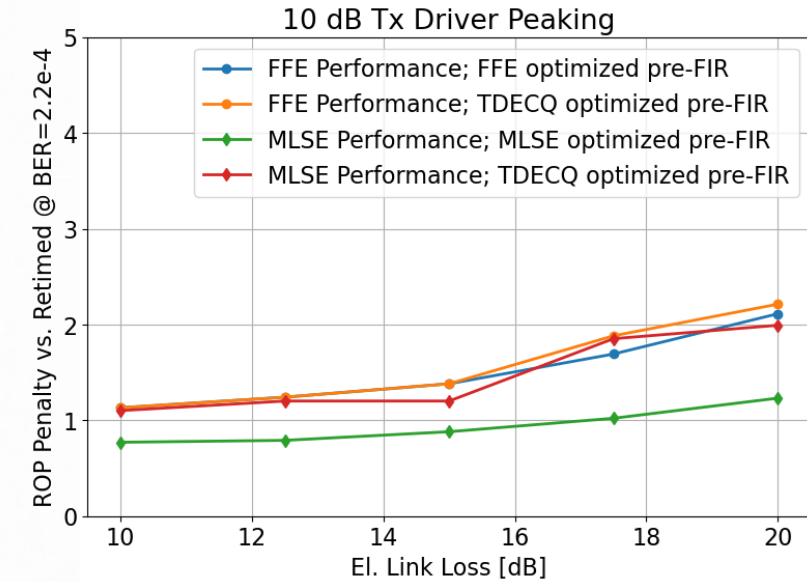
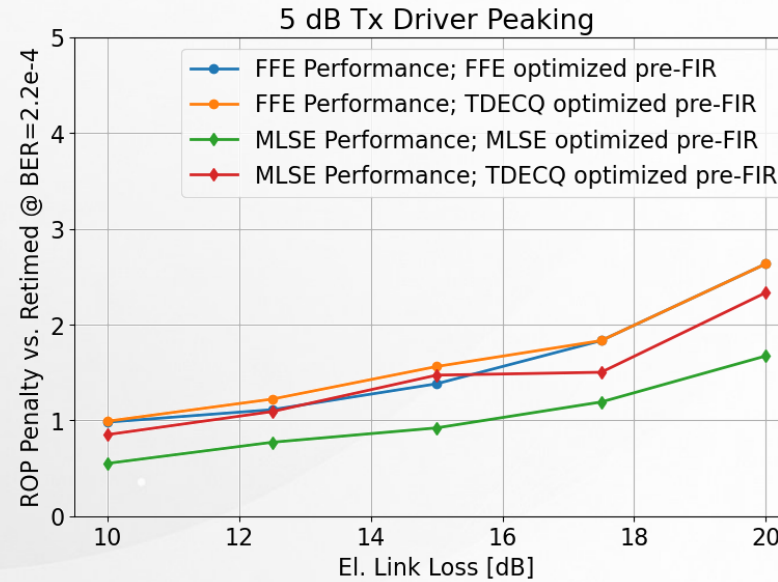
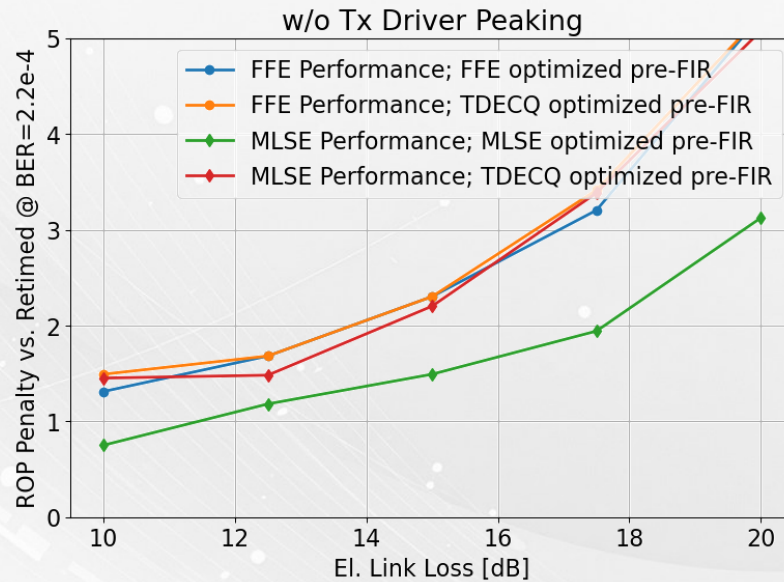
- As a transmitter quality metric, TDECQ should correlate with final link performance.
 - Inherent problem for linear drive systems: reference receiver is different from linear receiver.
 - Increased difference if MLSE is used in the receiver: Optimizing for TDECQ yields pre-FIR coefficients differing from those optimal for MLSE performance.
- A conflict exists between minimizing TDECQ and optimizing for specific Rx DSP configurations.

Optimization metric	Best α' @ 20 dB el. link loss
TDECQ	0.2
FFE Performance	0.2
MLSE Performance	0.4



Tx Pre-FIR and Analog Peaking Overview

Optimization metric is critical for the final performance



- With MLSE employed in the Rx DSP, TDECQ fails to accurately predict system performance.
 - An alternative transmitter quality metric is necessary.
 - An example would be MLSE TDECQ, proposed in https://www.ieee802.org/3/dj/public/23_07/stojanovic_3dj_01_2307.pdf
- Tx analog peaking is critical to minimize penalties in high-insertion-loss electrical links.

Conclusions

Digital and analog equalization require careful co-optimization

Feasibility

- 400 Gb/s/lane CPO/NPO feasibility depends on electrical link loss, analog peaking and Rx DSP.
 - For electrical link losses > 15 dB, strong Tx analog peaking and Rx MLSE are mandatory.

DSP Interaction

- Optimal pre-FIR configuration is strictly dependent on the Rx DSP (FFE vs. MLSE).

Metric Limitations

- Standard TDECQ is a poor predictor of link performance when Rx MLSE is used.
- An alternative metric (e.g., MLSE TDECQ) is required for accurate transmitter evaluation for E/O/E channels

The background is a dark blue, almost black, space filled with glowing blue lines and dots. These lines form a complex, circuit-like pattern that flows from the bottom left towards the top right. Some lines are straight, while others are jagged, resembling a stylized representation of a circuit board or data pathways. Small, bright blue dots are scattered along these lines, some appearing as single points and others as small clusters. The overall effect is one of high-tech, digital connectivity.

Thank you