Chip to Module and Optics Objectives

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Background

- **Current 400 GPL objectives are to support 400 Gb/s, 800 Gb/s, and 1.6 Tb/s PMDs/PHYs**
  - Support optional single-lane 400 Gb/s, 800 Gb/s, and 1.6Tb/s Gb/s attachment unit interfaces for chip-to-module and chip-to-chip applications
  - Define a physical layer specification that supports 400 Gb/s, 800 Gb/s, and 1.6Tb/s Gb/s operation over 1 pair of SMF with lengths up to at least 500 m
  - Define a single-lane, 400 Gb/s, 800 Gb/s, and 1.6Tb/s Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter
- **During 1st 400 GPL study group several contributions suggested that the project should define**
  - NPO and CPO implementations
  - Linear and RTLR (Retimed Transmit Linear Receive) AUI/optics
- **This contribution explore possible expanded objectives that 802.3 and what to avoid!**

Electrical Interfaces Defined in 802.3 and Their Logics

- **802.3ae 10 GbE Standard published in 2002**
  - Didn't define 10G AUI (retimed) interface
  - Instead of defined XSBI (16x wide) and XAUI (4x wide)
  - XFP MSA SNIA INF-8077i started in 2002 and published in 2004 defined 10G AUI interface – 6 years to get to 10G retimed AUI
  - SFF-8431 started in 2006 and published 2009 defined 10G PPI interface (non-retimed limiting) – 11 years to get to 10G PPI
- **802.3ba 40 GbE/100 GbE standard published in 2010**
  - Annex 86A borrowed SFF-8431 PPI for XLPPI and CPPI
- **802.3bm 40 GbE/100 GbE published 2014**
  - Annex 86E defines 4x25G AUI (retimed)

Took 4 more years to develop 25G AUI

- **802.3bs 200 GbE/400 GbE published 2017**
  - Annex 120E defines 4x50G/8x50G AUI (retimed) – 50G PAM4 AUI leveraged 25G AUI
- **802.3CK 100/200 GbE/400 GbE published 2022**
  - Annex 120G defines 100G/2x100G/4x100G AUI (retimed)

Took 5 more years to develop 100G AUI

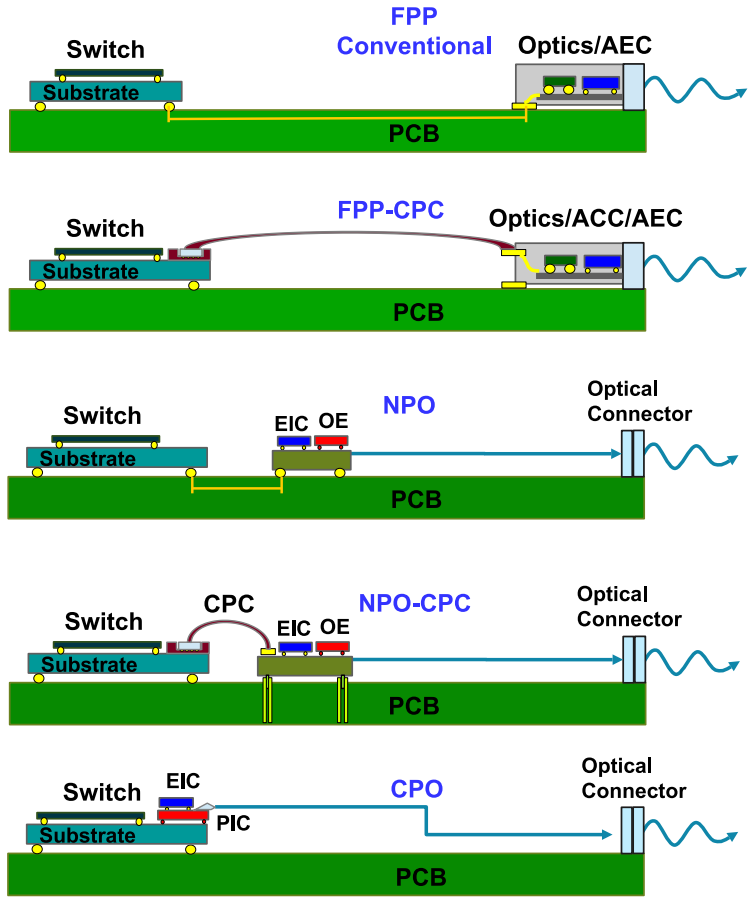
- **802.3dj 200GbE/400 GbE/800 GbE/1.6 TbE expected to be published by Q1-2027**
  - Annex 176D defines 200G/2x200G/4x200G/8x200G AUI (retimed) – DJ is the 1st project that defined both 200G PAM4 optical and electrical/AUI!

Linear and RTLR Specifications defined Outside IEEE

- **OIF 112G-Linear started in 2021 and published in 2025 – 7 years after 802.3bs 100G single λ**
  - Supports C2M loss up to 13 dB (vs 16 dB for IEEE AUI)
  - Compatible with IEEE TP2/TP3 optical specifications
- **LPO MSA 100G-DR specifications published 2025 – 7 years after 802.3bs 100G single λ**
  - Support C2M loss of 16 dB (same as IEEE AUI)
  - LPO MSA defines its own optical specifications and not compatible with IEEE PMDs
- **OIF 112G-RTLR started in 2024 and was published in 2025 – 7 years after 802.3bs 100G single λ**
  - Supports C2M loss up to 16 dB ball-ball (same as IEEE AUI)
  - Compatible with IEEE TP2/TP3 optical specifications
- **OIF 224G-Linear started in 2024 about 4 years after "Beyond 400 Gb/s Ethernet" CFI - ongoing effort**
  - Compatible with IEEE TP2/TP3 optical specifications
- **OIF 224G-RTLR started in 2024 "Beyond 400 Gb/s Ethernet" CFI - ongoing effort**
  - Compatible with IEEE TP2/TP3 optical specifications
- **What is and what isn't common in all the above interfaces**
  - All interfaces use the IEEE 802.3 CR specifications to close the optical and electrical link budget
  - All interfaces have a level of optimization/engineering to make the interface work for the target application
  - Generally, to make the interface work for Linear and RTLR the C2M loss has been reduced and some of the AUI channel parameters have been tighten!

IEEE 802.3dv Path to 400GPL Optics and Copper

- **IEEE 803.3 should focus on C2M interface that supports 400GPL optics and copper with necessary modulation and FEC**
  - FPP Conventional at 400G C2M full retime with PAM6/PAM8 likely will only support AEC – conventional FPP will result in higher power interfaces due to package and PCB!
  - FPP-CPC at 400G C2M Full Retime with PAM4/PAM6 Support both AEC/ACC and passive cable – IEEE 400GPL-C2M contribution will be foundational to the whole industry!
  - Conventional NPO (OBO) at 400G C2M Full Retime with PAM6/PAM8 – due to package and PCB limitation doesn't offer a real value unless these limitations are solved!
  - NPO-CPC and variant of this implementation "XSR+" with interposer support PAM4 with lower loss and simpler equalizer – IEEE 400GPL-C2N (chip to near optics) retimed interface may also have value but this can also be defined in OIF
  - CPO at 400G is interesting long term but unlikely to be near-term solution given SiPho modulator BW coupled with CPO manufacturing challenges!



Why Avoid Definition CPO in the TF

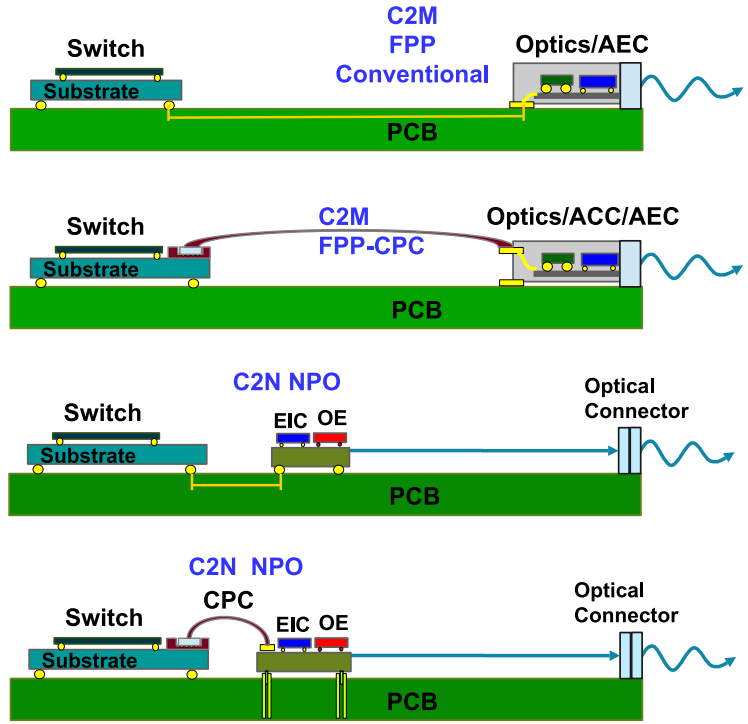
- **Major suppliers are building CPO system vertically – but TP2/TP3 of these products are compliant to the IEEE specifications**
  - Broadcom CPO, see https://www.youtube.com/watch?v=IxGQpfg8U5U
  - Nvidia CPO, see https://www.youtube.com/watch?v=kS8r7UcexJU
- **CPO may have variety of electrical interfaces such use slow-wide based on UCIe, RTLR, or Linear**
  - Even though CPO electrical interface maybe different, generally CPO implementations adhere to the IEEE TP2/TP3 specifications for interoperability
- **CPO electrical interface and driver require significant customization specially based on evolving devices**
  - TFLN have been demonstrated to have the necessary 90+ GHz BW – but not available in standard SiPhotonics process
  - Standard SiPhotoncis MRM and MZM are in development
    - MRM to support 400GPL BW would have to be significantly de-tuned
    - MZM would require power hungry distributed amplifier or segmented drivers
  - SiGe EAM devices can be integrated into SiPhotoncis process
  - InP EAM and MZM offer the BW and power efficiently but not scalable for CPO implantation
- **There is no broad market to define a common CPO implementation in IEEE given the vertical integration by major suppliers**
  - Evolving devices require significant analog customization
  - Some CPO implementations may use D2D interfaces such UCIe.

What 400GPL may want to define in addition to C2M in IEEE?

- **C2N Chip to near package optics is a retimed interface along the line of OIF 112G-XSR+ but does include one socket**
  - At 400G expect to see broad C2N adoption due to SI challenges and PD with conventional pluggable module!

Modulation Parameters	C2N	C2M	C2M
Modulation	PAM4	PAM4	PAM6
Baudrate	212.5 GBd	212.5 GBd	~178 GBd*
Loss @ Nyquist	20 dB	36 dB	32 dB
Pre-FEC BER	$1x10^{-5}$	$1x10^{-5}$	$\sim 1x10^{-4}$
FEC	FEC RS(514, 544)	FEC RS(514, 544)	FEC RS(514, 544)+FECi
Distance	100 mm Substrate/CPC	200 mm PCB 400 mm Cable	250 mm PCB 500 mm Cable
Interconnect	Substrate + 1 socket	PCB/Cable + 1 connector	PCB/Cable + 1 connector

* Actual line rate may vary few % depending on the FECi inner code.



FPP – Front Panel Pluggable
NPO - Near package optics

Comparisons of C2N with C2M PM4/PAM6

- **C2N expect to offer ~40% lower PD than C2M PAM4 – 400G C2M PAM4 equalizer is more like 200G-KR!**

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Loss @ Nyquist	20 dB	36 dB	32 dB
Pre-FEC BER	$1x10^{-5}$	$1x10^{-5}$	$\sim 1x10^{-4}$
FEC	FEC RS(514, 544)	FEC RS(514, 544)	FEC RS(514, 544)+FECi
Transmitter Parameters			
Jitter and rise time	Scaled from 802.3dj	Scaled from 802.3dj	Scaled from 802.3dj
SNR_{TX}	33.5 dB	33.5 dB	37 dB
TX FFE	3pre/2post	3pre/2post	3pre/2post
RLM	95%	95%	97%
Receiver Parameters			
Receiver	5 pre-cursors, 2x4 bank of floating, with Nmax=56, and 1T DFE	6 pre-cursors, 2x4 bank of floating, with Nmax=107, and 1T DFE	6 pre-cursors, 2x4 bank of floating, with Nmax=107, and 1T DFE
Eta0	$7.5x10^{-9}$ V^2/GHz	$5.0x10^{-9}$ V^2/GHz	$5.0x10^{-9}$ V^2/GHz
ENOB	5.5 bits	6.0 bits	6.5 bits
MLSD	Off	On	On

* Actual line rate may vary few % depending on the FECi inner code.

How to Best Address Linear and RTLR Applications

- **To define Linear and RTLR applications, 1st IEEE 802.3dv needs to define optical specifications, modulation, FEC/BER, channel requirements, and electrical specifications for C2M (C2N?)**
- **OIF PLL has already published 112G-Linear specifications, currently working on 224G-Linear, and expect to define 448G-Linear for C2M(C2N)**
  - 448G-Linear channel may have to be significantly better than C2M or C2N to be able to close the optical and electrical links using IEEE 400GPL-CR SerDes
- **OIF PLL has already published 112G-RTLR specifications, currently working on 224G-RTLR, and RTLR authors believe 448G-RTLR could be defined by leveraging 400GPL C2M(C2N) specifications**
  - OIF 224G-RTLR authors believe that 448G-RTLR Egress channel could be identical to C2M(C2N) but ingress channel may have to be better than C2M(C2N) to close the optical and electrical links using IEEE 400GPL-CR SerDes
- **The authors think the OIF structure is better suited to define 448G-Linear and 448G-RTLR specifications**
  - After availability of 802.3dv D1.x draft, OIF 224G-RTLR authors will have the visibility to determine feasibility of 448G-RTLR based on C2M or C2N or based on an improved sub-set.

Summary

- **IEEE 802.3dv TF focus should be:**
  - Define modulation, FEC, and electrical specifications for C2M(possibly C2N), C2C, CR, and KR
  - Define modulation, FEC, and Optical TP2/TP3 specifications for DR PMDs
- **There is merits to define both PAM4 and PAM6 C2M interfaces considering evolving interconnect technology**
  - PAM6 can be early enabler of C2M pluggable applications
  - C2N should only be defined based on PAM4 modulation
- **IEEE should avoid defining CPO considering vertical eco-system, evolving device implementations, and fragmented market**
  - IEEE greatest contribution to the CPO market is to define robust optical TP2/TP3 PMDs specifications
- **IEEE should also avoid defining 400G Linear and 400G RTLR as these implementation likely would require further improvement in the C2M(C2N) channels and may only operate over a sub-set of channels**
  - Trying to define Linear and RTLR links will slow down the IEEE development and likely will result in compromised Optical PMD and CR specifications – resulting in less reach and higher power PMDs!

Thank You!