Modulation and FEC scheme for 400G/lane CR

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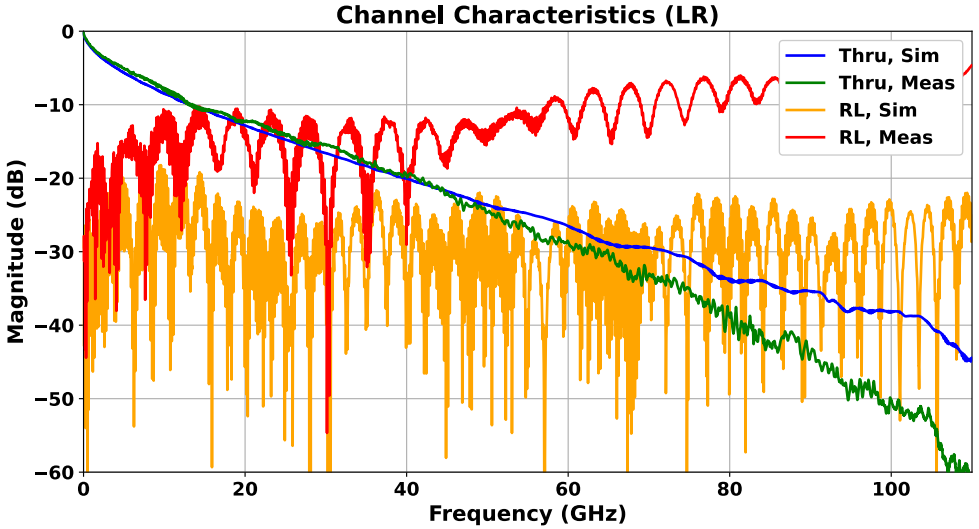
Background

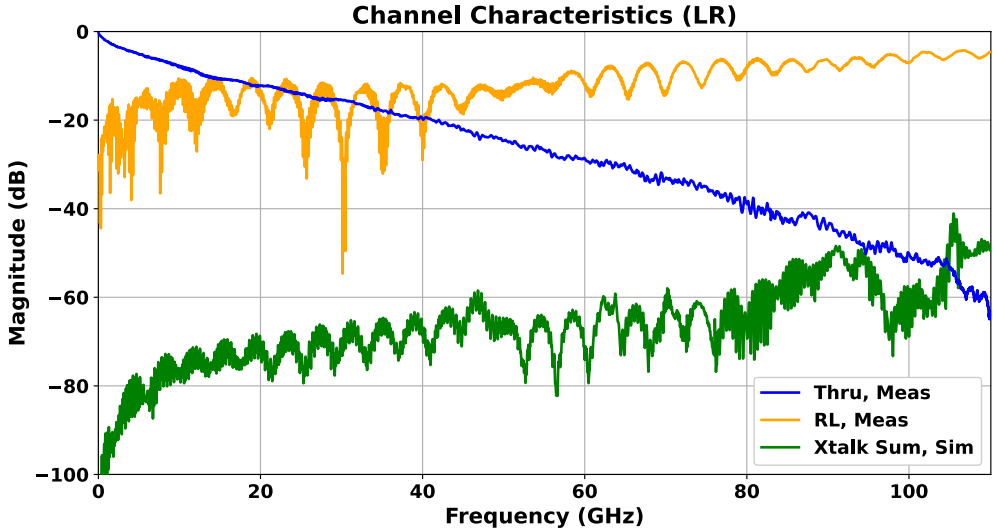
- **400GPL Study Group reached onsensus on 400G/lane AUI and CR objectives.**
  - **Next Steps:** Establishing modulation schemes, FEC baselines, and loss constraints.
- **Intra-Rack Cable Demand & Bottlenecks**
  - Strong end-user preference for copper interconnects within the rack.
  - Channel bandwidth limitation and high insertion loss are the primary physical reach bottleneck.
- **Passive Component & Connector Progress**
  - **Frequency Response Gains:** Rapid progress in high-bandwidth passive components.
  - Measured and simulated channel data demonstrates bandwidth extending beyond **100 GHz**, possibly supporting both **PAM4** and **PAM6** candidates.
- **Tighter cable loss budget due to higher package loss**
  - 40 dB die-to-die loss could be a good starting point to kick off discussion, but we should expect higher loss if we are targeting 1m panel-to-panel.

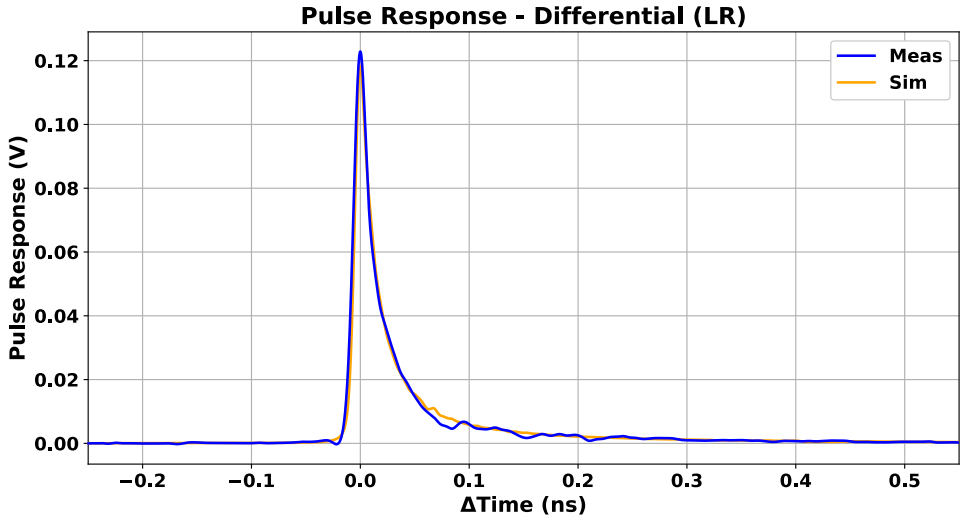
Introduction

- **We provided simulated NPC channel in he_e4ai_01_251023.pdf last year.**
- **This contribution focuses on CR channels with measured data.**
  - A new CR channel is constructed with >100 GHz bandwidth.
- **Both PAM4 and PAM6 modulations could be supported by the new channel.**
  - For PAM4, the legacy end-to-end KP4 FEC is the best choice, considering backward compatibility and technology reuse.
  - PAM6 for cables is getting more popular in recent discussions. We will introduce potential PAM6 modulation schemes followed by some FEC choices to compare their error performance.

Example CR channel – measured NPC w/ package







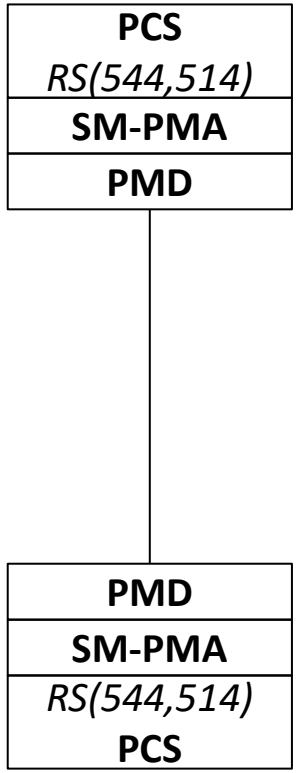
Channel construction:

- Simulated low-loss package
- Measured:
  NPC Conn. + 300 mm Cable + Conn + 300 mm Cable + NPC Conn

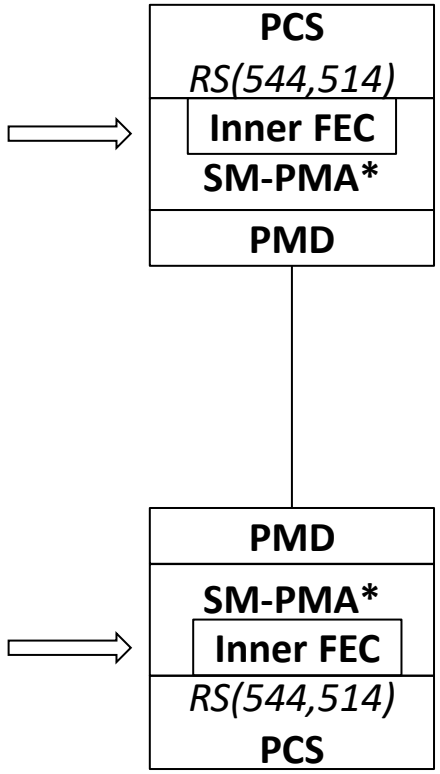
* We are having high-frequency de-embedding issues with the measurements. More corrected data to a higher bandwidth is expected in Q4.

Logic architecture for PAM4 and PAM6 modulations

- PAM4 with end-to-end RS(544,514) – same good old architecture



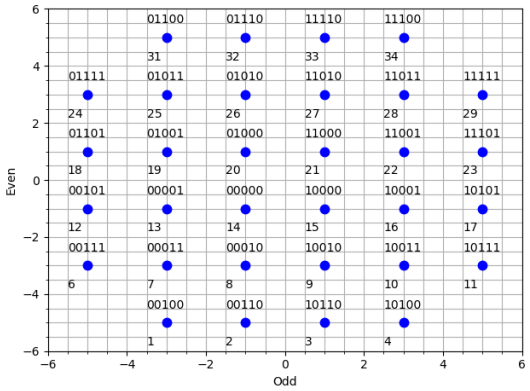
- PAM6 with RS(544,514) concatenated with an inner FEC to compensate SNR loss

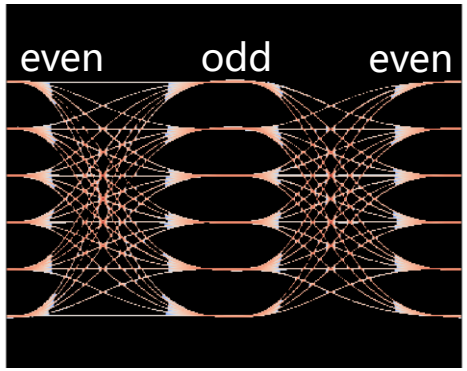


*PAM6 SM-PMA may be different from PMA4 SM-PMA

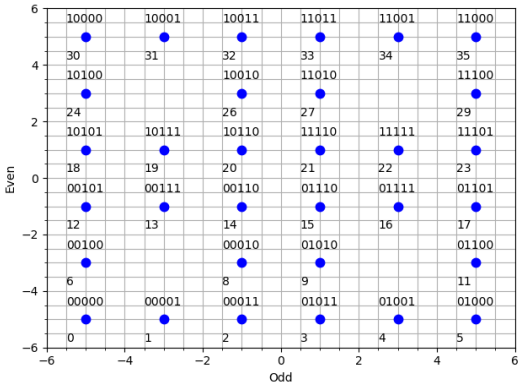
PAM6 modulation schemes

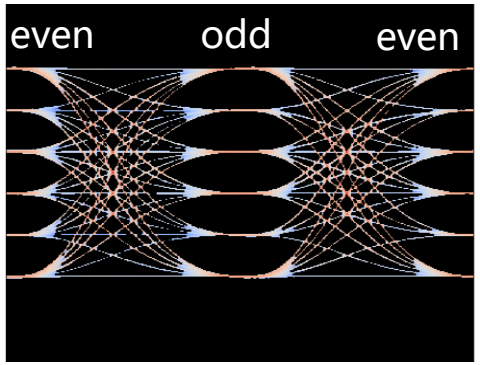
Cross32



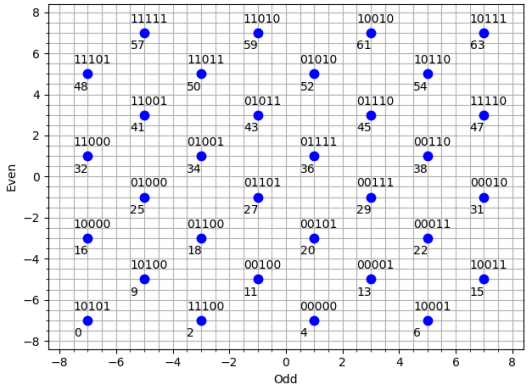


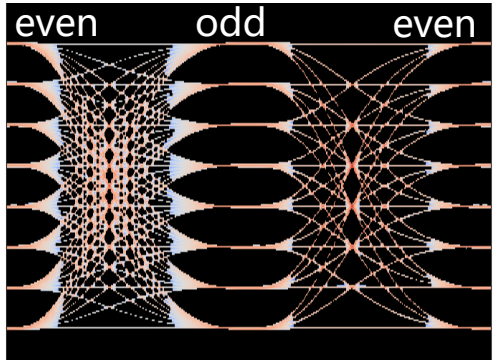
Framed-Cross32

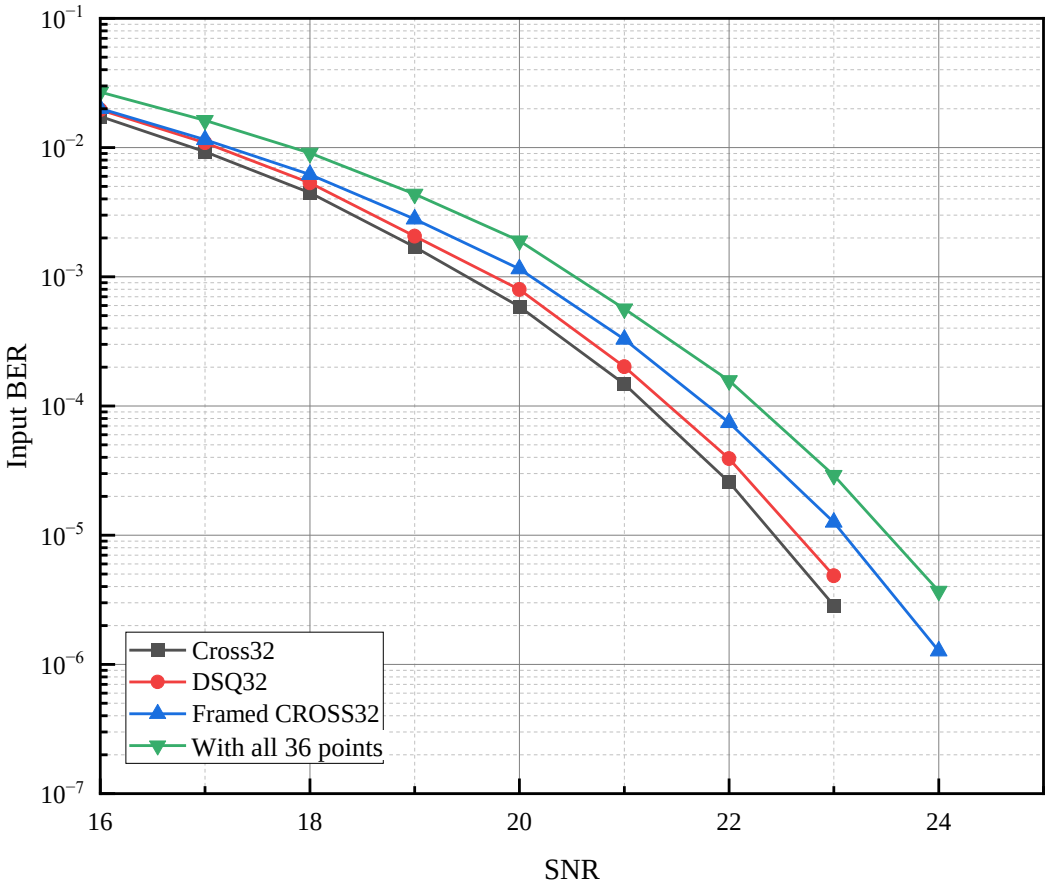




DSQ32



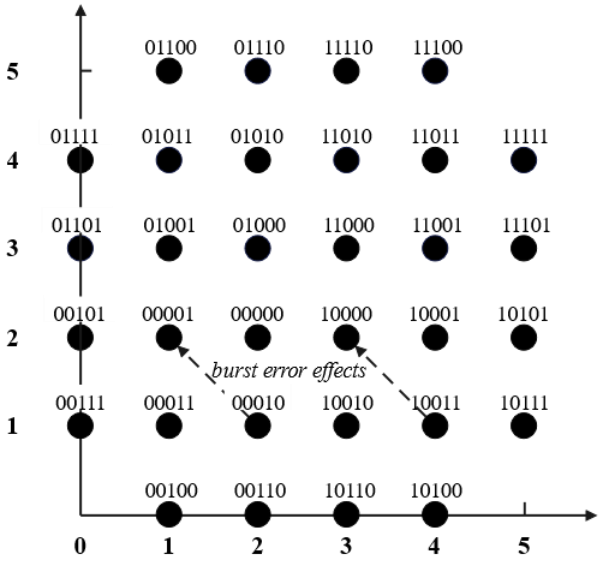


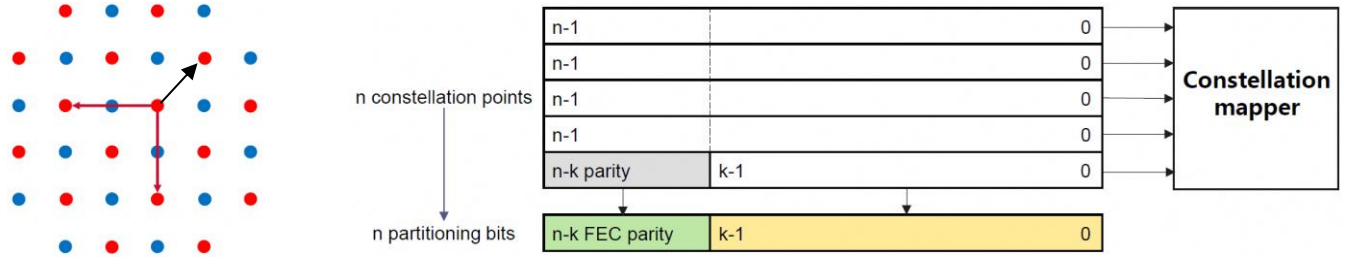


- At the same level of BER and same power level, Cross32 outperforms DSQ32 by 0.2dB, and by 0.7dB against Framed Fross32

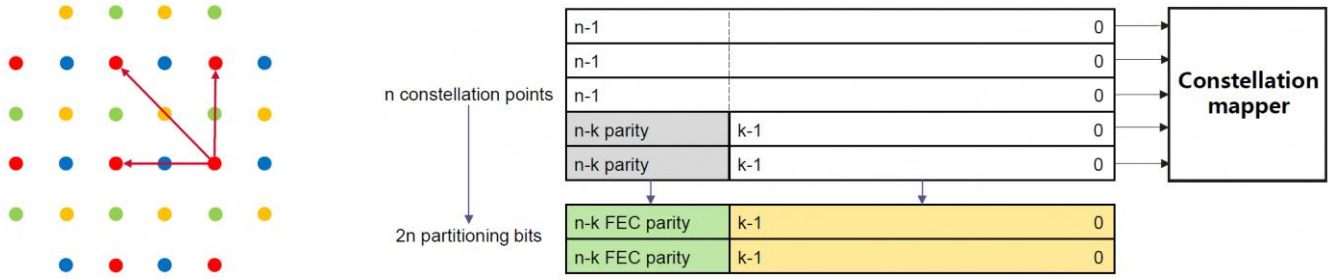
Set Partitioning on 2D-PAM6 (5B2S) with Cross32 constellation

- Set partitioning (SP) splits a 2D-PAM6 constellation into multiple subsets such that $d_{\min}$ within each subset gets larger.
- SP with two subsets[1] uses one partitioning bit to indicate the subset information and detect probable constellation errors. FEC only protects the partitioning bits[2] and corrects the constellation errors.
- A burst error affecting two consecutive PAM6 symbols means a constellation error along the diagonal.
  - SP with two subsets cannot deal with this type of constellation errors as they are in the same subset.
- We further consider ***SP with four subsets (SP4)*** to handle the diagonal constellation errors.





SP with two subsets and FEC protection

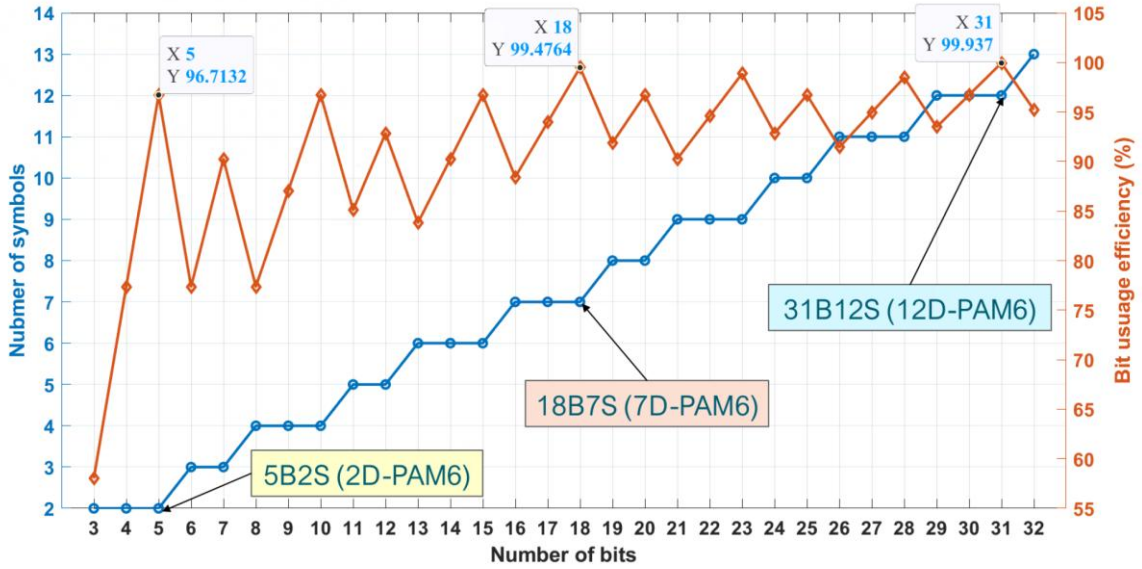


SP with four subsets and FEC protection

[1] C. Liu, “Performance Analysis at 400+Gbps Over Next-Generation VSR Channels”, Ethernet Alliance Technology Exploration Forum 2024.
[2] A. Healey, C. Liu, “Modulations, encoding, and error correction for 448 Gb/s per lane electrical links”, OIF 448Gbps Signaling for AI Workshop 2025.

High-dimensional PAM6 mapping

- With 2D-PAM6 constellation, each PAM6 symbol represents 2.5 bits.
- In theory, one PAM6 symbol could represent $\log_2 6 \approx 2.585$ bits.
- Higher dimensional mapping helps narrow the gap[1]:
  - 18B7S: 2.57 bits/symbol
  - Easily extendable to 41B16S



Credit: Geoff Zhang, Peijun Shan

	# of Binary Bit	Binary Patterns	# of Senary Symbol	Senary Patterns	Capacity	Efficiency
5B2S	5	32	2	36	5.169925002	96.71320180%
6B3S	6	64	3	216	7.754887503	77.37056144%
7B3S	7	128	3	216	7.754887503	90.26565501%
8B4S	8	256	4	1296	10.33985	77.37056144%
9B4S	9	512	4	1296	10.33985	87.04188162%
10B4S	10	1024	4	1296	10.33985	96.71320180%
11B5S	11	2048	5	7776	12.92481251	85.10761758%
12B5S	12	4096	5	7776	12.92481251	92.84467373%
13B6S	13	8192	6	46656	15.50977501	83.81810823%
14B6S	14	16384	6	46656	15.50977501	90.26565501%
15B6S	15	32768	6	46656	15.50977501	96.71320180%
16B7S	16	65536	7	279936	18.09473751	88.42349879%
17B7S	17	131072	7	279936	18.09473751	93.94996746%
18B7S	18	262144	7	279936	18.09473751	99.47643614%
19B8S	19	524288	8	1679616	20.67970001	91.87754171%
20B8S	20	1048576	8	1679616	20.67970001	96.71320180%
21B9S	21	2097152	9	10077696	23.26466251	90.26565501%
22B9S	22	4194304	9	10077696	23.26466251	94.56401954%
23B10S	23	8388608	10	60466176	25.84962501	88.97614565%
24B10S	24	16777216	10	60466176	25.84962501	92.84467373%
25B10S	25	33554432	10	60466176	25.84962501	96.71320180%
26B11S	26	67108864	11	362797056	28.43458751	91.43793625%
27B11S	27	134217728	11	362797056	28.43458751	94.95477995%
28B12S	28	268435456	12	2176782336	31.01955001	90.26565501%
29B12S	29	536870912	12	2176782336	31.01955001	93.48942840%
30B12S	30	1073741824	12	2176782336	31.01955001	96.71320180%
31B12S	31	2147483648	12	2176782336	31.01955001	99.93697519%

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Burst error effect on high-dimensional PAM6 mapping

- A long burst error corrupts successive PAM6 symbols.
  - For high-dimensional mapping, burst errors could cause a large number of bit errors after the inverse mapping.
  - The burst error effect **may** be mitigated by interleaving PAM6 symbols after the inner FEC.

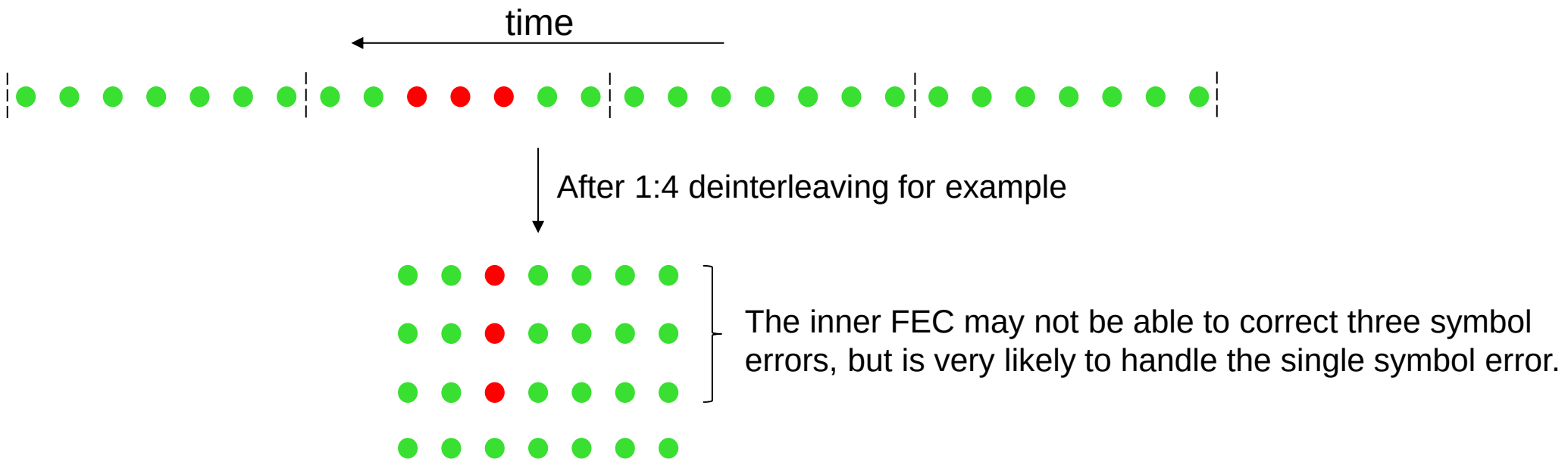


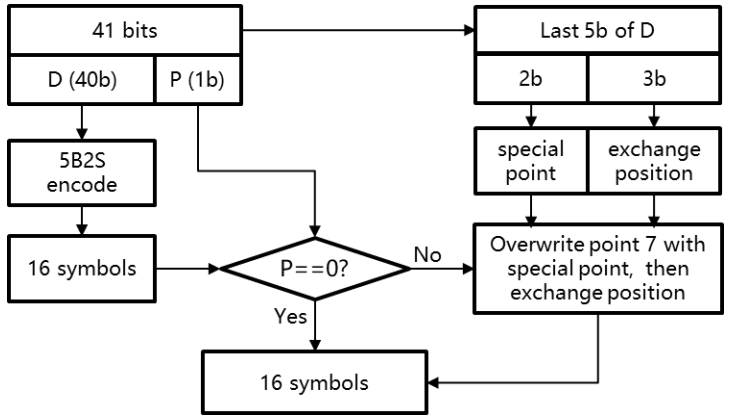
Figure above assuming 18B7S.

- Red dots are symbol errors. Green dots are correct symbols.
- A single burst due to inverse mapping could affect all 7 symbols.

FEC based on 2-set partition with 41B16S

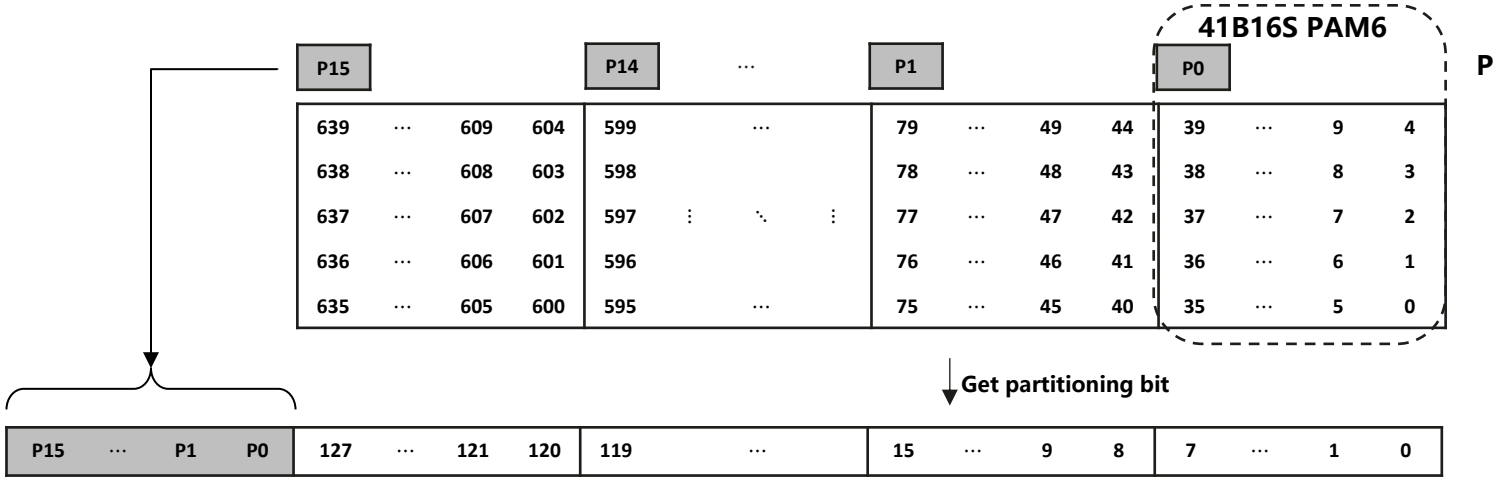
TX process:

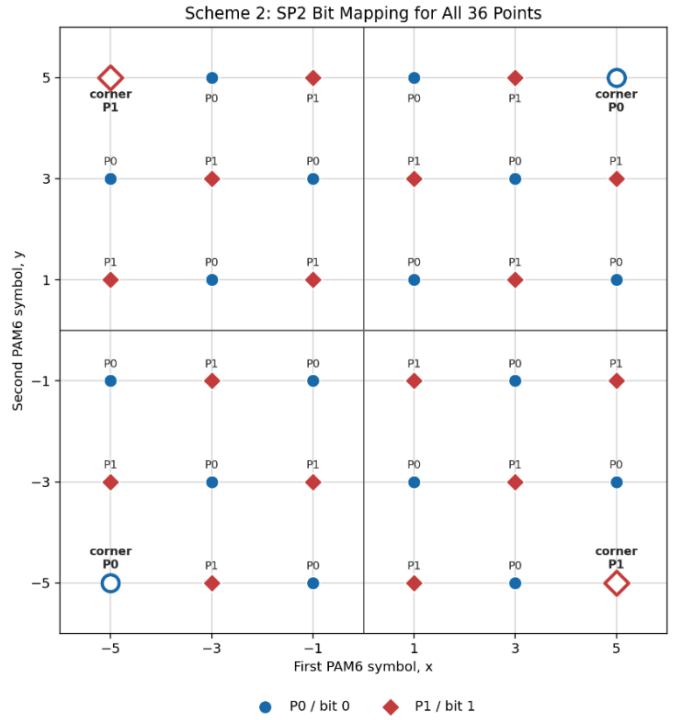
1. Input bits are arranged into matrix format to cooperate FEC encoding and modulation.
2. FEC encoding based on 2-set partition constellation mapping. The parity bit in 41b also affects mapping.
3. Segmenting transmission of input bits for modulation.
4. 41B16S and 5B2S modulations are independent of FEC encode to simplify processing.



RX process:

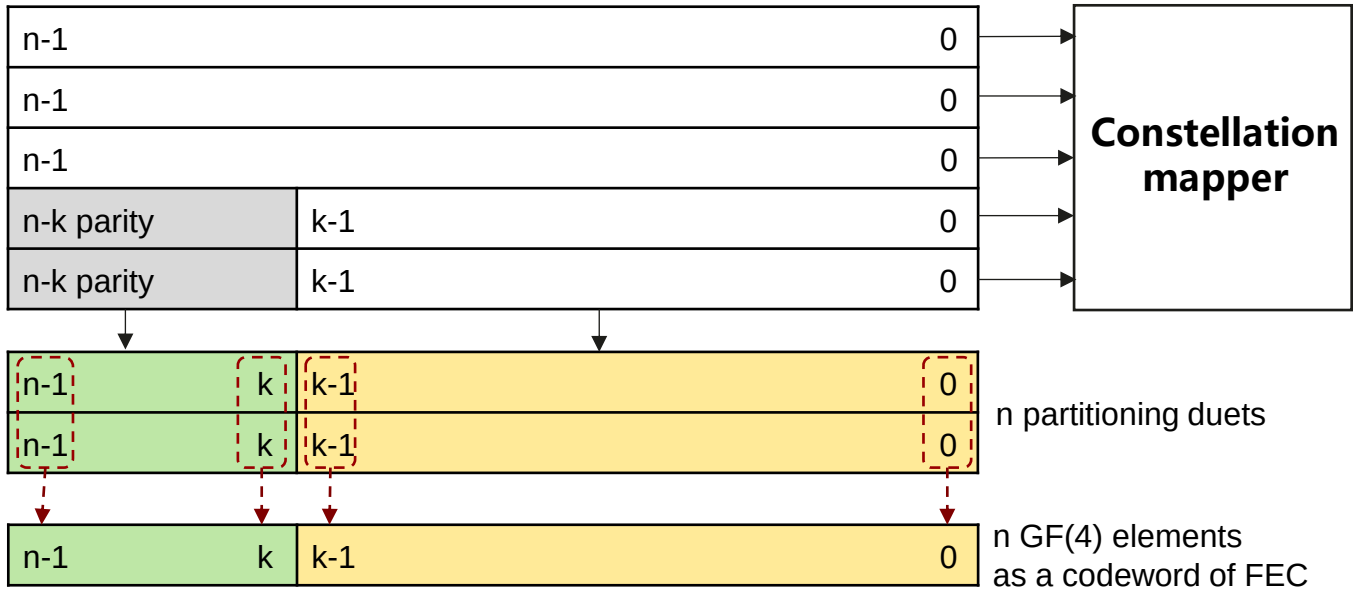
1. Collect FEC codewords based on 2-set partition mapping of received PAM6 symbols, then decoding.
2. Correct up to 2 error position, and check invalid special point cases.
3. De-modulation of 41B16S and 5B2S.

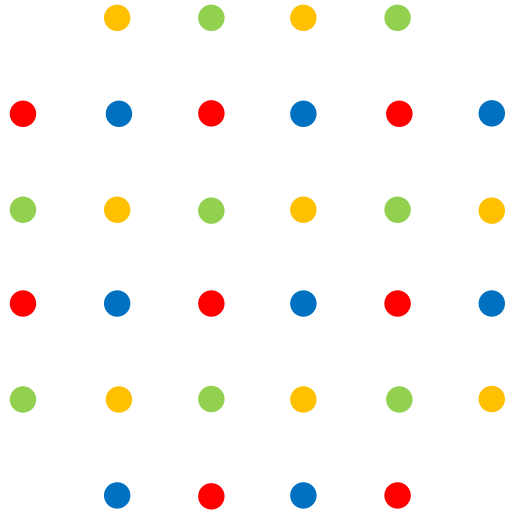




4-set Partitioning with GF(4)-based linear block code

- Treat partitioning duets of a constellation as an GF(4) element and protect with GF(4)-based linear block code.
- GF(4)-based FEC can correct partitioning duets instead of partitioning bits.
- 2(n-k) parity bits are added such that the corresponding n partitioning duets form an GF(4)-based FEC codeword.





Simulation results (AWGN channel)

- Four-way interleaved KP4 is used as the outer FEC.
- Four Inner FEC schemes are considered:
  1. Binary(340,330) for Cross32 with soft-decision decoding, w/ convolutional interleaver and circular shift functions as in P802.3dj.
  2. SP4(660,640) for Cross32 with hard-decision decoding
     a. Partitioning bits protected by binary BCH
     b. Partitioning bits protected by a GF(4) code
  3. Binary(648,630) for 18B7S with hard-decision decoding
  4. Binary(656,640) for 41B16S with hard-decision decoding

Inner FEC	SNR (dB)	Pre-inner FEC BER	FLR	Coding gain (dB)	Inner FEC overhead	Lane Rate (Gbps)	Bandwidth (GHz)
Option 1	18.71	2.4e-3	6.2e-11	8.57	3.03%	437.9	87.6
Option 2a	19.58	9.7e-4		7.70	3.125%	438.3	87.7
Option 2b	19.60	9.5e-4		7.68	3.125%	438.3	87.7
Option 3	19.70	8.4e-4		7.58	2.857%	437.1	85
Option 4	19.77	7.8e-4		7.51	2.5%	435.6	85

Coding gain is calculated against no FEC case.
For NCG, subtract about 0.3dB out of option 1 and 2.

Simulation results (1+0.5D, precoding off)

- Four-way interleaved KP4 is used as the outer FEC.
- Four Inner FEC schemes are considered:
  1. Binary(340,330) for Cross32 with soft-decision decoding, w/ convolutional interleaver and circular shift functions as in P802.3dj.
  2. SP4(660,640) for Cross32 with hard-decision decoding
     a. Partitioning bits protected by binary BCH
     b. Partitioning bits protected by a GF(4) code
  3. Binary(648,630) for 18B7S with hard-decision decoding
  4. Binary(656,640) for 41B16S with hard-decision decoding

Inner FEC	SNR (dB)	Pre-inner FEC BER	FLR	Coding gain (dB)	Inner FEC overhead	Lane Rate (Gbps)	Bandwidth (GHz)
Option 1	18.39	2.2e-3	6.2e-11	8.89	3.03%	437.9	87.6
Option 2a	19.22	7.5e-4		8.06	3.125%	438.3	87.7
Option 2b	19.10	8.9e-4		8.18	3.125%	438.3	87.7
Option 3	19.24	7.3e-4		8.04	2.857%	437.1	85
Option 4	19.26	7.1e-4		8.02	2.5%	435.6	85

Coding gain is calculated against no FEC case.
For NCG, subtract about 0.3dB out of option 1 and 2.

Simulation results (1+0.9D, precoding on)

- Four-way interleaved KP4 is used as the outer FEC.
- Four Inner FEC schemes are considered:
  1. Binary(340,330) for Cross32 with soft-decision decoding, w/ convolutional interleaver and circular shift functions as in P802.3dj.
  2. SP4(660,640) for Cross32 with hard-decision decoding
     a. Partitioning bits protected by binary BCH
     b. Partitioning bits protected by a GF(4) code
  3. Binary(648,630) for 18B7S with hard-decision decoding
  4. Binary(656,640) for 41B16S with hard-decision decoding

Inner FEC	SNR (dB)	Pre-inner FEC BER	FLR	Coding gain (dB)	Inner FEC overhead	Lane Rate (Gbps)	Bandwidth (GHz)
Option 1	18.24	1.3e-3	6.2e-11	9.04	3.03%	437.9	87.6
Option 2a	18.65	7.3e-4		8.63	3.125%	438.3	87.7
Option 2b	18.60	7.9e-4		8.68	3.125%	438.3	87.7
Option 3	18.64	7.4e-4		8.64	2.857%	437.1	85
Option 4	18.70	6.8e-4		8.58	2.5%	435.6	85

Coding gain is calculated against no FEC case.
For NCG, subtract about 0.3dB out of option 1 and 2.

Latency and area comparison of inner FEC options

- Four-way interleaved KP4 is used as the outer FEC.
- Four Inner FEC schemes are considered:
  1. Binary(340,330) for Cross32 with soft-decision decoding, w/ convolutional interleaver and circular shift functions as in P802.3dj.
  2. SP4(660,640) for Cross32 with hard-decision decoding
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  3. Binary(648,630) for 18B7S with hard-decision decoding
  4. Binary(656,640) for 41B16S with hard-decision decoding

Inner FEC	Operating rate (Gbps)	TX+RX Latency[1] (ns)	Relative Area[2]
Option 1	437.9	53	3.91
Option 2a	438.3	22	1.00
Option 2b	438.3	22	1.00
Option 3	437.1	23	1.02
Option 4	435.6	23	0.92

1. Latency is evaluated based on 1 GHz clock frequency (1 ns per cycle).
2. High-dimensional modulation like 18B7S and 41B16S may require additional logic in implementation.

Summary

- A CR channel with >100GHz bandwidth has been presented.
- Several PAM6 modulation schemes have been discussed.
  - 5B2S w/ Cross32, 18B7S and 41B16S are considered.
  - Different Inner FEC designs were shown for performance comparison.
  - We proposed a 4-set partitioning (SP4) method to correct diagonal constellation errors for Cross32.
  - A new FEC over GF(4) was introduced to protect partitioning bits of SP4.
  - Efficient coding scheme for 41B16S was shown, too.
- Different Inner FEC schemes of similar overhead show close error performance.

Thank you!