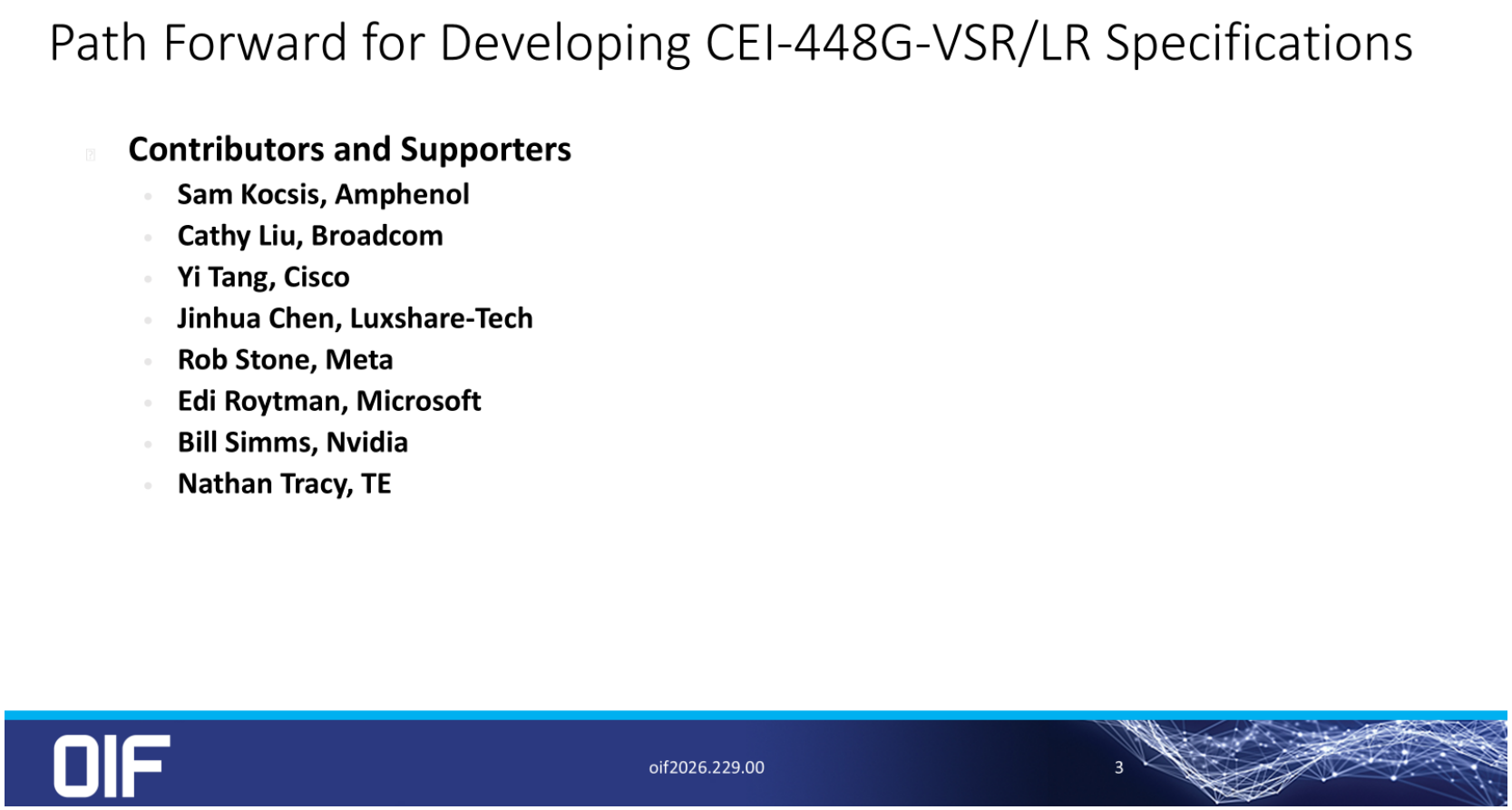
Path Forward for Developing IEEE 802.3 400GPL C2M/CR Specifications

Mike Li, AMD
Ed Frlan, Semtech
Sept 10th, 2026

Background

- This presentation is developed based on a recent and relevant contribution made at the OIF Q3/2026 [1], which has been updated to be appropriate for 802.3dv 400GPL C2M/CR electrical/copper interfaces



OIF2026.229

Adopted IEEE 802.3 400GPL SG Objectives[2]

400GPL SG Objectives (1/4)

Non-Rate Specific

- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum FrameSize of current IEEE 802.3 standard
- Support a BER of better than or equal to 10-13 at the MAC/PLS service interface (or the frame loss ratio equivalent)

400GPL SG Objectives (2/4)

400 Gb/s Related

- Support a MAC data rate of 400 Gb/s
- Support optional single-lane 400 Gb/s attachment unit interfaces for chip-to-module and chip-to-chip applications
- Define a physical layer specification that supports 400 Gb/s operation over 1 pair of SMF with lengths up to at least 500 m
- Define a single-lane, 400 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter

400GPL SG Objectives (3/4)

800 Gb/s Related

- Support a MAC data rate of 800 Gb/s
- Support optional two-lane 800 Gb/s attachment unit interfaces for chip-to-module and chip-to-chip applications
- Define a physical layer specification that supports 800 Gb/s operation over 2 pairs of SMF with lengths up to at least 500 m
- Define a two-lane, 800 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter

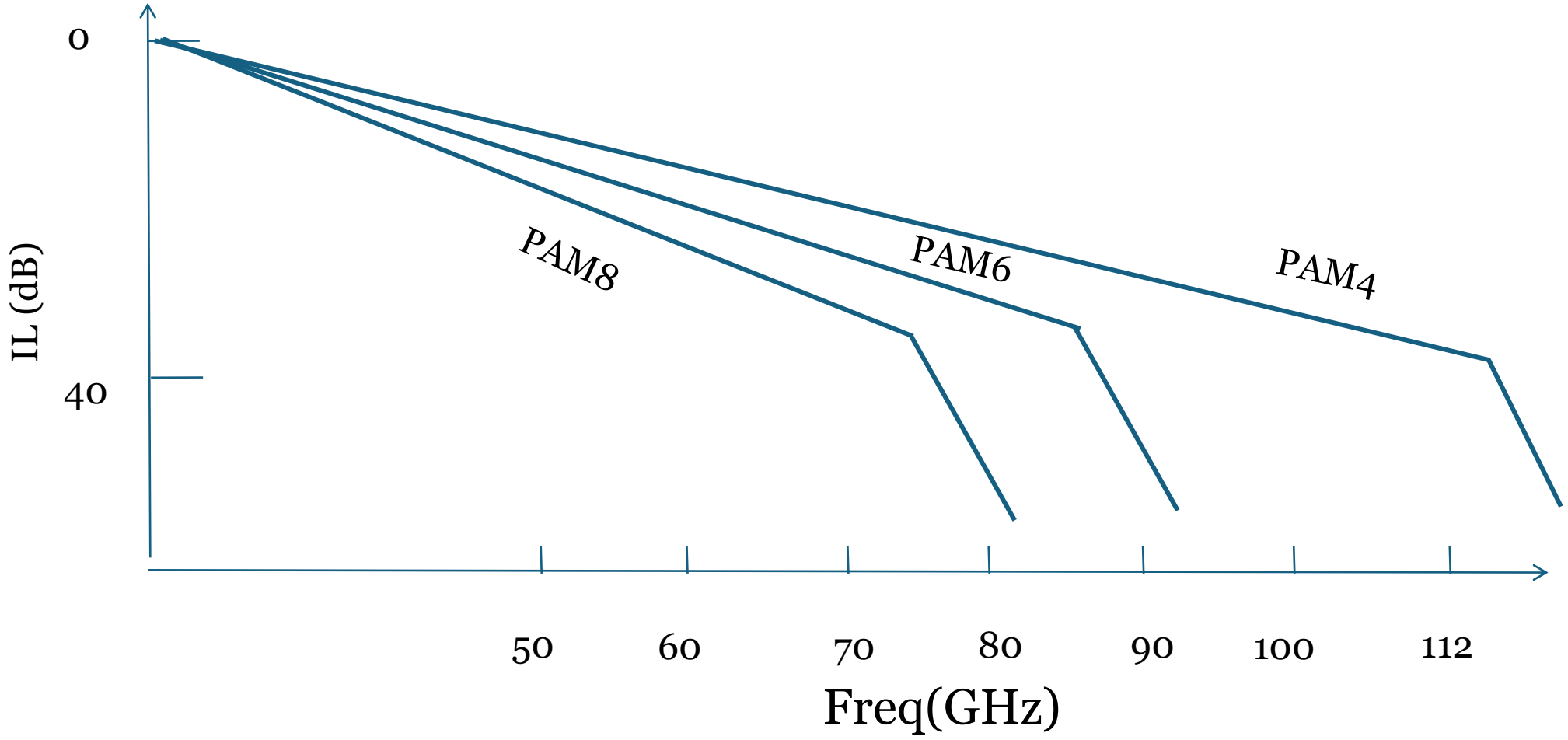
400GPL SG Objectives (4/4)

1.6 Tb/s Related

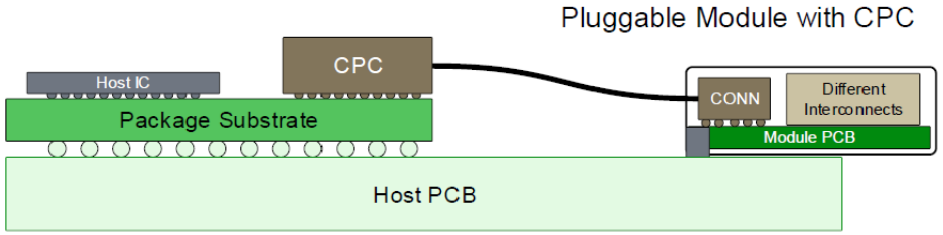
- Support a MAC data rate of 1.6 Tb/s
- Support optional four-lane 1.6 Tb/s attachment unit interfaces for chip-to-module and chip-to-chip applications
- Define a physical layer specification that supports 1.6 Tb/s operation over 4 pairs of SMF with lengths up to at least 500 m
- Define a four-lane, 1.6 Tb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter

400GPL Channel IL vs PAMn

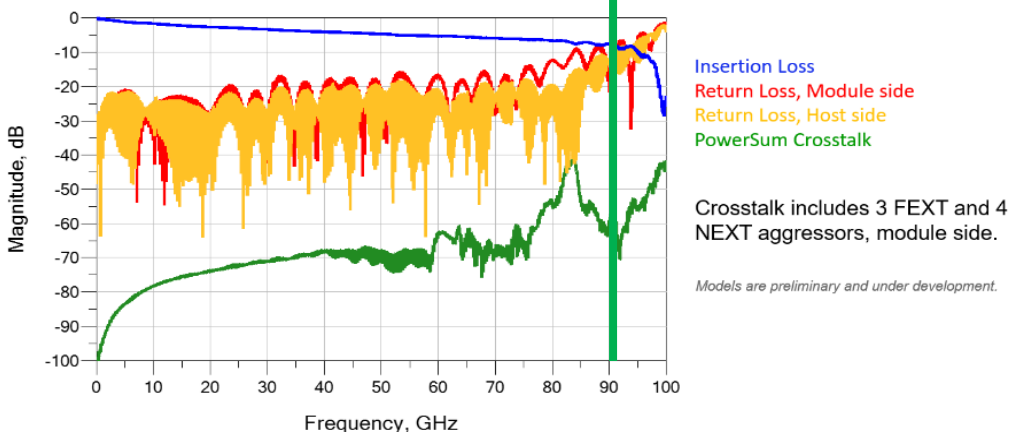
- PAMn choice critically depends on the channel bandwidth



400GPL–C2M Channels

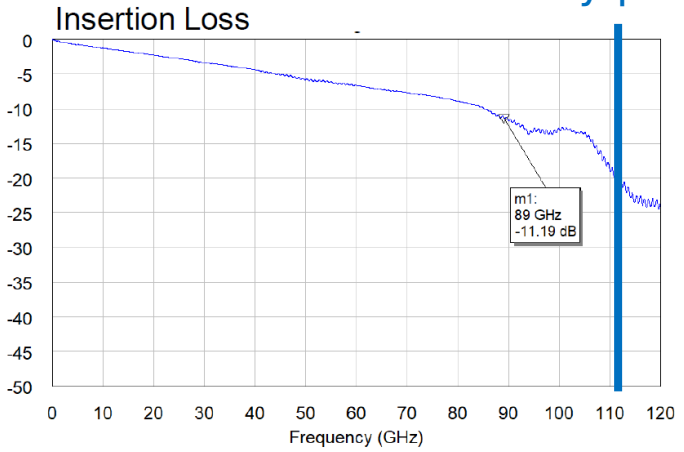


PAM6 Nyquist



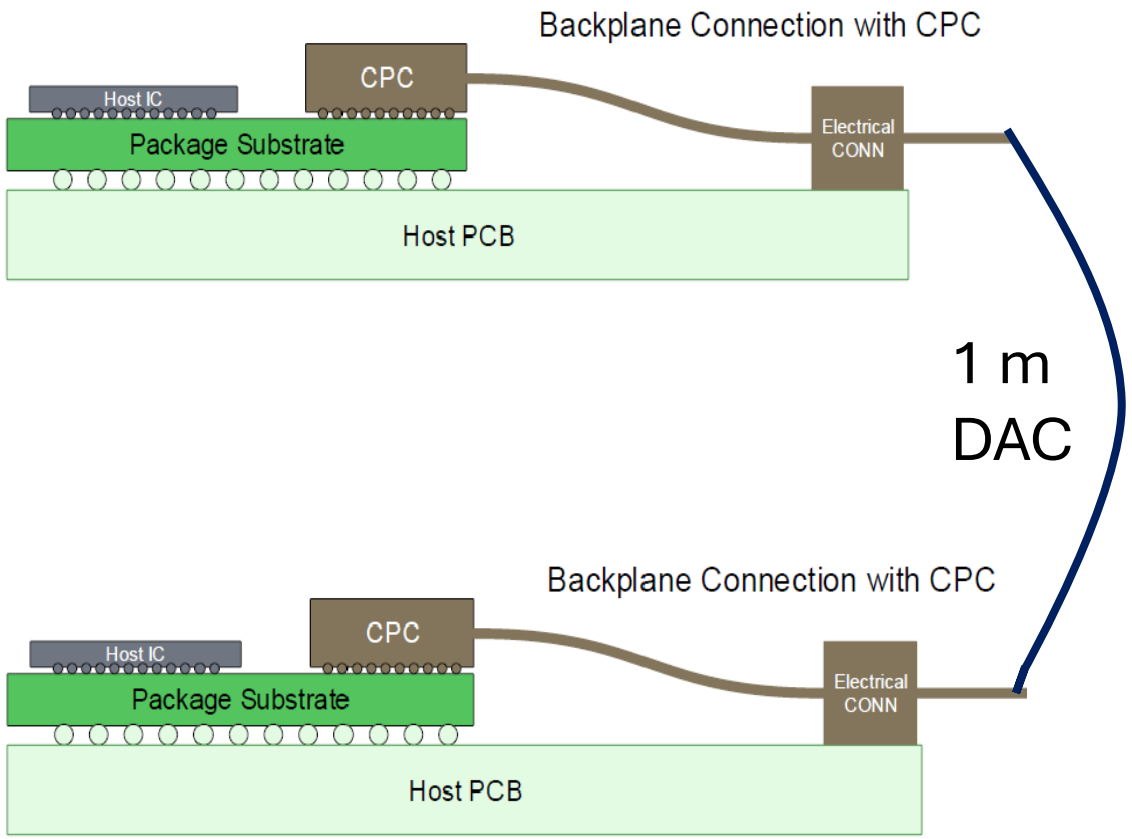
Available [3]

PAM4 Nyquist

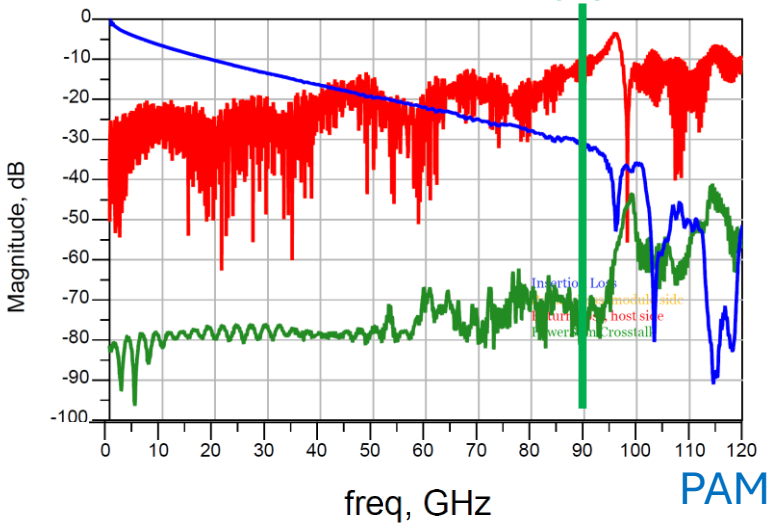


Under Development [4]

400GPL-CR Channels

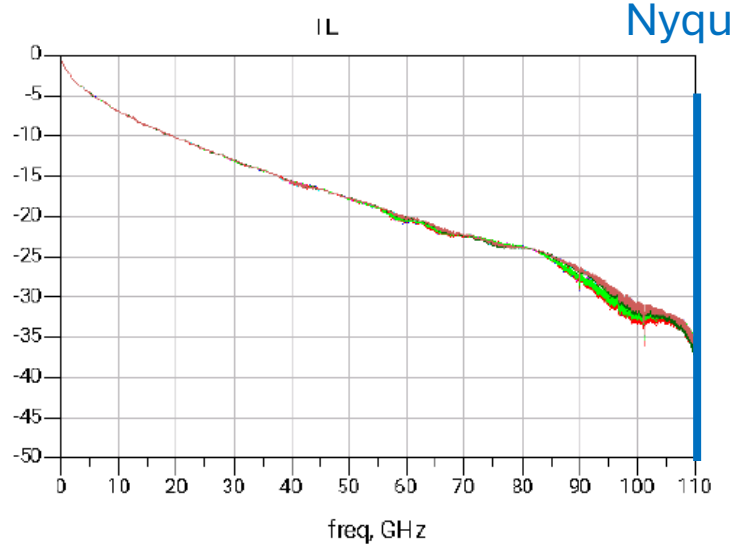


PAM6 Nyquist



Available [5]

PAM4 Nyquist



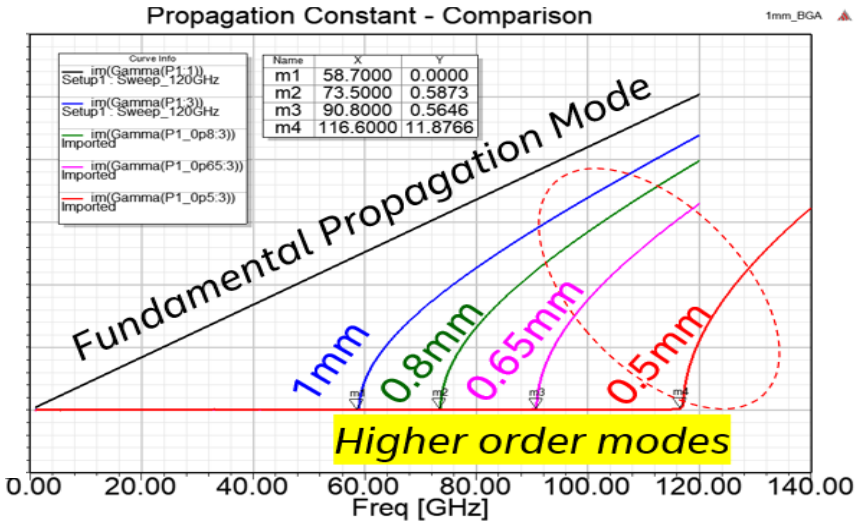
Under Development [6]

400GPL SERDES

- 400GPL-PAM4/PAM6 SERDES test chips had demonstrated the feasibility with 3nm publicly [7], or privately
  - More TC results are expected to become publicly available
  - PPA would be further improved if using 2nm or 18A

400GPL Package

- Package BW depends on ball pitch
  - 112G (PAM4): ≤ 1mm
  - 224G (PAM4): ≤ 0.8mm
  - 448G (PAM4): ≤ 0.5mm
- **Package ball pitch of <= 0.5 mm is available today**



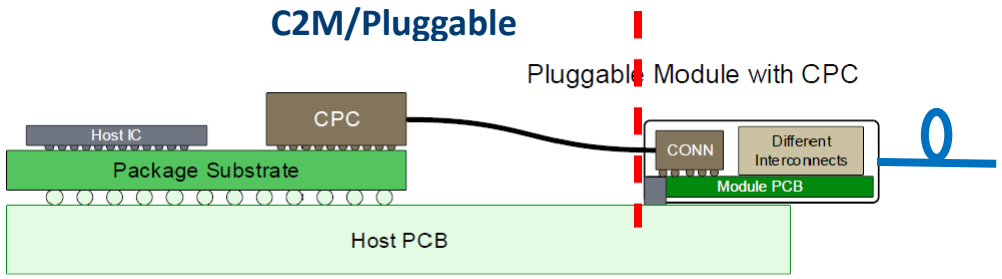
Cut-off frequency of BGA ball pitch

BGA pitch	1.0mm	0.8mm	0.65mm	0.5mm
Cutoff Frequency	58GHz	72GHz	90GHz	115GHz

	224G		448G			
Modulation	PAM4	PAM6	PAM4	PAM6	PAM8	PAM16
Nyquist Freq, GHz	56 GHz	44.8 GHz	112 GHz	89.6 GHz	74.67 GHz	56 GHz

- PKG can support 400GPL-PAM4/PAM6 signaling [8]

400GPL Chip-to-Module Modulation Considerations



	e-C2M	o-DR	Notes
212.5G	**PAM4**	**PAM4**	
425G -PAM4 elec -PAM4 opt	**PAM4 -Desirable for elec to opt alignment -Unknown if production is feasible**	**PAM4 -Desirable for elec to opt alignment -Desirable for better SNR**	**vs PAM6 elec • e-o compatibility • Higher BW, lower SNR penalty • Enable LPO/lower power/latency/cost • Lower latency in optical links/backward compatibility • Production feasibility under investigation • Elec channel reach is compromised**
425G -PAM6 elec -PAM4 opt	**PAM6 -Improved production feasibility -Undesirable for elec to opt alignment**	**PAM4 -Undesirable for elec to opt alignment -Doesn't get to the lowest power (LPO)**	**vs PAM4 • Better TTM • Lower BW, higher SNR penalty • No e-o compatibility without gearbox • No LPO/lower power/latency/cost**

IEEE 802.3 400GPL –C2M/CR Path Forward

- 425G-PAM4/PAM6 SERDES feasibility with test chips have been demonstrated by multiple vendors
- 425G PKG with CPC has the BW to support both PAM4 and PAM6 modulation
- 425G C2M/CR channels has production solution with PAM6 today, and with PAM4 in the near future
- Developing both PAM6 and PAM4 specifications for IEEE 400GPL C2M/CR meet the project start requirements and serve the end customers needs of
  - Time to market (TTM)
    - with the channel technology today
  - Power/latency/perf optimized
    - with the channel technology in the near future

References

1. M. Li, K. Lusted, “Path Forward for Developing CEI-448G-VSR/LR Specifications “, OIF, OIF2026.229, 2026
2. IEEE 802.3 400 Gb/s/lane “400GPL” SG Objectives
3. C. Liu, N. Tracy, M. Li, R. Stone, K. Lusted, Y. Tang, J. Maki, J. Calvin, “Next Generation CEI-448G Framework”, OIF, oif2025.346.05, 2025
4. T. Ito, “Insertion loss and Routing Length of VLC-PCB for 448G”, OIF, oif2025.178.13, 2025
5. A. P. Shaji, “400G/lane Interconnects for AI: Channel Feasibility, Reach Extension, and Early Measurement Results”, Ethernet for AI, TEF/Ethernet Alliance, 2025
6. A. Kim, J. Chen, C. Liu, “Advanced Connector Technologies in Support of 400G Signaling – VSR and LR study”, OIF, oif2026.253.00, 2026
7. N. Ben-Hamida, “448G Technology for Next Gen Networking”, Ethernet for AI, TEF/Ethernet Alliance, 2025
8. M. Li, “The Path to 448G in Support of Next Generation AI: Electrical Channel and Modulation Considerations”, Ethernet for AI, TEF/Ethernet Alliance, 2025

Thank You !