400G/800G/1.6T Logic Architecture Considerations

Gary Nicholl, Cisco
Eugene Opsasnick, Broadcom
Matt Brown, Qualcomm
Xiang He, Huawei
Shawn Nicholl, AMD
Adee Ran, Cisco

Supporters and Contributors

Contributor

- Kent Lusted

Outline

- P802.3dj Review
- Starting Assumptions for P802.3dv
- Future Work Areas

P802.3dj Logic Architecture (Review)

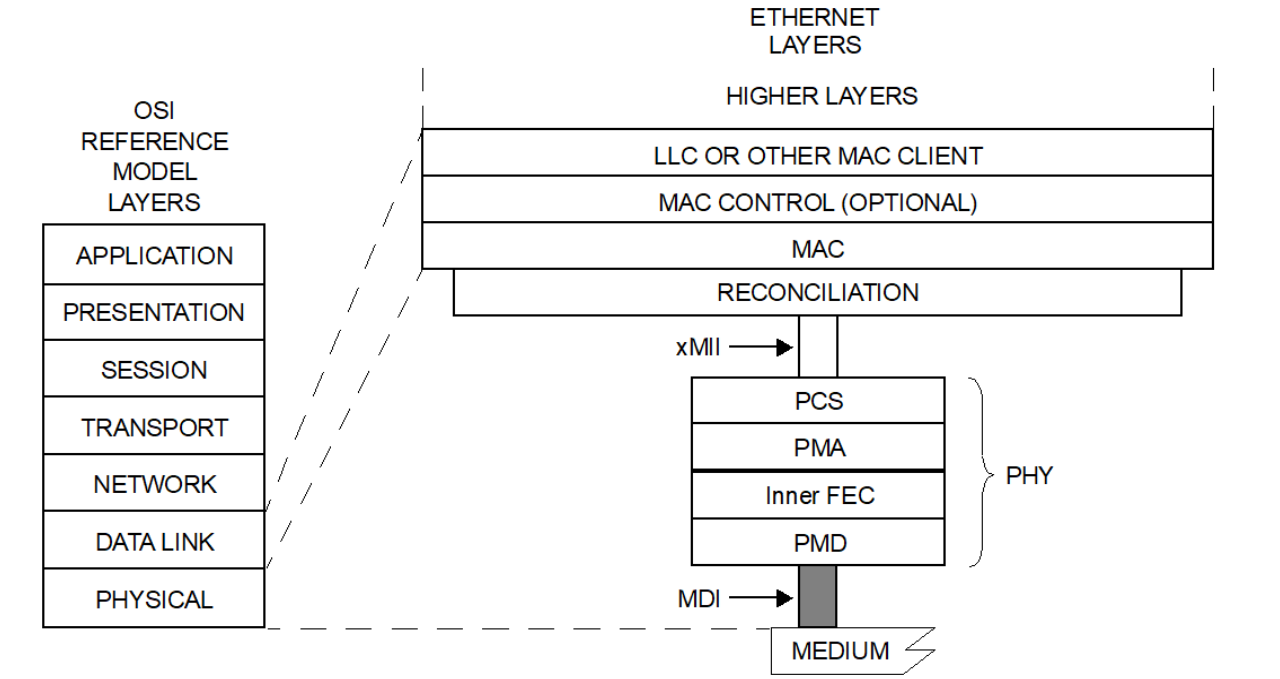
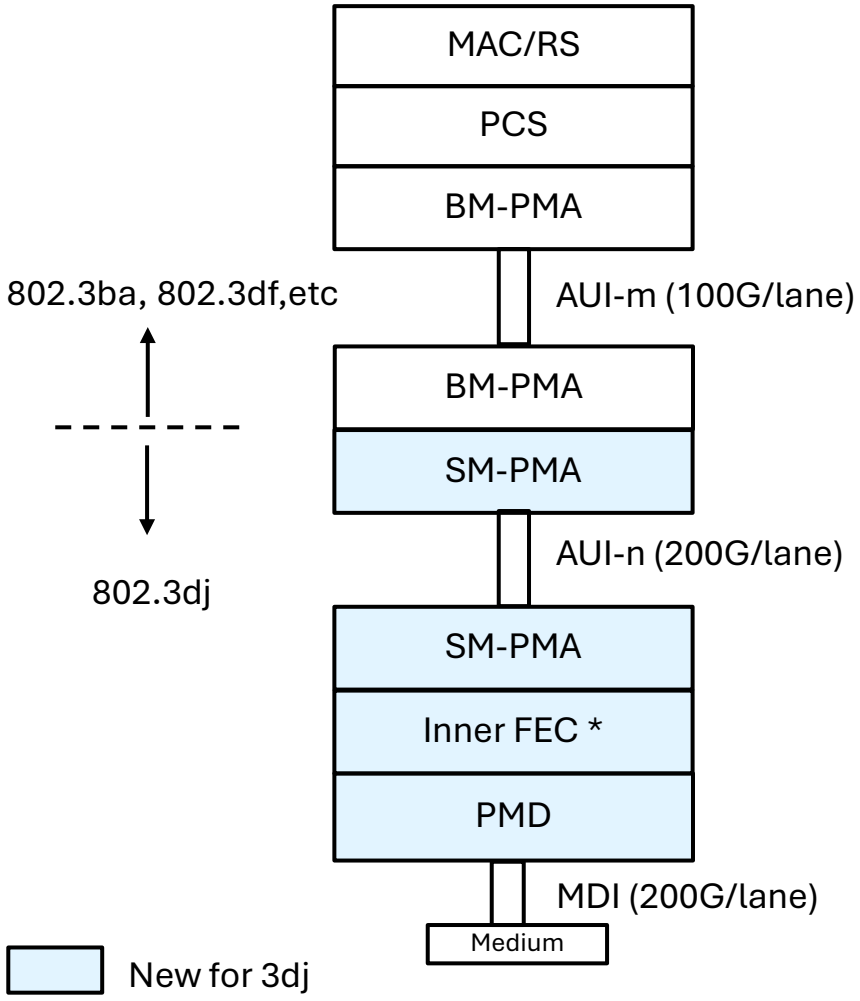


Figure 177–1—Relationship of Inner FEC to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

- Based on existing 802.3 architecture
- PCS includes RS FEC
- Flexible architecture that supports different FEC schemes (end-to-end, concatenated and segmented)
- New:
  - RS Symbol muxing PMA (SM-PMA)
  - Inner FEC sublayer (conditional based on PMD)

P802.3dj Logic Architecture (Review)



SM-PMA

- RS symbol-muxing PMA
- In conjunction with PCS, this results in 200G lanes that are **all** RS symbol muxed and 4 RS codeword interleaved
- Improves burst error tolerance
- Note: conversion between legacy bit-muxed 100G lanes and new symbol-muxed 200G lanes is achieved via back-to-back BM-PMA and SM-PMA (nice specification trick!)

Inner FEC

- Additional FEC conditional on PMD type
- Added “on top” of existing RS FEC (in PCS), i.e. increases lane rate (sometimes called “concatentated FEC”)

* Inner FEC conditional on PMD type includes

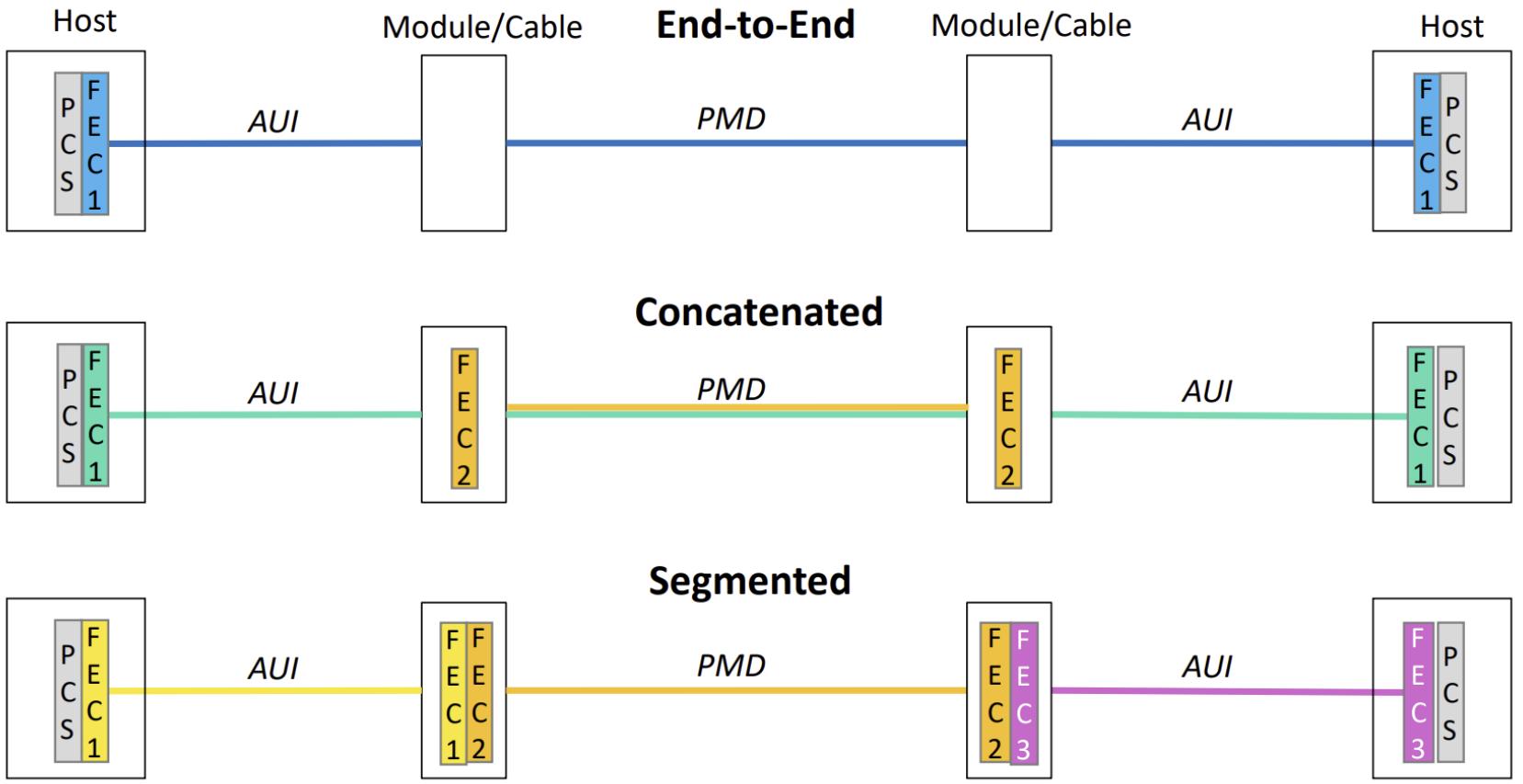
P802.3dj FEC Schemes

FEC 1: is end-to-end (AUI+PMD+AUI)

FEC 1 (outer): (AUI+ partial PMD+AUI)

FEC 2 (inner): (PMD only)

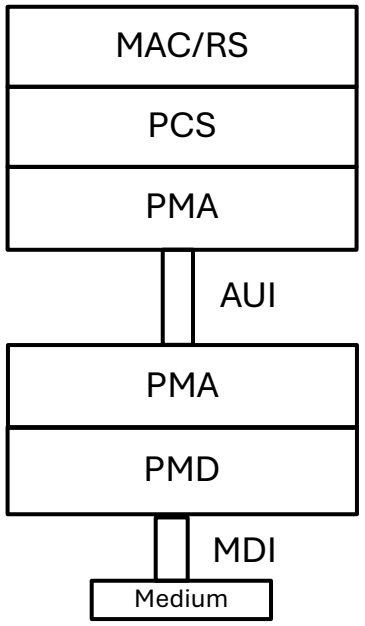
FEC 1: left AUI only
FEC 2: PMD only
FEC 3: right AUI only



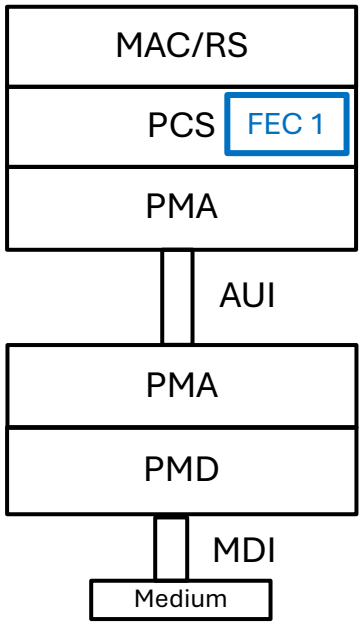
Source: shrikhande_3df_01a_220203

P802.3dj FEC Architecture Flexibility

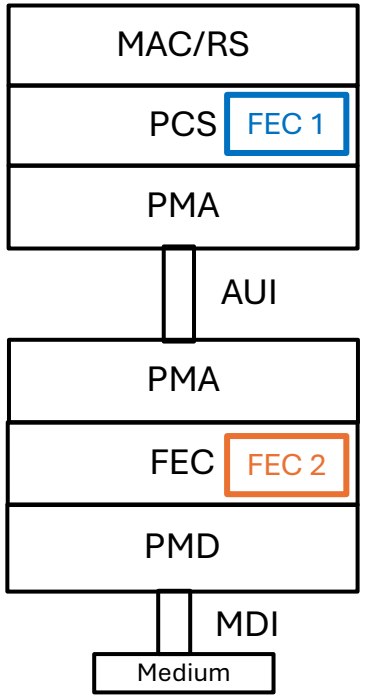
Generic 3dj Architecture



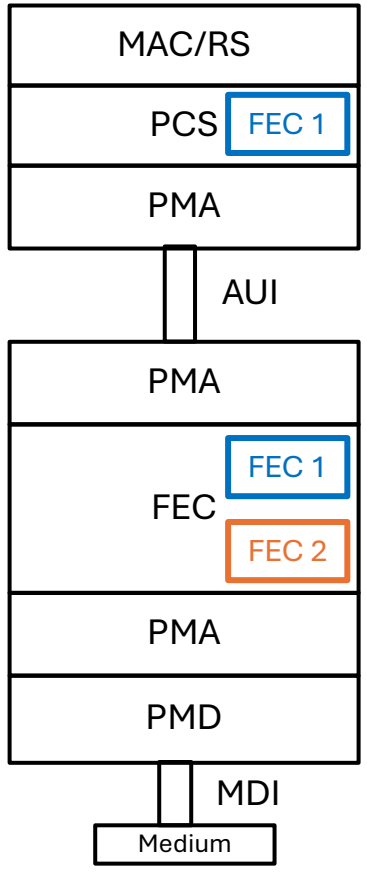
FEC location for End-to-end option



FEC location for Concatenated option

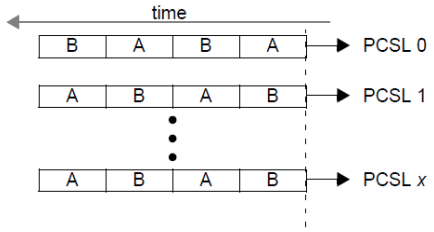


FEC location for Segmented option

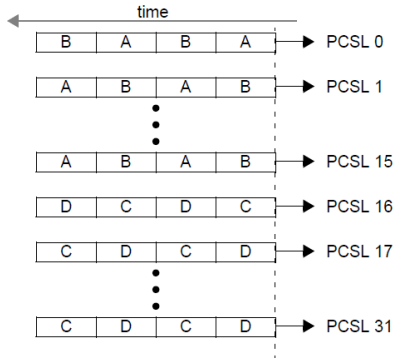


Architecture supports all FEC schemes

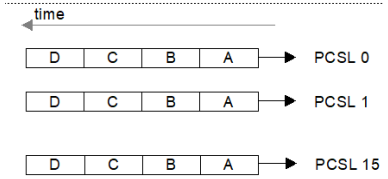
P802.3dj PMA



200GBASE-R, 400GBASE-R



800GBASE-R



1.6TBASE-R

SM-PMA (Clause 176)

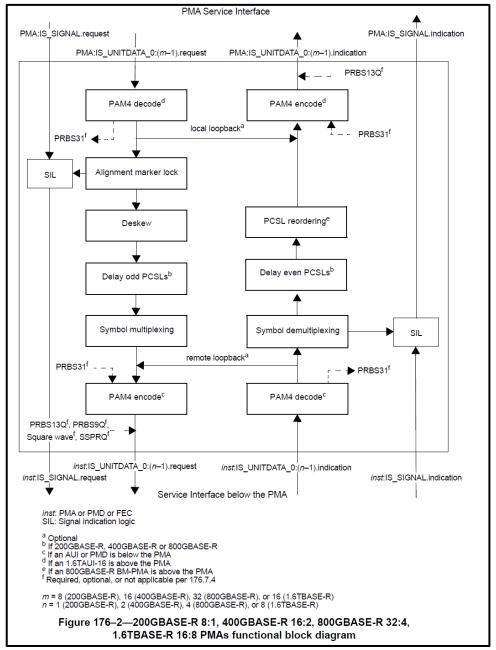
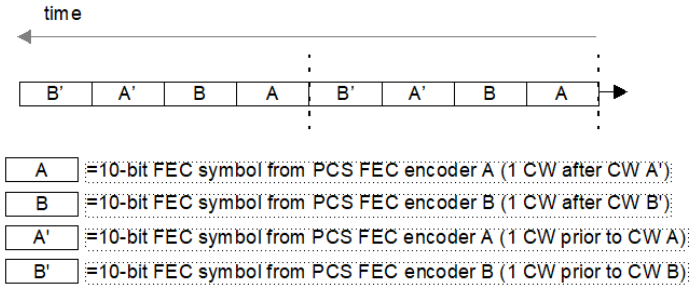
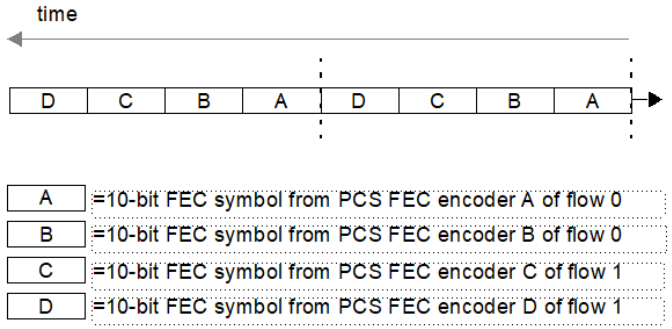


Figure 176–2—200GBASE-R 8:1, 400GBASE-R 16:2, 800GBASE-R 32:4, 1.6TBASE-R 16:8 PMAs functional block diagram

- Operates on PCS lanes and generates 200G lanes based on RS symbol muxing with 4 CW interleave
- Note: functionality of PMA is rate dependent to accommodate the different PCS lane formats for 200GBASE-R, 400GBASE-R, 800GBASE-R and 1.6TBASE-R



200GBASE-R/400GBASE-R



800GBASE-R/1.6TBASE-R

Starting Assumptions for P802.3dv “400GPL”

- Build upon P802.3dj
  - Use existing 400G, 800G, 1.6T PCS (Clause 119, 172 and 175)
  - Use existing SM-PMA (Clause 176)
- RS 544 FEC, with RS symbol muxing and 4 CW interleave
  - Get there via combination of PCS and PMA (same as 802.3dj)
- Support legacy 200 G/lane AUIs

P802.3dv Areas for Study

- Details of PMA Mapping to 400G/lane
- How many AUI rates back do we need to support?
  - 200G/lane, 100G/lane? 50G/lane?
- Considerations for PAM4 and PAM6 modulations
- Inner FEC
- Additional FEC Schemes?

Summary

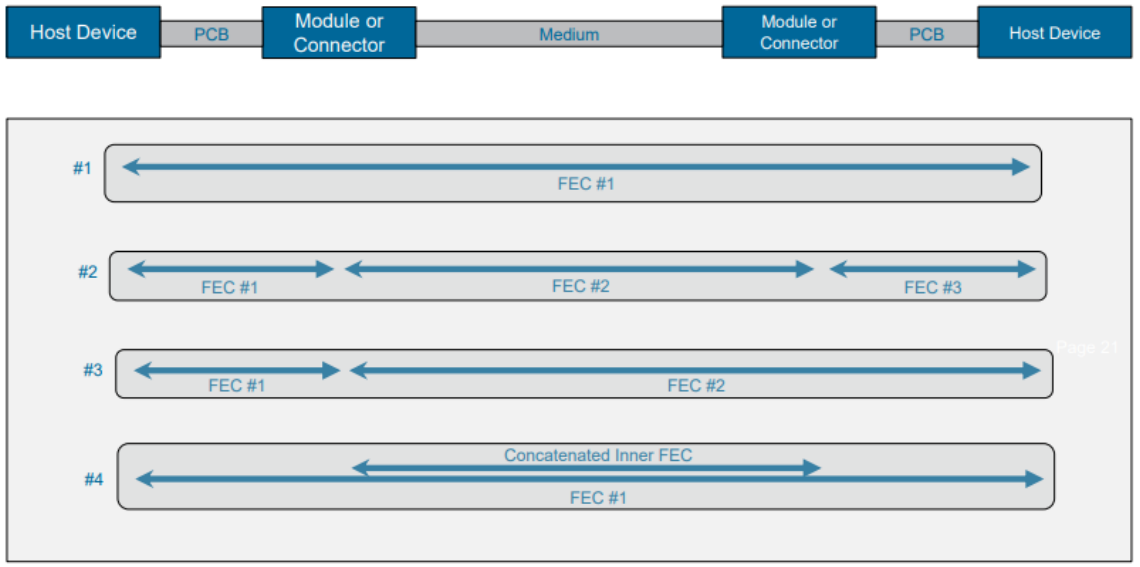
- The P802.3dj logic architecture is a great place to start
  - Flexibility to support different FEC schemes
  - Based on RS symbol muxing with 4 CW interleave for all rates
- Before we consider changing the logic, we should understand if changes are necessary
- More updates in November

Thanks!

P802.3dj FEC Schemes

Possible FEC Schemes for 200Gbps/lane

200 Gbps/lane



#1 End to end FEC
#2 Segmented FEC
#3 Mix of #1/2
#4 Concatenated

Is the modulation consistent across the link?

Page 21

From: https://www.ieee802.org/3/B400G/public/21_1028/B400G_overview_c_211028.pdf