

# **CFP2 / CFP4 connector SI capability for 400Gb/s Ethernet**

Rev B: Added page 19

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400Gb/s Ethernet Study Group

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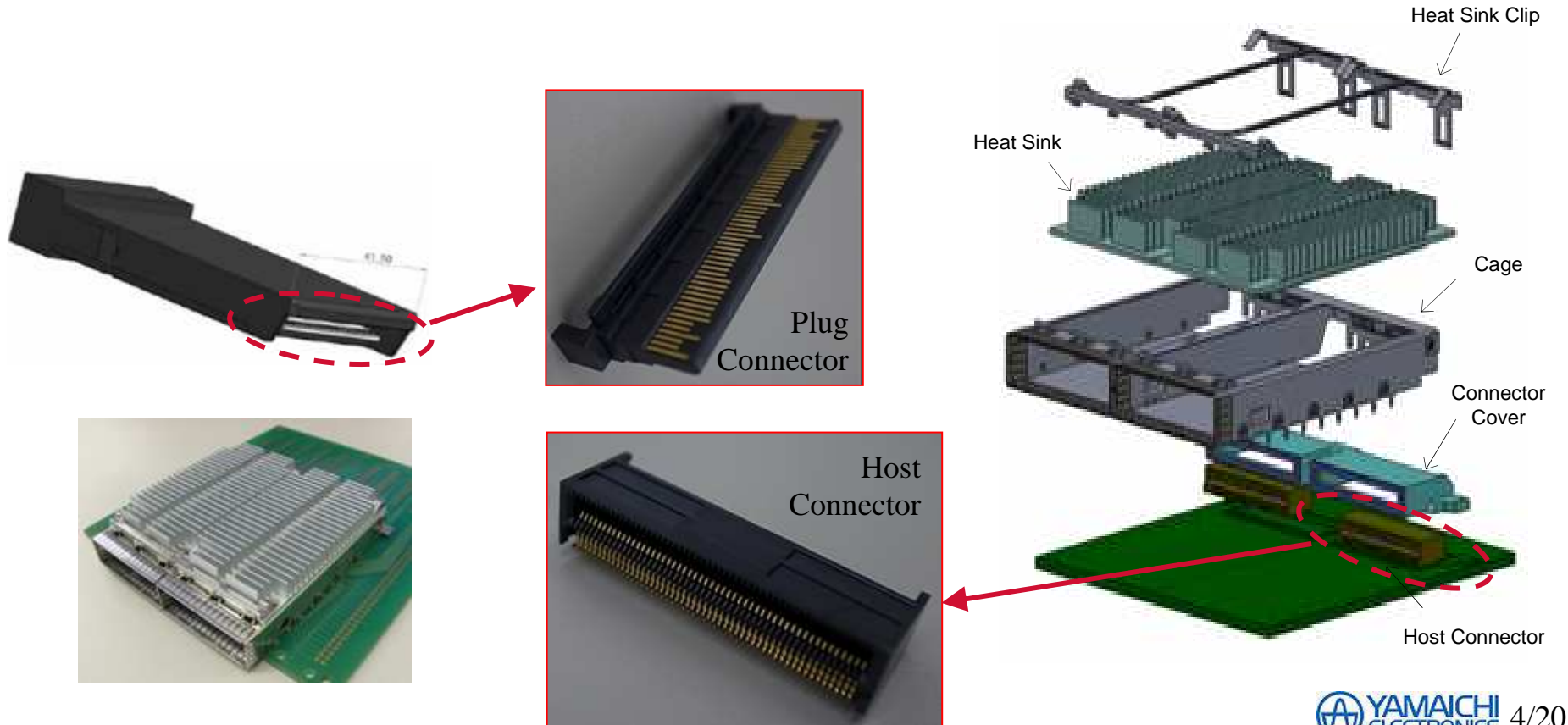
# Introduction

This presentation attempts to show feasibility of the CFP2/CFP4 connector usage at 400Gb/s Ethernet on “25Gbps x 16ch” and “50Gbps x 8ch” interface condition

# CFP2/CFP4 Connector Overview

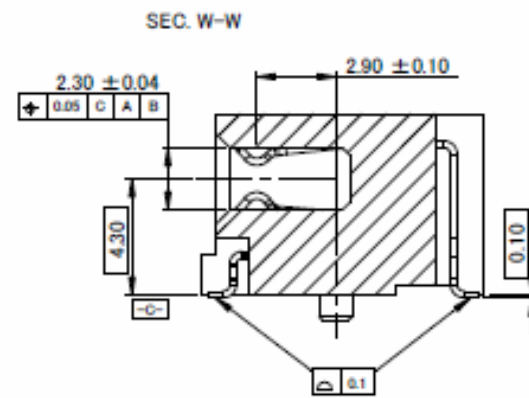
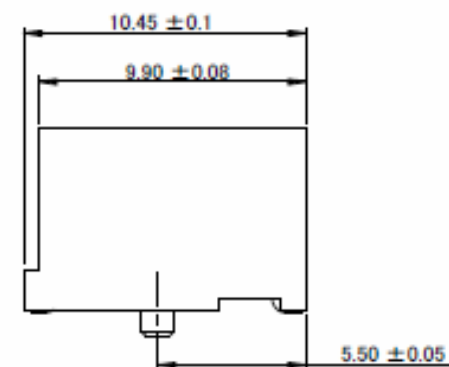
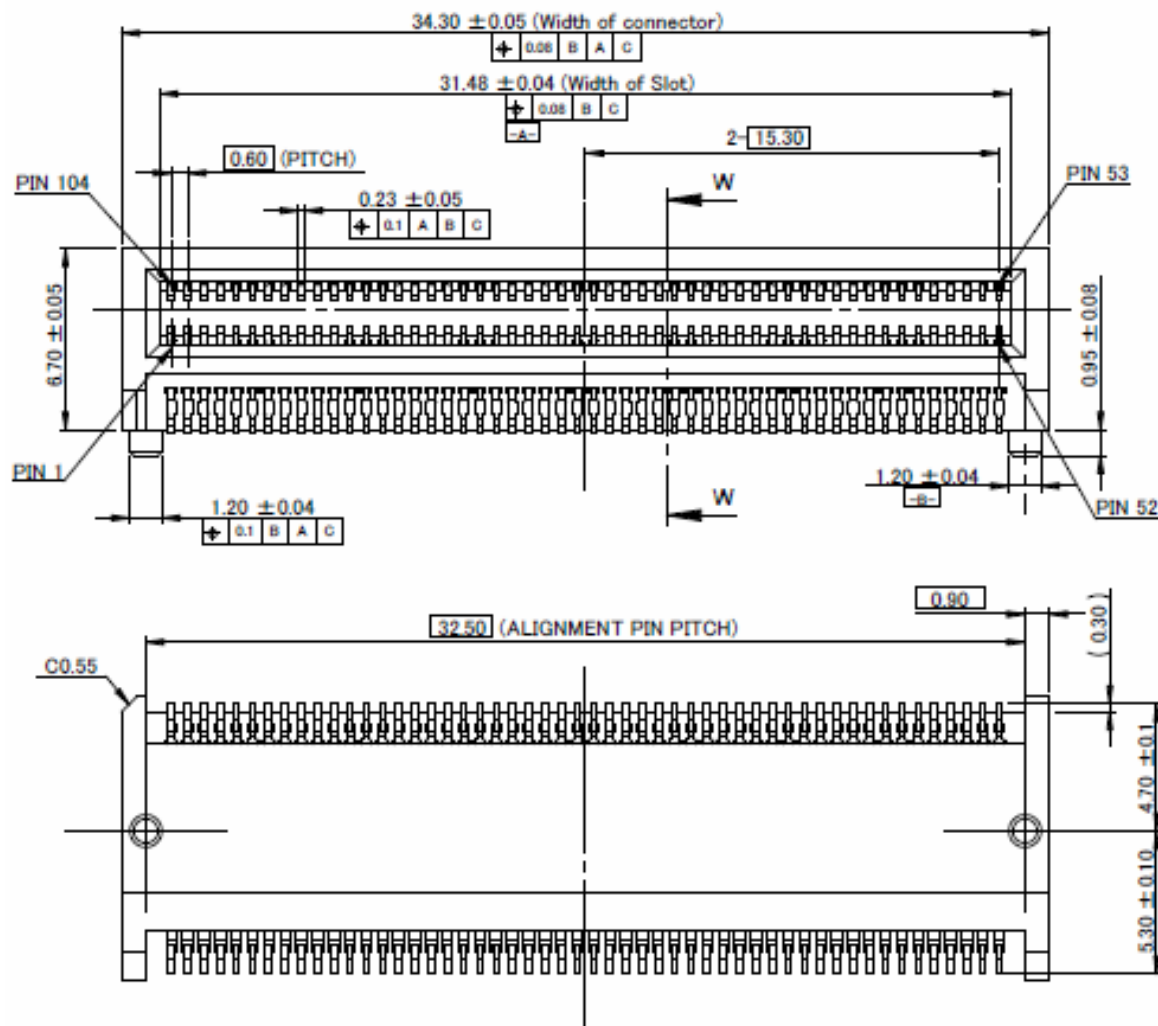
# CFP2/CFP4 Connector Overview

- Standardized by CFP MSA
- 0.6mm contact pitch, two piece plug and receptacle connector design
- Host connector uses all same contacts within each top row and bottom row
- Sequential mating controlled by plug connector contact length
- CFP2 and CFP4 connector use common contact parts for both plug and receptacle
- CFP2 connector is available in mass-production



# Host Connector

- CFP2 Host Connector Dimensions Specified in CFP MSA spec.



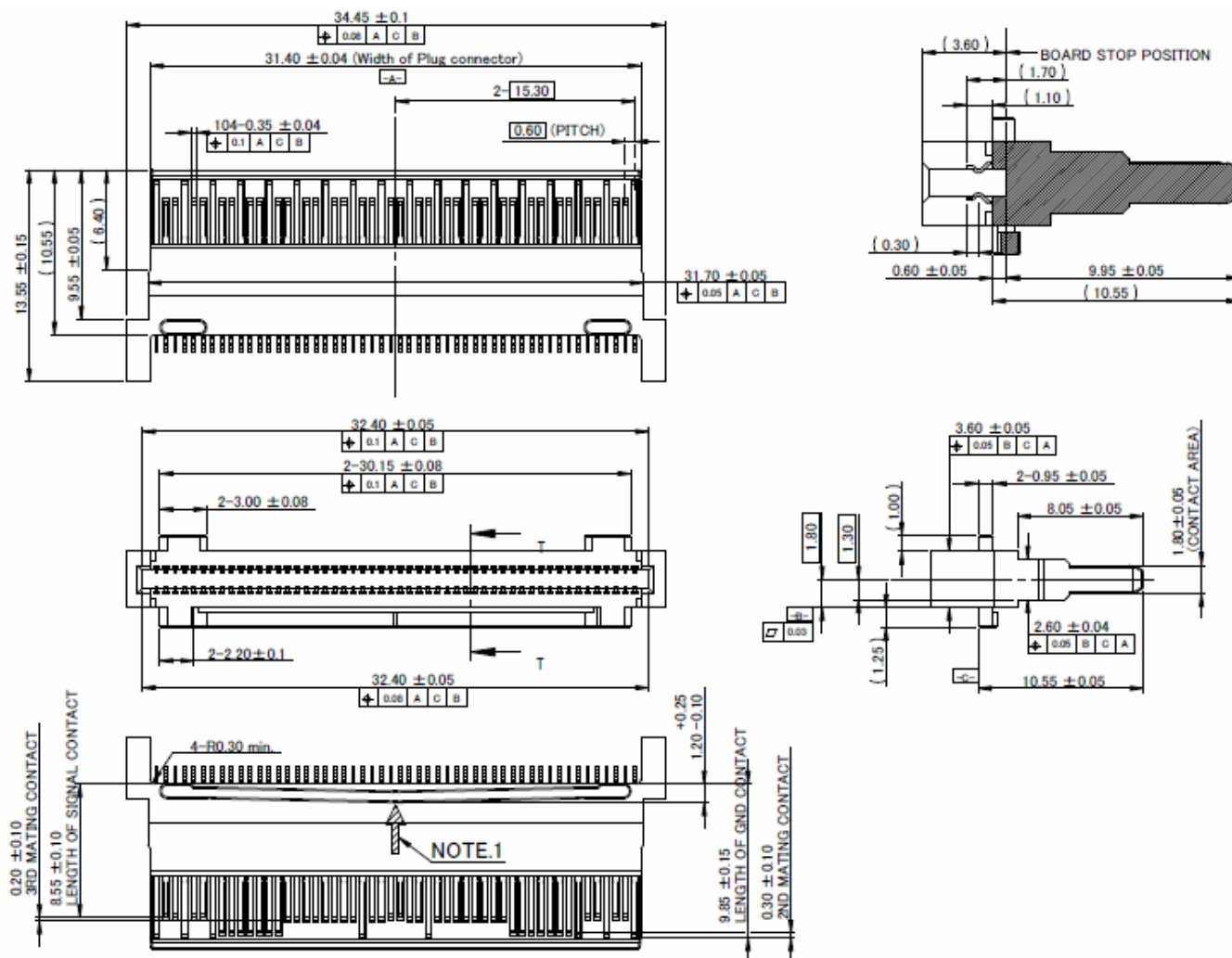
16 dif-pair (8Tx + 8Rx)  
on top row

CFP2 Pin Assignment (Example)

CFP2 Top		CFP2 Bottom	
104	GND	1	GND
103	(TX5n)	2	(TX_MCLKn)
102	(TX5p)	3	(TX_MCLKp)
101	GND	4	GND
100	(TX4n)	5	N.C.
99	(TX4p)	6	N.C.
98	GND	7	3.3V_GND
97	TX3n	8	3.3V_GND
96	TX3p	9	3.3V
95	GND	10	3.3V
94	TX2n	11	3.3V
93	TX2p	12	3.3V
92	GND	13	3.3V_GND
91	TX1n	14	3.3V_GND
90	TX1p	15	VMD_IO_A
89	GND	16	VMD_IO_B
88	TX0n	17	PRG_CTL1
87	TX0p	18	PRG_CTL2
86	GND	19	PRG_CTL3
85	N.C.	20	PRG_ALRM1
84	N.C.	21	PRG_ALRM2
83	GND	22	PRG_ALRM3
82	N.C.	23	GND
81	N.C.	24	TX_D1S
80	GND	25	RX_LOS
79	(REFCLKn)	26	MOD_LOPWR
78	(REFCLKp)	27	MOD_ABS
77	GND	28	MOD_RSTn
76	(RX5n)	29	GLB_ALRMn
75	(RX5p)	30	GND
74	GND	31	MDC
73	(RX4n)	32	MDIO
72	(RX4p)	33	PRTADR0
71	GND	34	PRTADR1
70	RX3n	35	PRTADR2
69	RX3p	36	VMD_IO_C
68	GND	37	VMD_IO_D
67	RX2n	38	VMD_IO_E
66	RX2p	39	3.3V_GND
65	GND	40	3.3V_GND
64	RX1n	41	3.3V
63	RX1p	42	3.3V
62	GND	43	3.3V
61	RX0n	44	3.3V
60	RX0p	45	3.3V_GND
59	GND	46	3.3V_GND
58	N.C.	47	N.C.
57	N.C.	48	N.C.
56	GND	49	GND
55	N.C.	50	(RX_MCLKn)
54	N.C.	51	(RX_MCLKp)
53	GND	52	GND

# Plug Connector

- CFP2 Plug Connector Dimensions Specified in CFP MSA spec.

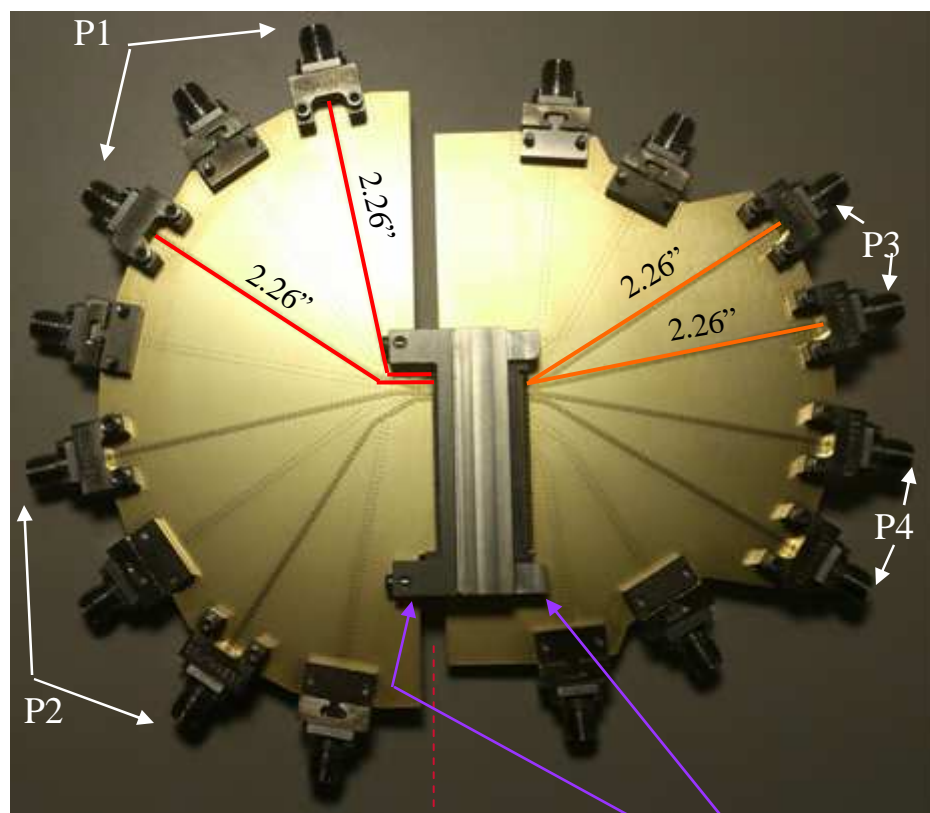


# CFP2 Connector SI Measurement Data

# CFP2 Connector SI Performance Measurement Condition

Measuring S-parameter data on  
“Mated Connector Test Board” and “Reference Board”

Mated Connector Test Board

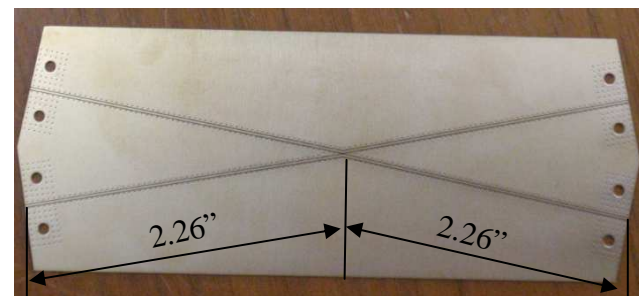


Module side

Host side

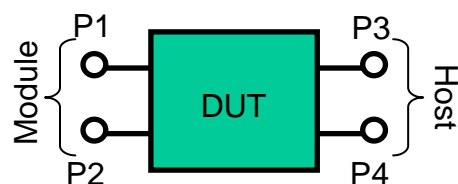
Connector engagement fixture

Reference Board

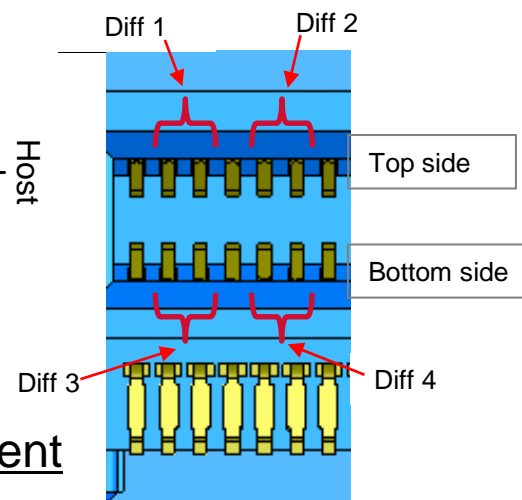


(Same trace length with the connector test boards)

Port Setup



Host Connector



Measuring Instrument

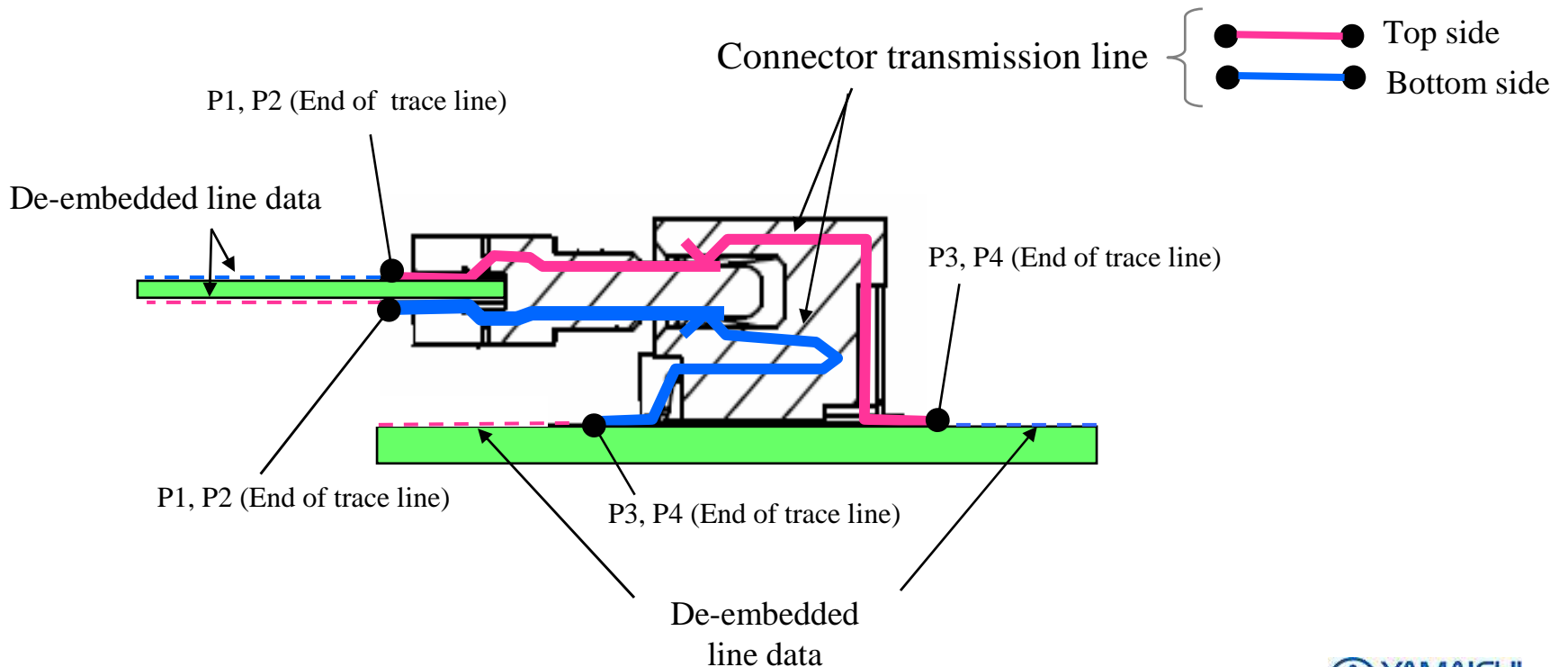
VNA : Agilent N5230A



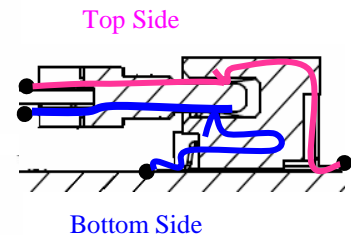
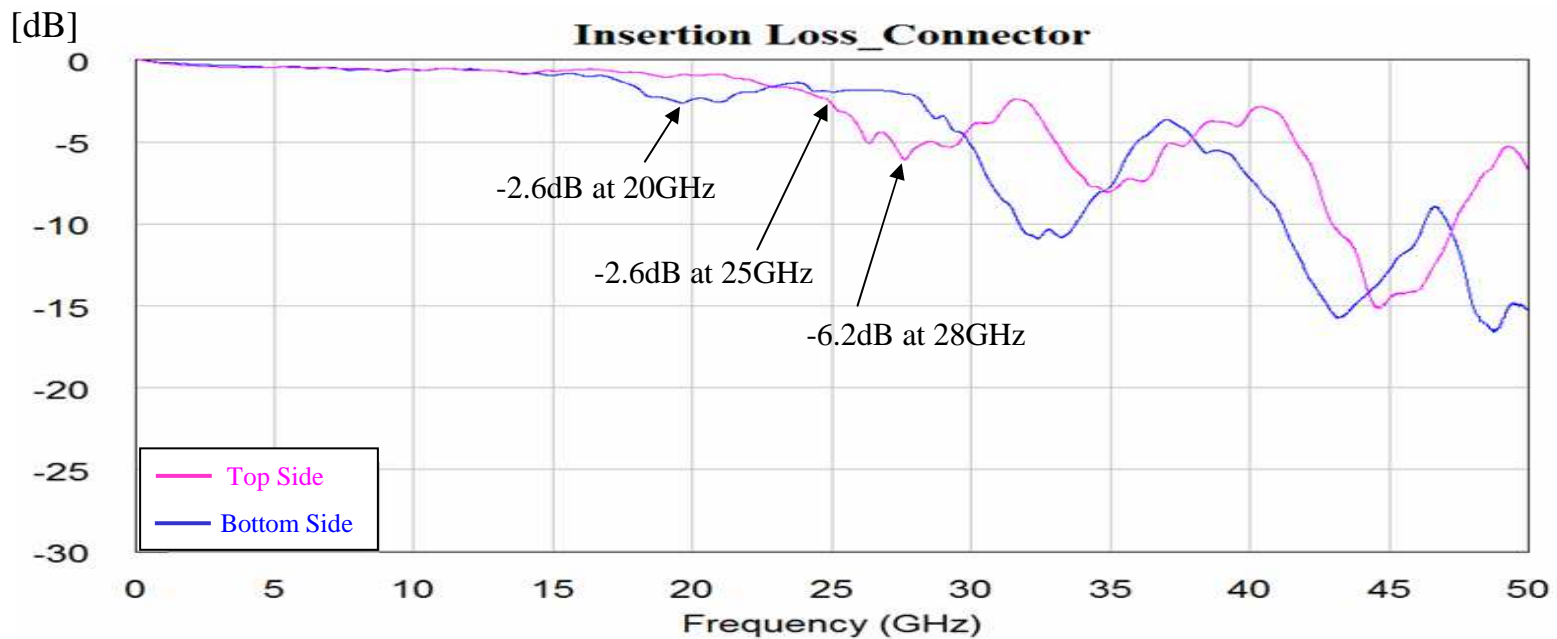
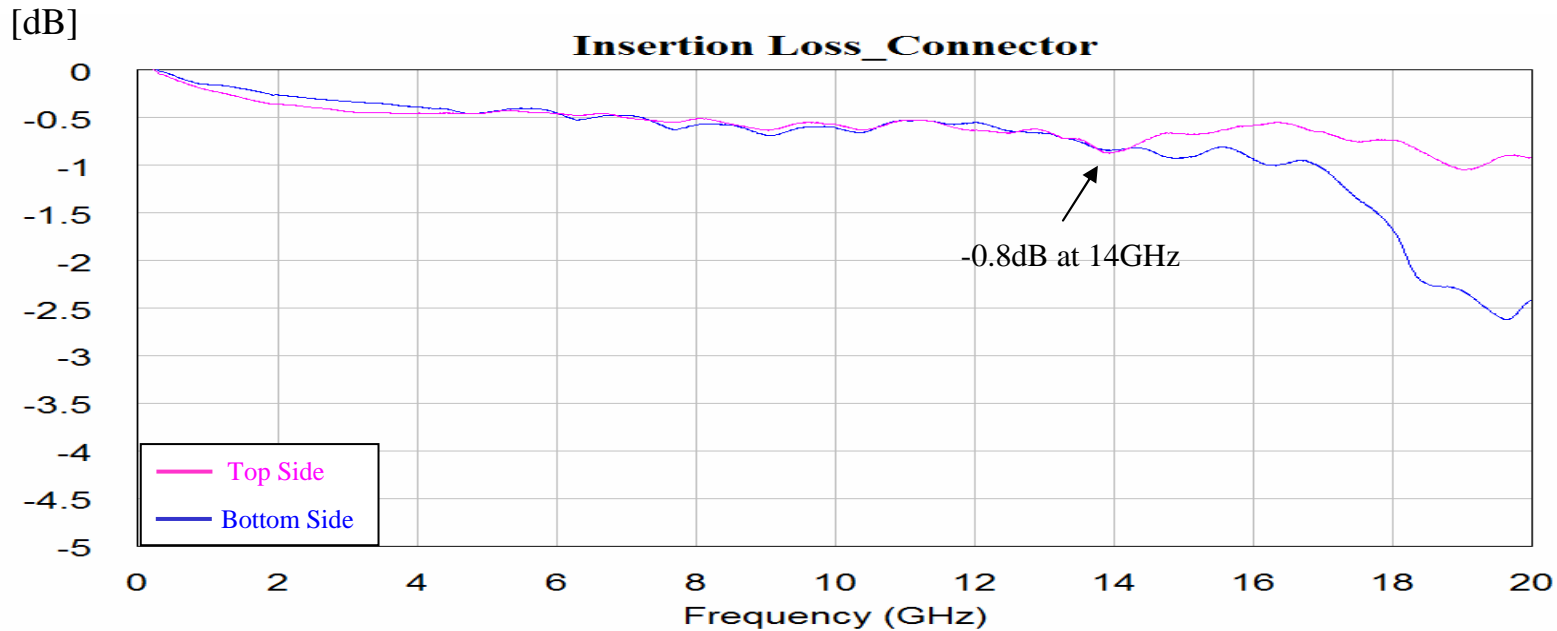
# CFP2 Connector SI Performance Measurement Condition

Using the data measured from “Reference Board” de-embed the trace line data then extract transmission performance of connector region (using Agilent N5230A)

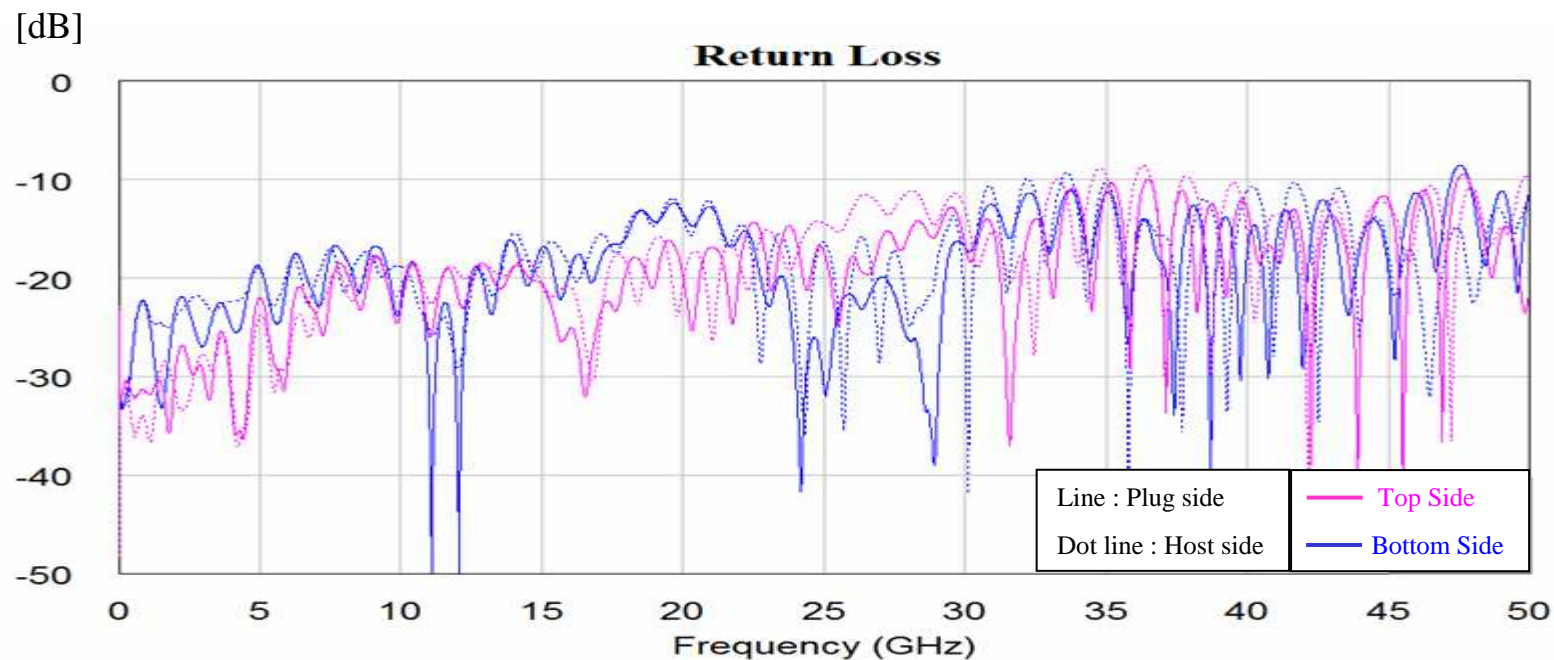
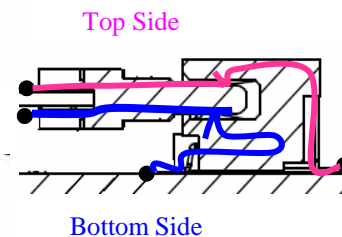
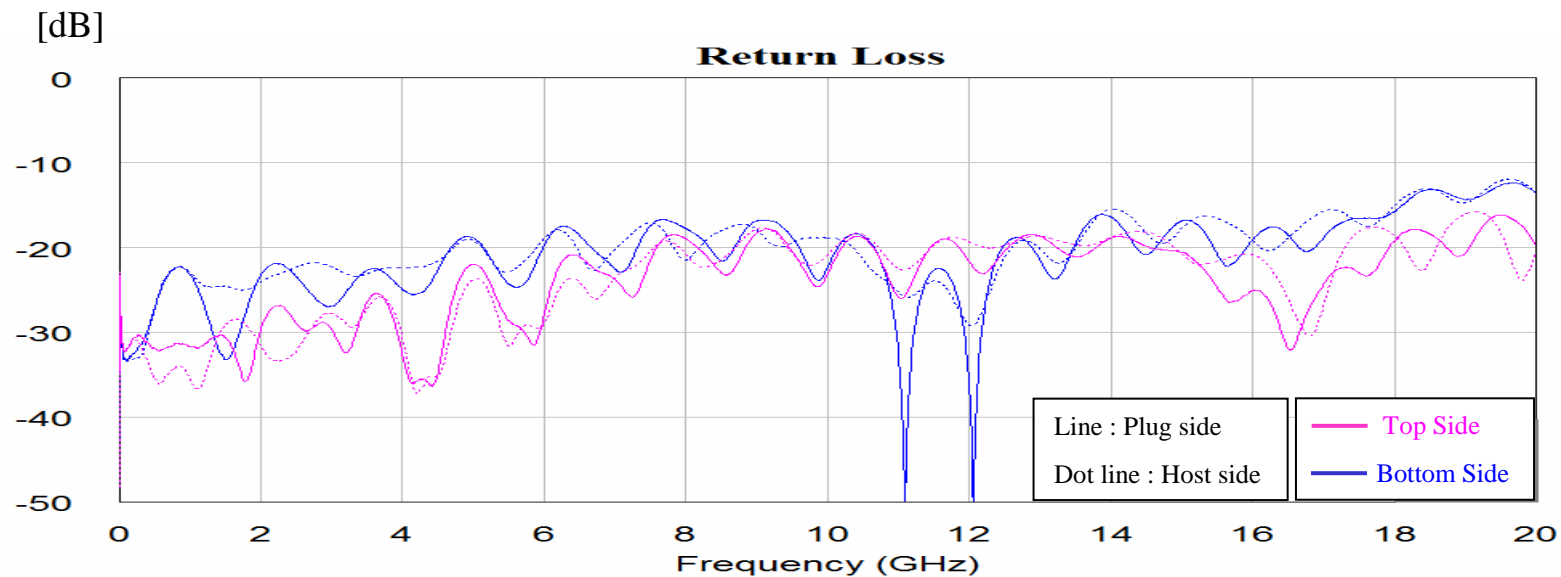
## Extracted Connector Transmission Region



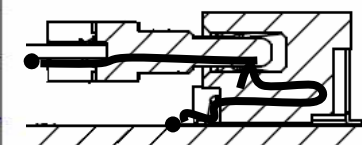
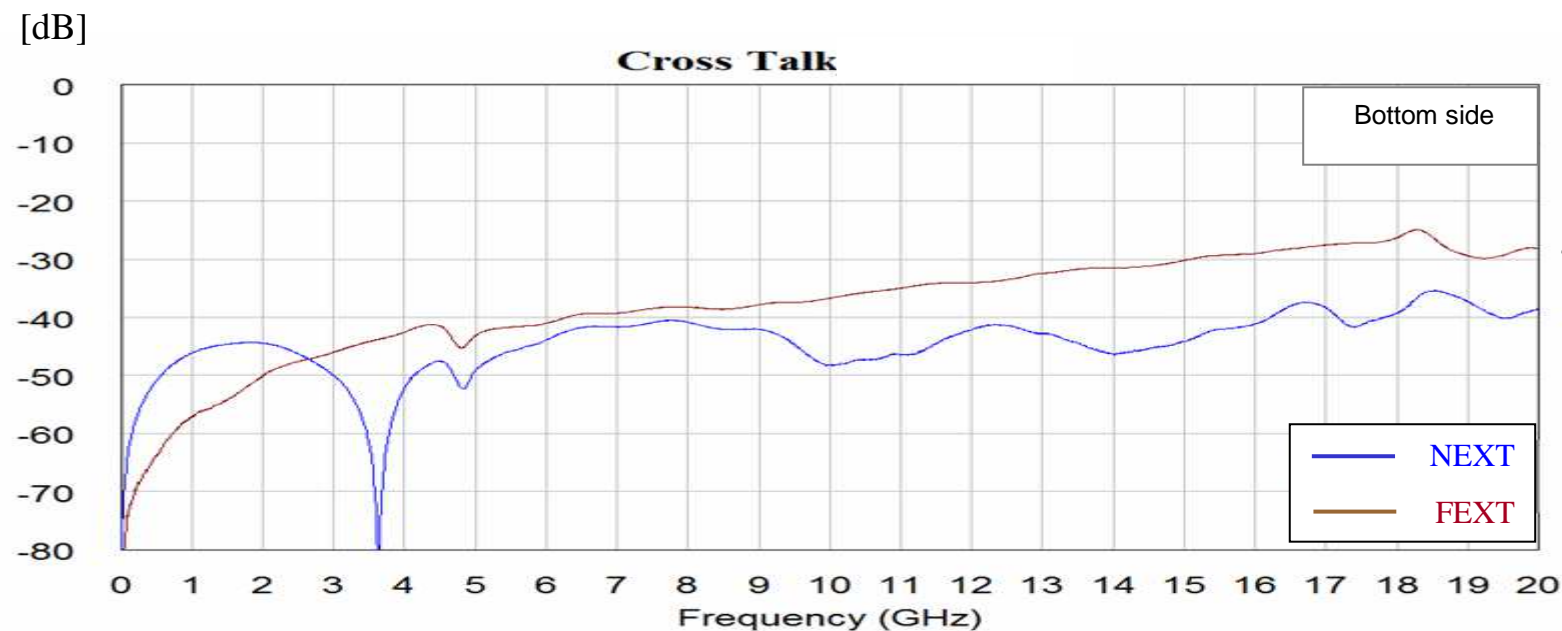
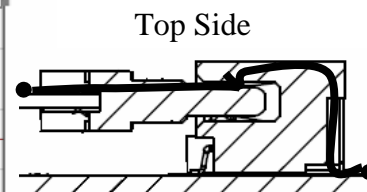
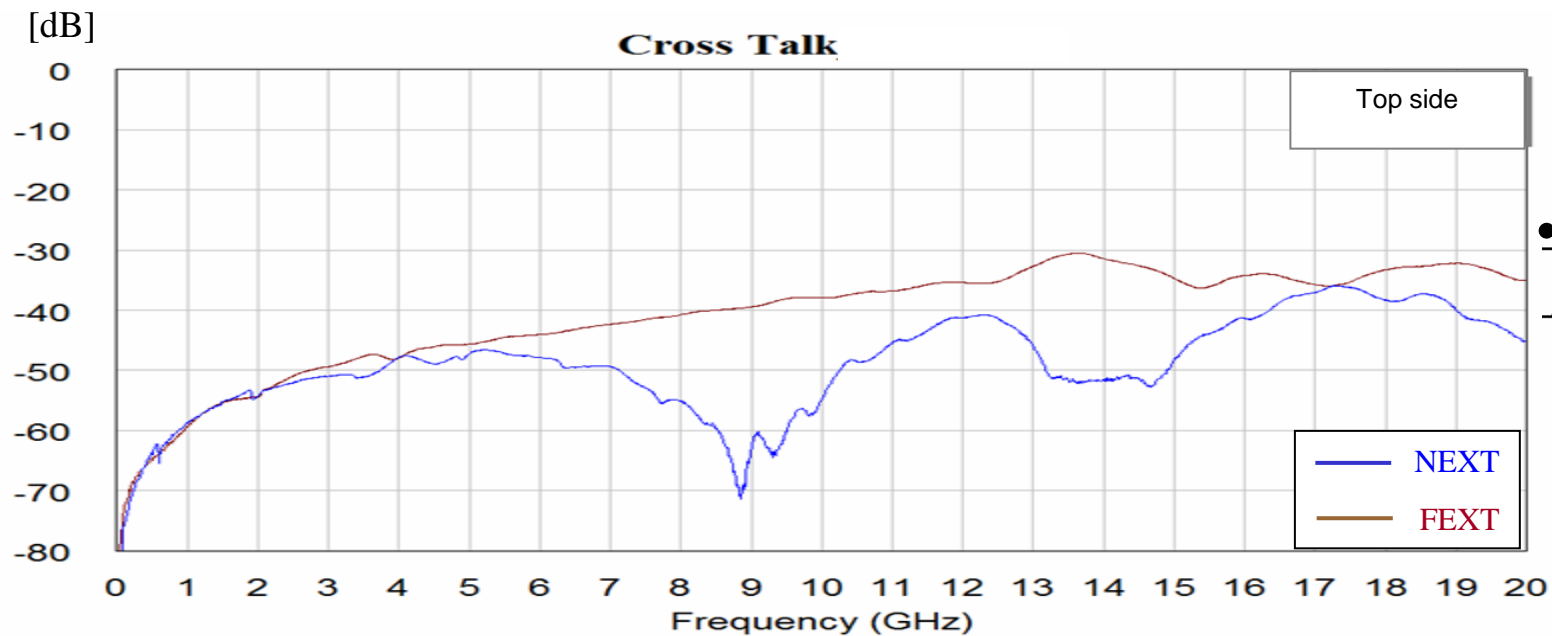
# Differential Insertion Loss(Sdd21)



# Differential Return Loss(Sdd11/Sdd22)



# Differential Cross talk



# **Channel Simulation Using Actual Connector Measurement Data**

# Channel Model

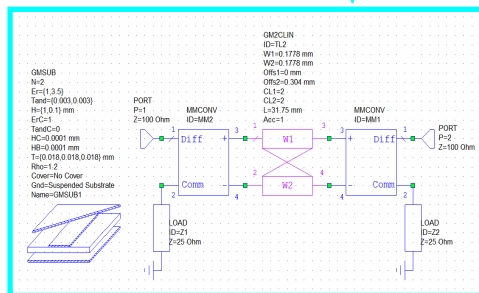
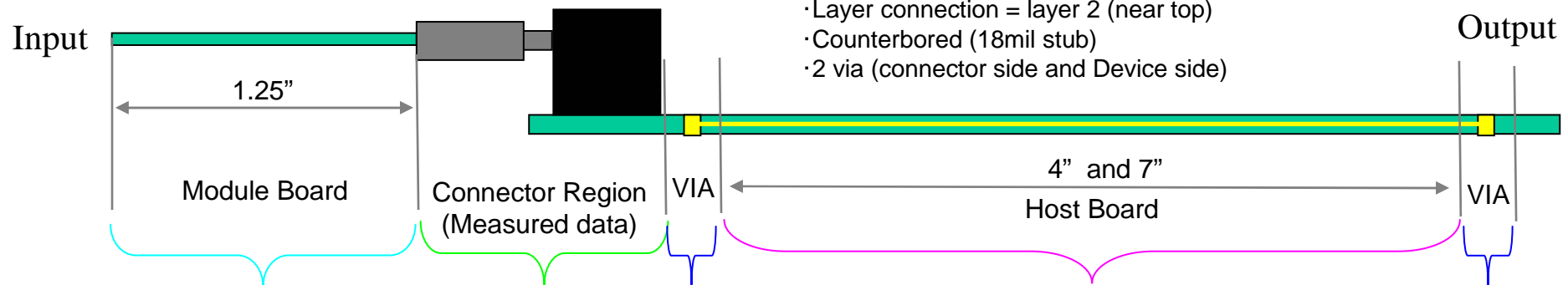
- Connector region = Import CFP2 actual measurement data
- Module board and host board = Use simulation file
- Simulate channel S-parameter of 2 diff-pairs each on top and bottom row

## Module Board

- Board material = Megtoron6 ( $\epsilon = 3.5, \tan \delta = 0.002$ )
- Trace length = 1.25"
- Trace geometry = microstrip
- Trace width = 7 mils
- Differential trace spacing = 5 mils
- No via required on module PCB

## Host Board

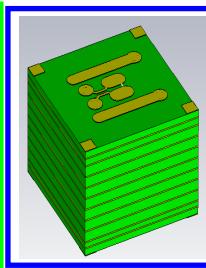
- Board material = Megtoron6 ( $\epsilon = 3.5, \tan \delta = 0.002$ )
- Trace length = 4" and 7"
- Trace geometry = stripline
- Trace width = 5 mils
- Differential trace spacing = 6 mils
- 2 signal layers
- Layer connection = layer 2 (near top)
- Counterbored (18mil stub)
- 2 via (connector side and Device side)



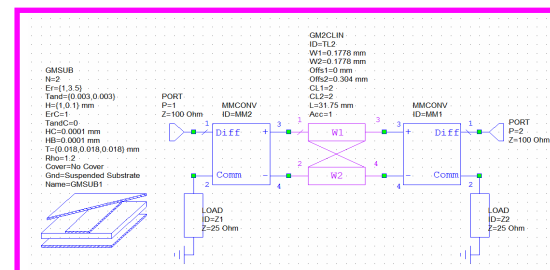
Circuit simulator element

```
Agilent Technologies,MS245A,MY49151186,A.09.20.08
Agilent MS245A: A.09.20.08
Date: Thursday, March 21, 2013 18:29:40
Correction: S11(Full 4 Port (1,2,3,4))
S12 (Full 4 Port (1,2,3,4))
S13 (Full 4 Port (1,2,3,4))
S14 (Full 4 Port (1,2,3,4))
S21 (Full 4 Port (1,2,3,4))
S22 (Full 4 Port (1,2,3,4))
S23 (Full 4 Port (1,2,3,4))
S24 (Full 4 Port (1,2,3,4))
S31 (Full 4 Port (1,2,3,4))
S32 (Full 4 Port (1,2,3,4))
S33 (Full 4 Port (1,2,3,4))
S34 (Full 4 Port (1,2,3,4))
S41 (Full 4 Port (1,2,3,4))
S42 (Full 4 Port (1,2,3,4))
S43 (Full 4 Port (1,2,3,4))
S44 (Full 4 Port (1,2,3,4))
S4P File: Measurements: <S11,S12,S13,S14>,
<S21,S22,S23,S24>,
<S31,S32,S33,S34>,
<S41,S42,S43,S44>:
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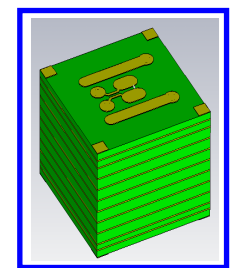
Touchstone file from actual measured data



3D model simulation

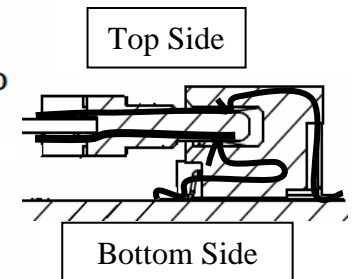
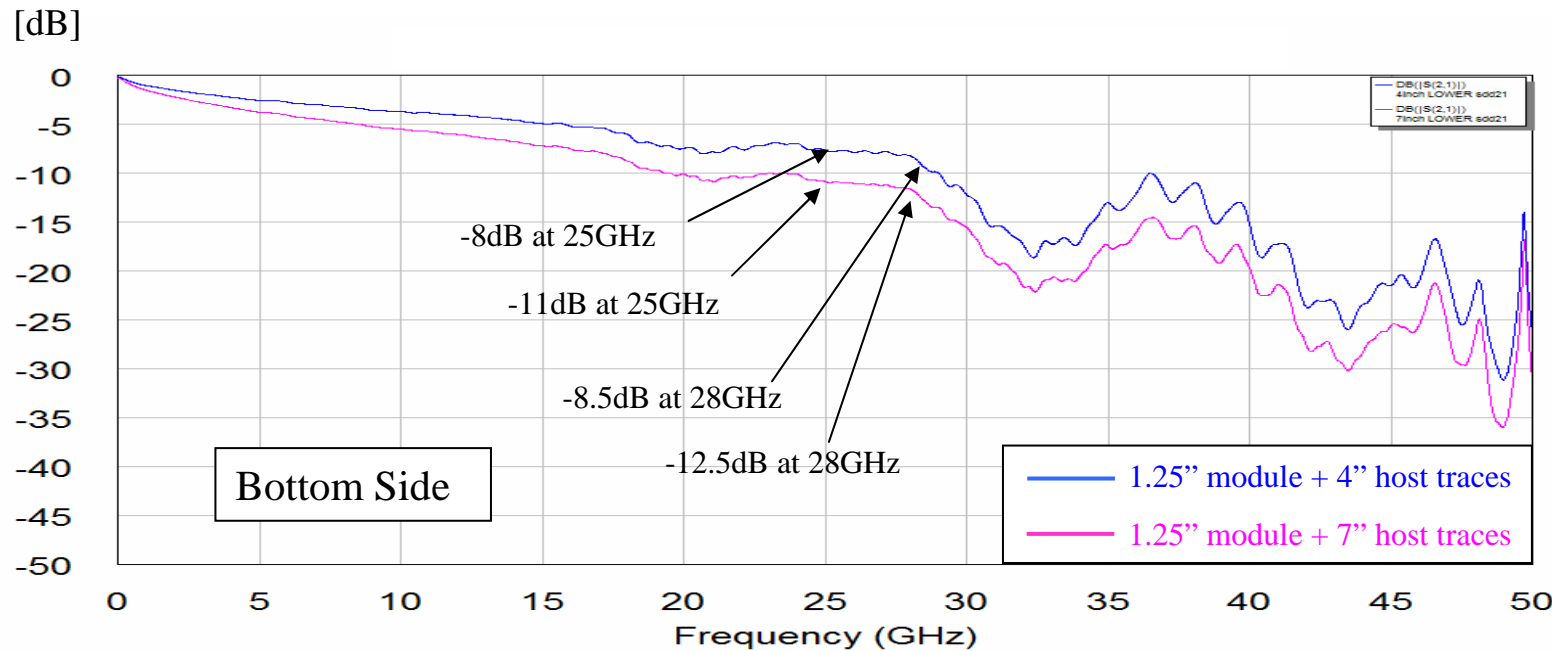
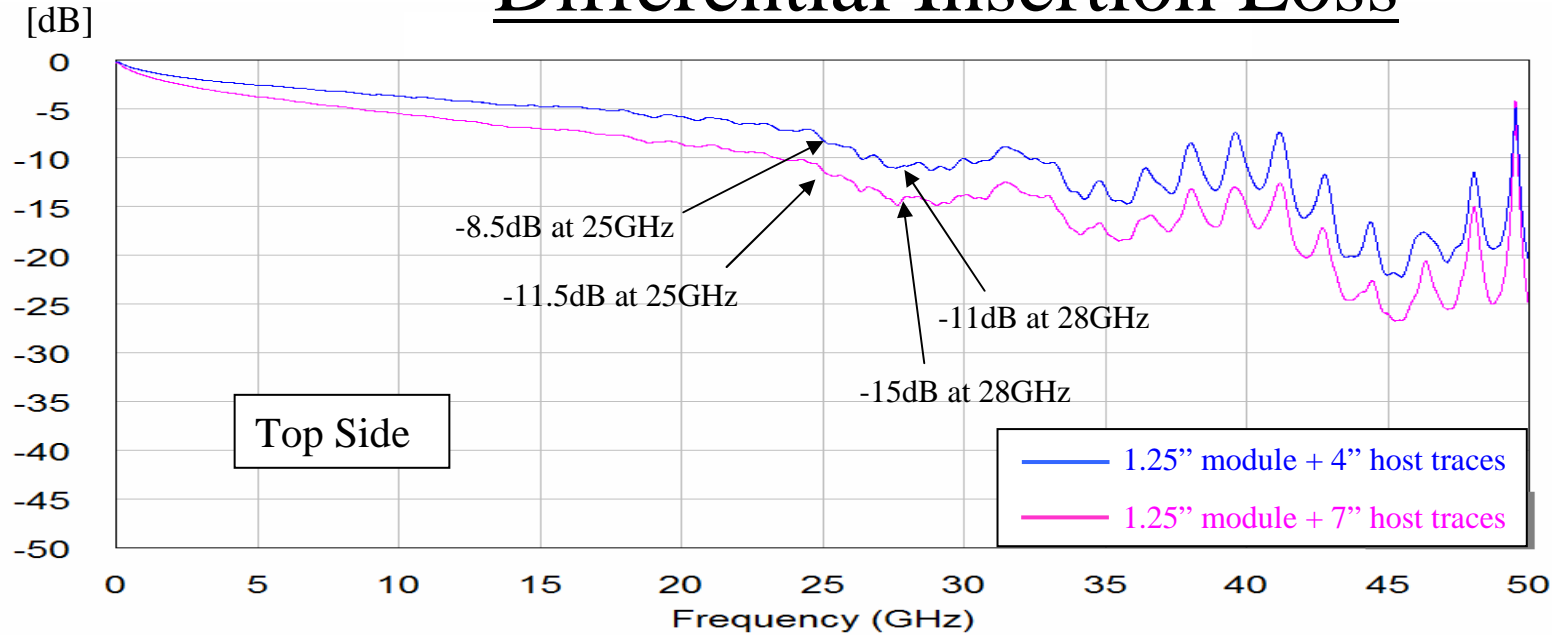


Circuit simulator element

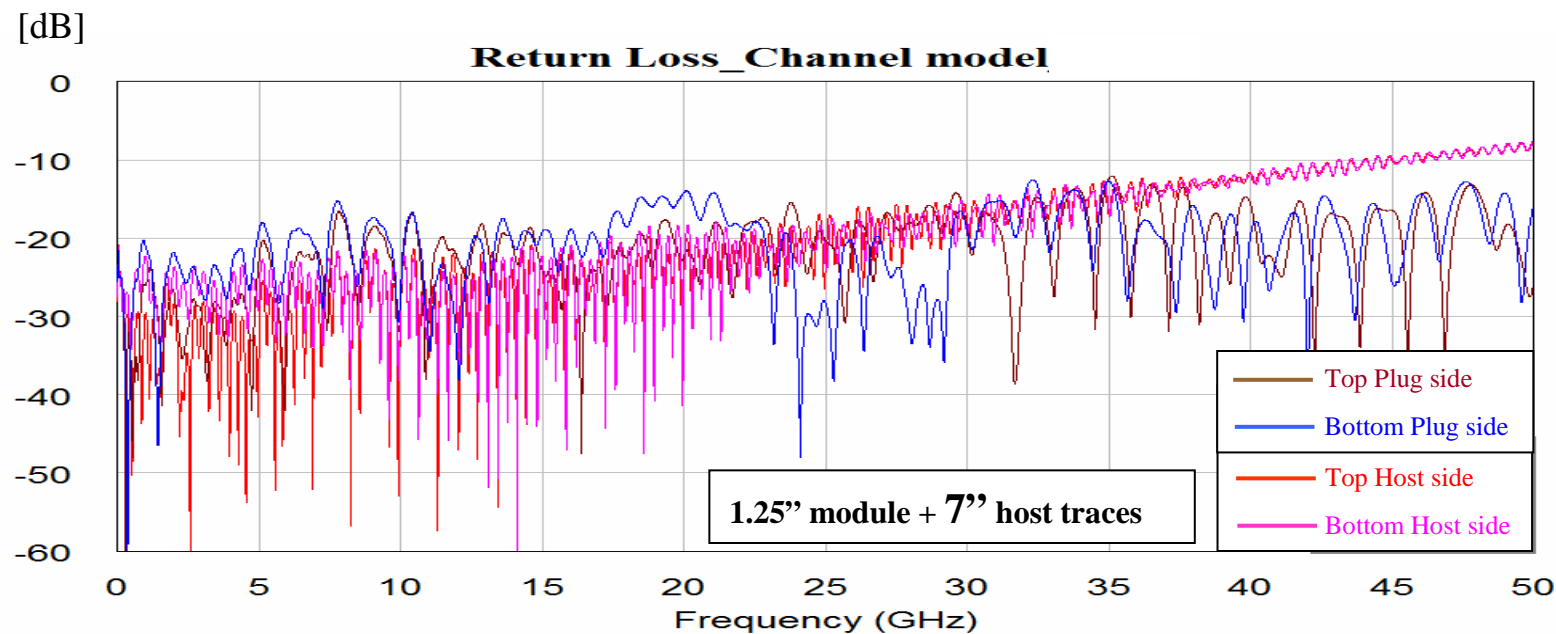
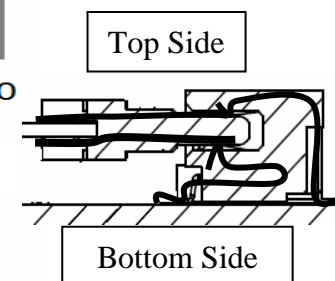
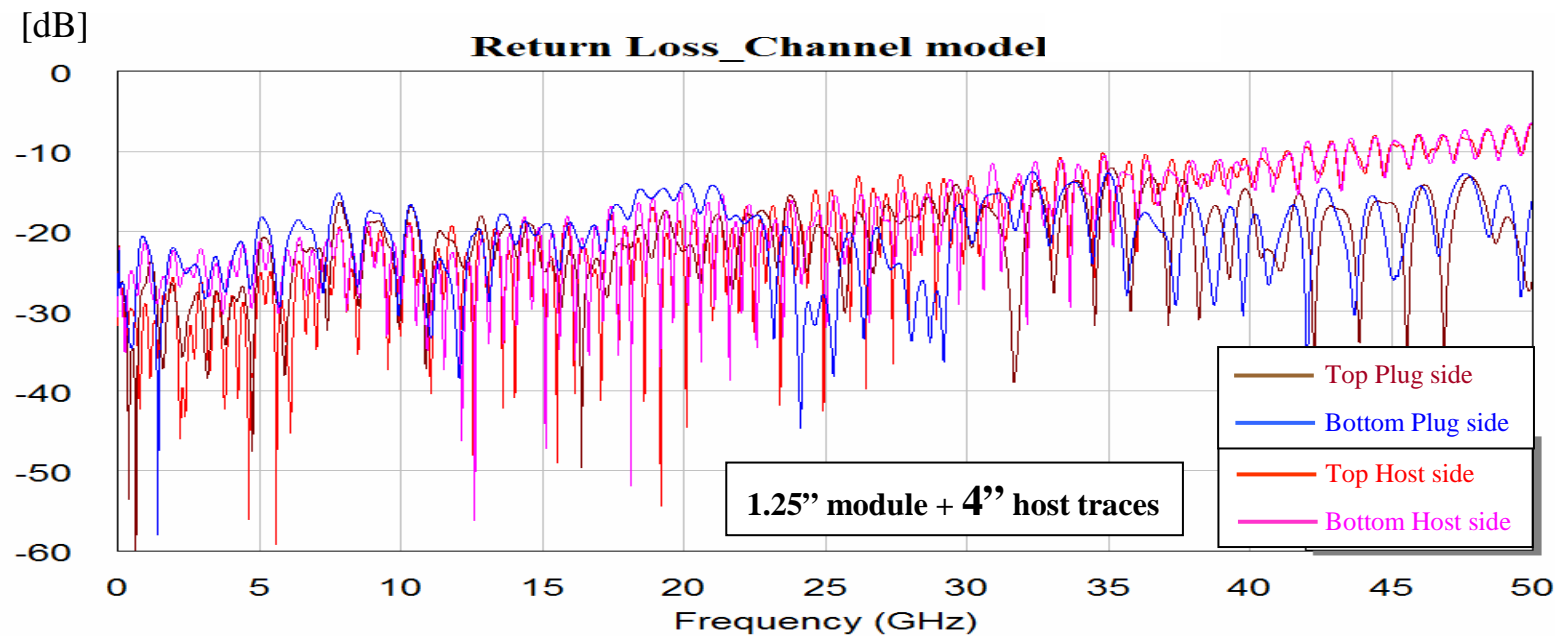


3D model simulation

# Differential Insertion Loss

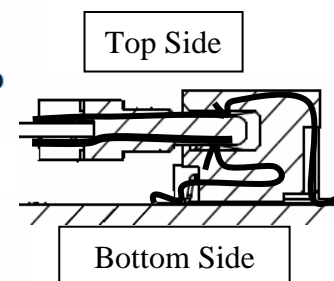
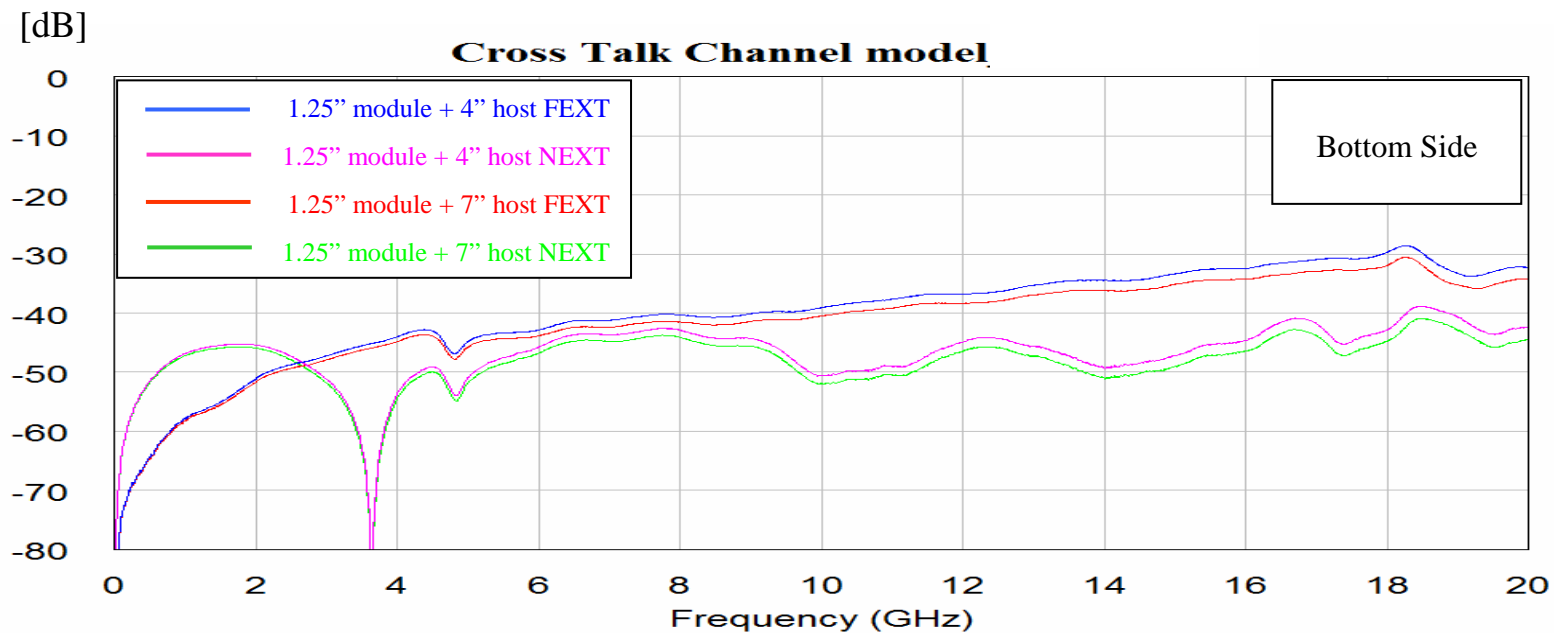
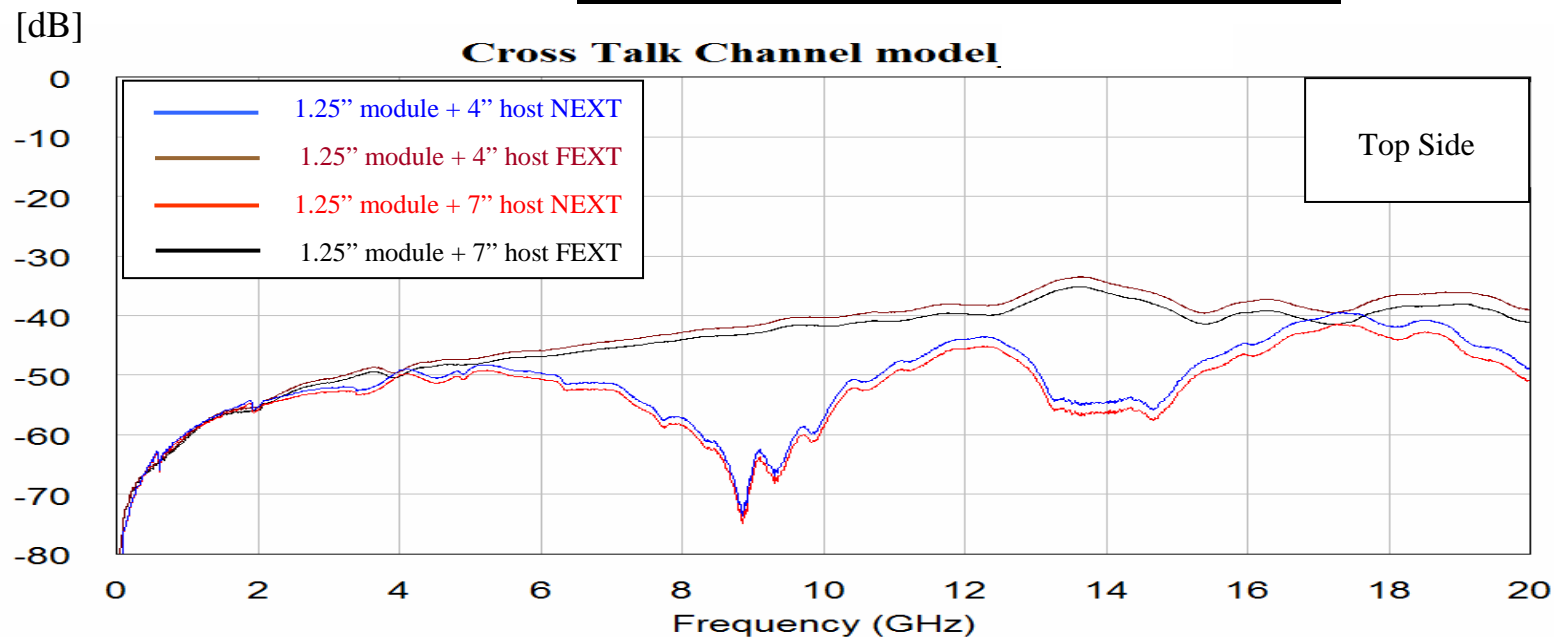


# Differential Return Loss





# Differential Cross talk



# Summary

- Existing CFP2 connector capable to handle 28Gbps signal and potentially capable for 56Gbps signal as well.
- Yamaichi CFP2 connector have almost same signal integrity performance on both top row and bottom row contacts, which allows allocating high speed channels to both top and bottom row contacts.
- 0.6 mm contact pitch is providing size benefit on CFP2/CFP4 module. This is also of benefit at the 25G x 16ch condition.

**Based on the conclusion above, CFP2 connector is suitable solution at high density “25G x 16ch” interface, and potentially feasible at “50G x 8ch” interface which being explored.**

(Yamaichi is working for further performance enhancement for 56Gbps x 8ch usage)

## CFP4 x 4 : 25G x 4ch x 4

Module Width : 21.5mm x 4 = 86.0mm

Top	Bottom
56 GND	1 3.3V GND
55 TX3n	2 3.3V GND
54 TX3p	3 3.3V
53 GND	4 3.3V
52 TX2n	5 3.3V
51 TX2p	6 3.3V
50 GND	7 3.3V GND
49 TX1n	8 3.3V GND
48 TX1p	9 VND IO A
47 GND	10 VND IO B
46 TX0n	11 TX DIS
45 TX0p	12 RX LOS
44 GND	13 GLB ALRMn
43 (REFCLKn)	14 MOD LOPWR
42 (REFCLKp)	15 MOD ABS
41 GND	16 MOD RSTn
40 RX3n	17 MDC
39 RX3p	18 MDIO
38 GND	19 PRTADR0
37 RX2n	20 PRTADR1
36 RX2p	21 PRTADR2
35 GND	22 VND IO C
34 RX1n	23 VND IO D
33 RX1p	24 VND IO E
32 GND	25 GND
31 RX0n	26 (MCLKn)
30 RX0p	27 (MCLKp)
29 GND	28 GND

## 140pin CFP2 (CDFP) : 25G x 16ch

Module Width : 52.3mm

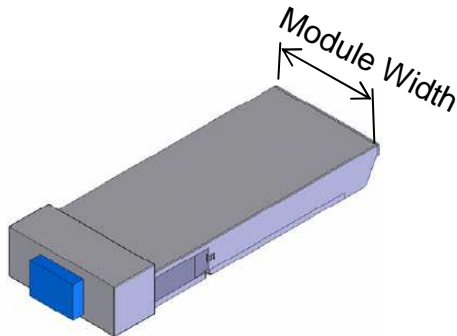
Top	Bottom
140 GND	1 GND
139 TX10n	2 TX15n
138 TX10p	3 TX15p
137 GND	4 GND
136 TX9n	5 TX14n
135 TX9p	6 TX14p
134 GND	7 GND
133 TX8n	8 TX13n
132 TX8p	9 TX13p
131 GND	10 GND
130 TX7n	11 TX12n
129 TX7p	12 TX12p
128 GND	13 GND
127 TX6n	14 TX11n
126 TX6p	15 TX11p
125 GND	16 GND
124 TX5n	17 3.3V GND
123 TX5p	18 3.3V
122 GND	19 3.3V
121 TX4n	20 3.3V
120 TX4p	21 3.3V
119 GND	22 3.3V GND
118 TX3n	23 3.3V GND
117 TX3p	24 VND IO A
116 GND	25 VND IO B
115 TX2n	26 PRG CNTL1
114 TX2p	27 PRG CNTL2
113 GND	28 PRG CNTL3
112 TX1n	29 PRG ALRM1
111 TX1p	30 PRG ALRM2
110 GND	31 PRG ALRM3
109 TX0n	32 GND
108 TX0p	33 TX DIS
107 GND	34 RX LOS
106 (REFCLKn)	35 MOD LOPWR
105 (REFCLKp)	36 MOD ABS
104 GND	37 MOD RSTn
103 RX10n	38 GLB ALRMn
102 RX10p	39 GND
101 GND	40 MDC
100 RX9n	41 MDIO
99 RX9p	42 PRTADR0
98 GND	43 PRTADR1
97 RX8n	44 PRTADR2
96 RX8p	45 VND IO C
95 GND	46 VND IO D
94 RX7n	47 VND IO E
93 RX7p	48 3.3V GND
92 GND	49 3.3V GND
91 RX6n	50 3.3V
90 RX6p	51 3.3V
89 GND	52 3.3V
88 RX5n	53 3.3V
87 RX5p	54 3.3V GND
86 GND	55 GND
85 RX4n	56 RX15n
84 RX4p	57 RX15p
83 GND	58 GND
82 RX3n	59 RX14n
81 RX3p	60 RX14p
80 GND	61 GND
79 RX2n	62 RX13n
78 RX2p	63 RX13p
77 GND	64 GND
76 RX1n	65 RX12n
75 RX1p	66 RX12p
74 GND	67 GND
73 RX0n	68 RX11n
72 RX0p	69 RX11p
71 GND	70 GND

## CFP2 : 50G x 8ch

Module Width : 41.5mm

Top	Bottom
104 GND	1 GND
103 TX7n	2 (TX_MCLKn)
102 TX7p	3 (TX_MCLKp)
101 GND	4 GND
100 TX6n	5 N.C.
99 TX6p	6 N.C.
98 GND	7 GND
97 TX5n	8 3.3V GND
96 TX5p	9 3.3V
95 GND	10 3.3V
94 TX4n	11 3.3V
93 TX4p	12 3.3V
92 GND	13 3.3V GND
91 TX3n	14 3.3V GND
90 TX3p	15 VND IO A
89 GND	16 VND IO B
88 TX2n	17 PRG CNTL1
87 TX2p	18 PRG CNTL2
86 GND	19 PRG CNTL3
85 TX1n	20 PRG ALRM1
84 TX1p	21 PRG ALRM2
83 GND	22 PRG ALRM3
82 TX0n	23 GND
81 TX0p	24 TX DIS
80 GND	25 RX LOS
79 (REFCLKn)	26 MOD LOPWR
78 (REFCLKp)	27 MOD ABS
77 GND	28 MOD RSTn
76 RX7n	29 GLB ALRMn
75 RX7p	30 GND
74 GND	31 MDC
73 RX6n	32 MDIO
72 RX6p	33 PRTADR0
71 GND	34 PRTADR1
70 RX5n	35 PRTADR2
69 RX5p	36 VND IO C
68 GND	37 VND IO D
67 RX4n	38 VND IO E
66 RX4p	39 3.3V GND
65 GND	40 3.3V GND
64 RX3n	41 3.3V
63 RX3p	42 3.3V
62 GND	43 3.3V
61 RX2p	44 3.3V
60 RX2n	45 3.3V GND
59 GND	46 GND
58 RX1p	47 N.C.
57 RX1n	48 N.C.
56 GND	49 GND
55 RX0p	50 (RX_MCLKn)
54 RX0n	51 (RX_MCLKp)
53 GND	52 GND

## Module Width Comparison



\*Pin assignments are example only

Thank You