

Considerations on Options for 400GE Optical Interfaces

Xiaolu Song, Peter Stassar, Li Zeng, Suping Zhai,
Xinyuan Wang, Wei Chen, Wenjun Zhou.

Huawei Technologies Co., Ltd.

May 2013

Supporters

- ▣ Pete Anslow, Ciena
- ▣ Keith Conroy, Multiphy
- ▣ Ali Ghiasi, Broadcom
- ▣ Wenbin Jiang, Cosemi
- ▣ Song Shang, Semtech
- ▣ Francois Tremblay, Semtech

Introduction

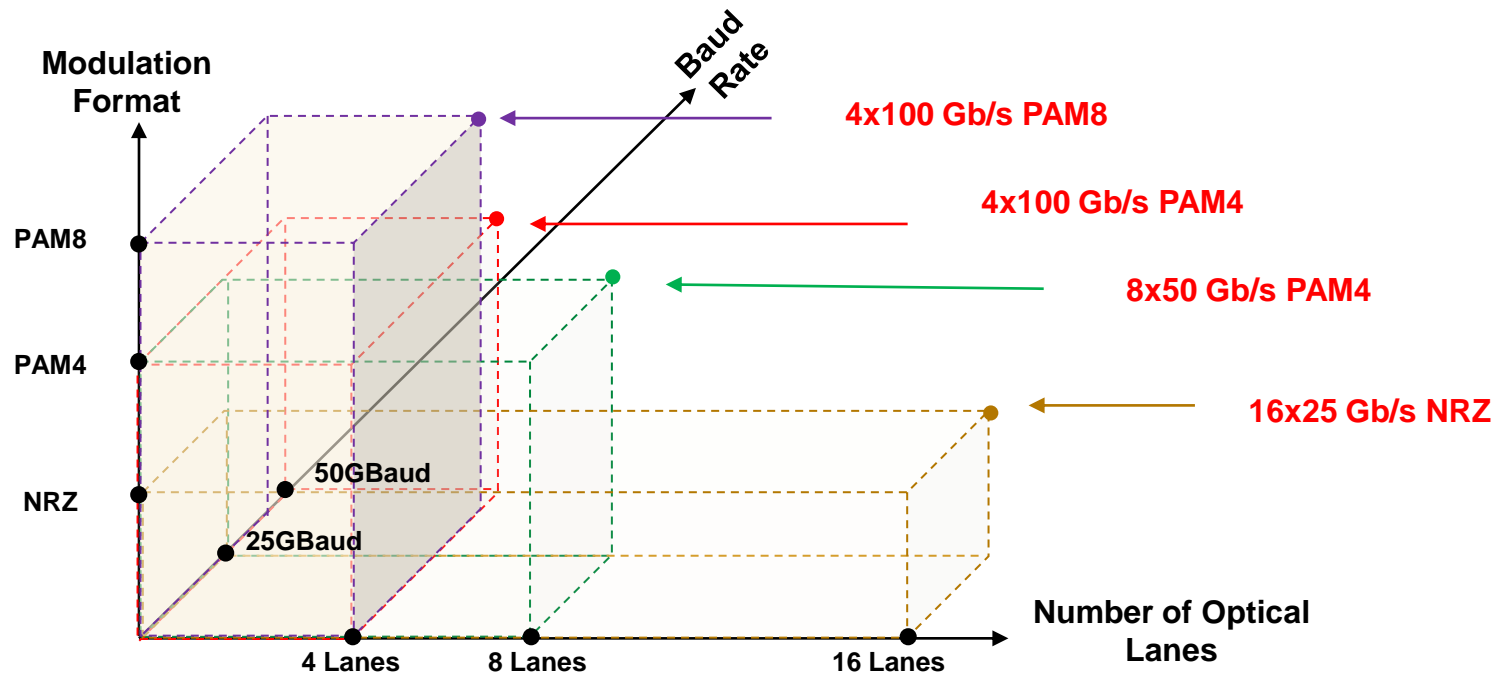
- ▣ This presentation provides some options for 400GE optical interfaces, taking into consideration:
 - ▣ Whether it makes sense to define only SMF interfaces for 400GbE or also MMF interfaces.
 - ▣ Ways to increase the data rate from 100 Gb/s to 400 Gb/s.
 - ▣ The experience from 100GbE projects, 802.3ba and 802.3bm.
 - ▣ Advantages and disadvantages for short versus medium / long term solutions.
- ▣ For 400GbE we will need a solution which provides the right balance between cost & power (enabling a lower cost per bit) and port density.

Options for 400GbE MMF optical interfaces

- ❑ If 100GBASE-SR4 will work at 100m reach w/ FEC over OM4, then the 400GBASE-SR16 will also work at 100m over OM4.
- ❑ But the contributors are of the opinion that it may be difficult to agree on a useful objective for 400GbE multimode fiber applications because it may require one (or a combination) of the following solutions:
 - ❑ Extending the total number of fibers per module from 2x4 to 2x16 which is 32 fibers per link which seems rather challenging.
 - ❑ The introduction of WDM solutions on multimode fiber, not “easy” for the 850nm window of operation.
 - ❑ Increase of the bit-rate per fiber, which will be difficult in view of the limited bandwidth of multimode fibers.

Options for 400GbE SMF optical interfaces

- To increase the data rate to 400 Gb/s, several ways could be chosen, starting from existing and proposed solutions for 100GbE:
 - Increase the number of fibers
 - increase the number of optical wavelengths
 - increase the bandwidth per fiber or per lane
 - increase the number of bits per symbol by introducing a PAM-n modulation format
 - Or a combination thereof



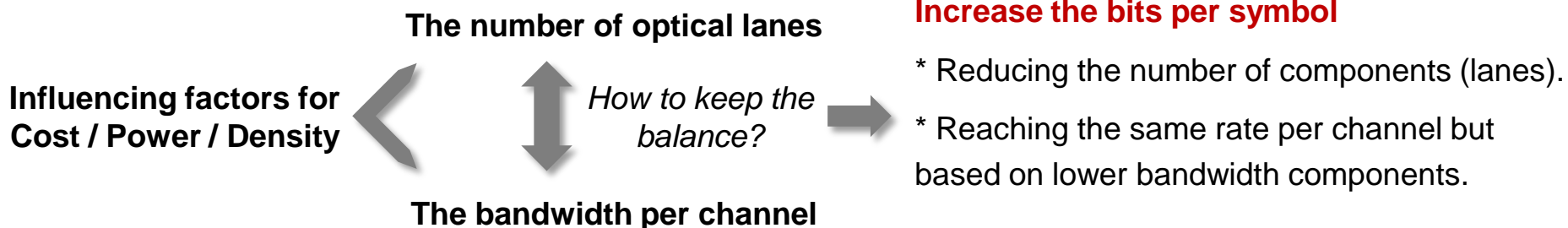
Cost / Power / Density: The Never Ending Balancing Acts

- For client side, multi-lane solutions are unavoidable, e.g. 16x25 Gb/s, 8x50 Gb/s and 4x100 Gb/s will achieve the 400GbE capacity.
- Not “can it be done” but “can it be done at right cost & power, and the right port density !”

The never ending balancing acts!



Source: CFI_01_0313.



- Optimizing the number of optical lanes is a key to achieve a higher port density and lower cost for client side applications in the future.

To Reduce the Number of Lanes New Technology is Needed

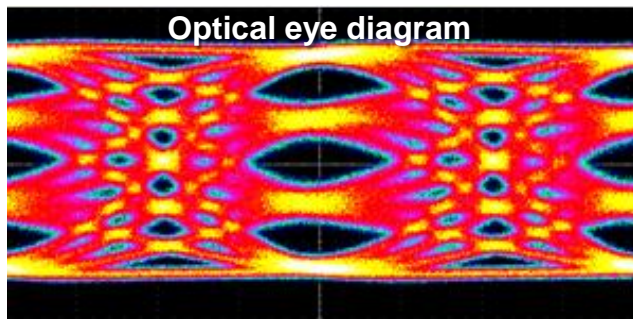
Modulation for bit rate	Symbol rate (Baud)	Bandwidth (Hz) (w/o overhead)
NRZ	R	$< R$
PAM4	$R/2$	$< R/2$
DSQ-32 (a PAM8 mapping)	$R/2.5$	$< R/2.5$
PAM8	$R/3$	$< R/3$

- ❑ In view of previous experience NRZ will not be practical at 100Gb/s per lane and therefore some level of advanced modulation technique is needed.
- ❑ For a 50Gb/s NRZ per lane architecture, the performance of optical components is still challenging. The link loss and the transmission penalty maybe an issue for electrical lanes.
- ❑ For a 25Gb/s per lane architecture we can reuse the E/O technology and leverage the high volume 100GbE market.
- ❑ The use of Advanced Modulation is a promising method to get the right balance between cost, power and density for different scenarios.

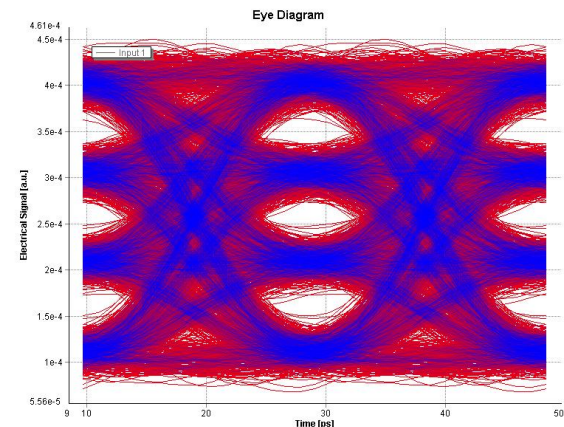
Advanced Modulation (e.g. PAM4)

- When using a PAM4 approach, possible PMDs are 8x50G PAM4 or 4x100G PAM4.
 - 8x50G PAM4: in this case the electrical and optical interfaces can remain at 25GBd, reusing similar components from 100GbE.
 - 4x100G PAM4: In this case high bandwidth optical components will be needed.
- E.g. the experimental result of 50Gb/s PAM4 & simulation result of 100Gb/s PAM4.

Measured PAM4 eye
(~20GHz EML)

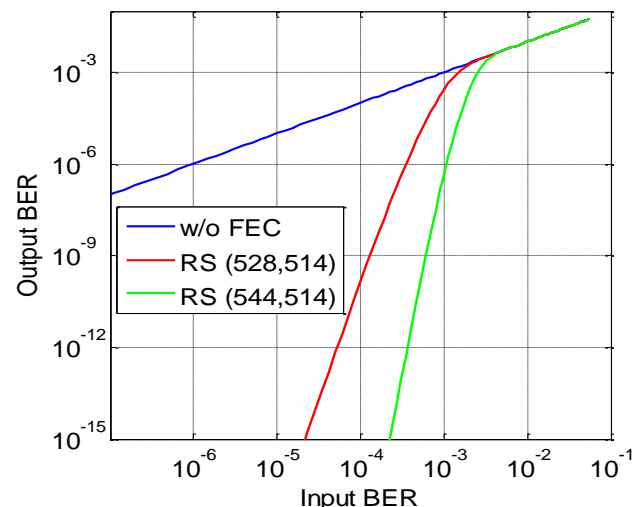
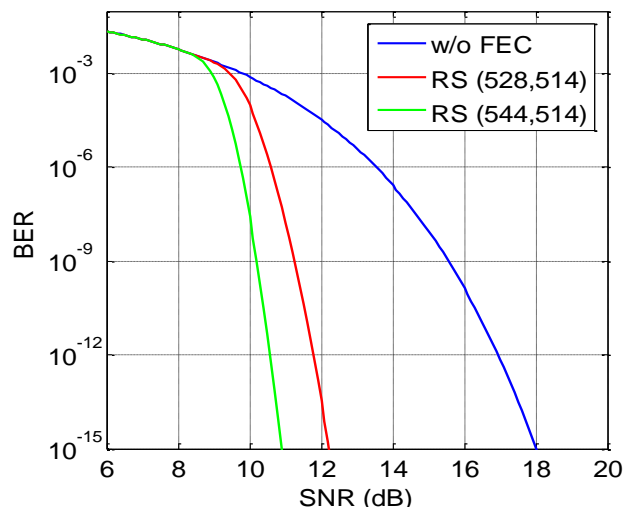


Simulated 100Gb/s PAM4
eye (~45GHz Modulator)

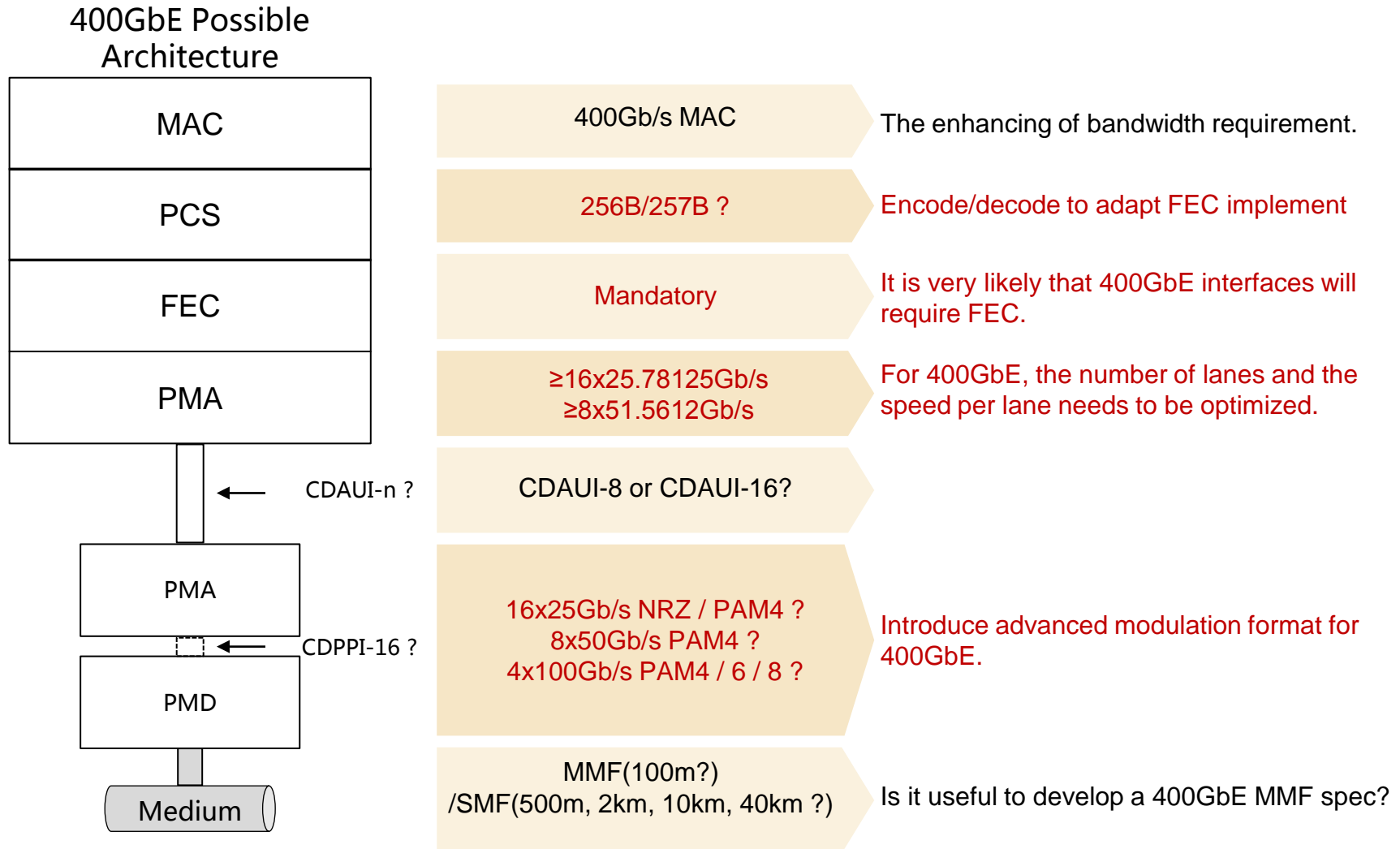


Thoughts on the use of FEC for 400GbE

- In order to achieve lowest cost and not too tight specifications for 400GbE it is probably unavoidable to use FEC.
- For instance P802.3bj uses RS(544,514) to form a 100GBASE-KP4 PHY.
- The emerging 100GBASE-SR4 will use FEC (for 100m).
- **To be addressed:**
 - Which kind of FEC (or new FEC code) may vary with the choice of PMD.
 - Depending on the different reach/rate/modulation electrical/optical interface requirements, different FEC solutions might be needed.
 - FEC schemes like RS, MLC, BCH et al with high NCG, low latency, and easy implementation in hardware will be candidates.



A Possible Architecture



Summary

- ❑ To enable quick time to market, mainstream 100GbE 25 Gb/s NRZ technology can be reused, by simply increasing the number of channels from 4 to 16. This however implies a low port density, high cost and power consumption compared with an approach based on fewer optical channels operating at a higher bit rate.
- ❑ Lower long term cost and a higher port density can be achieved by reducing the number optical lanes combined with the introduction of advanced modulation.
- ❑ We feel that high speed NRZ will not be economically feasible or practical on the short-medium term at rates of 50Gb/s or 100Gb/s per lane. It appears that reducing the number of optical lanes is only possible by introducing advanced modulation formats.
- ❑ Based upon today's experience and past discussions in P802.3bm we feel that an approach based upon 8 optical lanes, each operating at 50Gb/s PAM4 could be a very promising approach, but we do not want to exclude other, more complex optical modulation formats at a later stage.

Next Investigation Steps

❑ Advanced modulation

- ✓ Confirm the modulation code selection for different scenarios
- ✓ The link budget, EQ compensation, and the bandwidth tradeoffs
- ✓ The linearity of components
- ✓ The feasibility of encode and decode for Ethernet interconnection

❑ FEC

- ✓ High NCG and low latency FEC for advanced modulation
- ✓ Timing Error / Jitter ...

❑ Electrical interface

- ✓ CDAUI-n
- ✓ CDPPI-16 ...?

Thank you