400Gb/s PMD Road Map

400Gb/s Ethernet Study Group

IEEE 802.3 Interim

Victoria, BC, Canada

17 May 2013

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Outline

- Near-Term 400GbE PMD Observations
- Long-Term 400GbE PMD Observations
- 100GbE Configuration
- Gen1 400GbE Configuration
- Gen2 400GbE Configuration
- Gen3 400GbE Configuration
- Possible 400GbE Standardization Approach

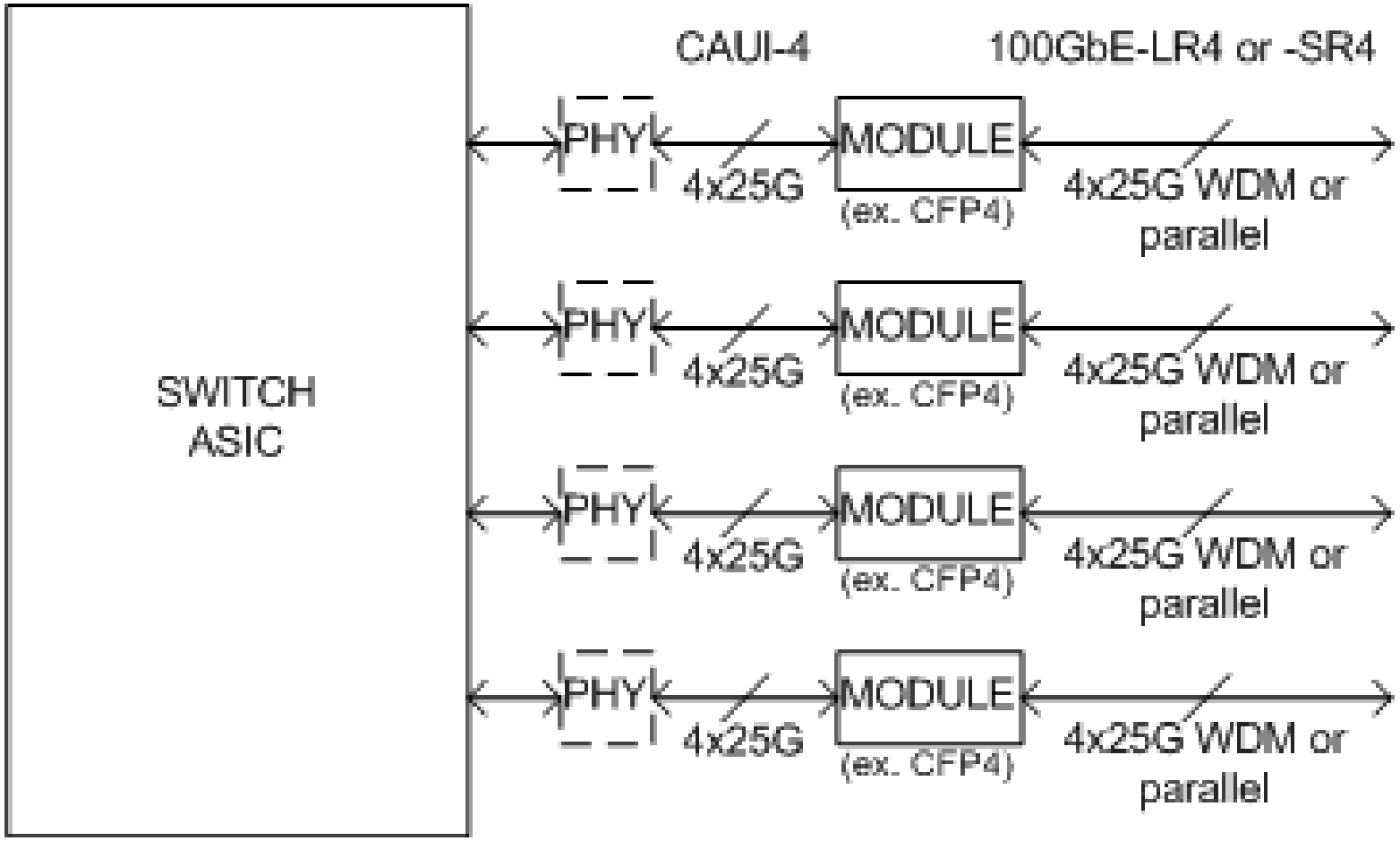
Near-Term 400GbE PMD Observations

- Today's priority for optical component industry is to reduce the cost, size and power of 100GbE interfaces
- Long-term (high-volume) 400GbE interface technology, such as duplex SMF WDM, possibly with HOM (higher order modulation,) will require large R&D investment
- Initial 400GbE port volumes will be low so there is no near-term ROI on a large 400GbE R&D investment
- Many optical component suppliers supported 400GbE assuming no need for large near-term 400GbE PMD R&D
- End user expectation of 400GbE is 100GbE bit/sec cost parity, which is inconsistent with advanced technology
- These constraints are best met by configuring 4x 100GbE interfaces as initial 400GbE PMDs (16x25G architecture)

Long-Term 400GbE PMD Observations

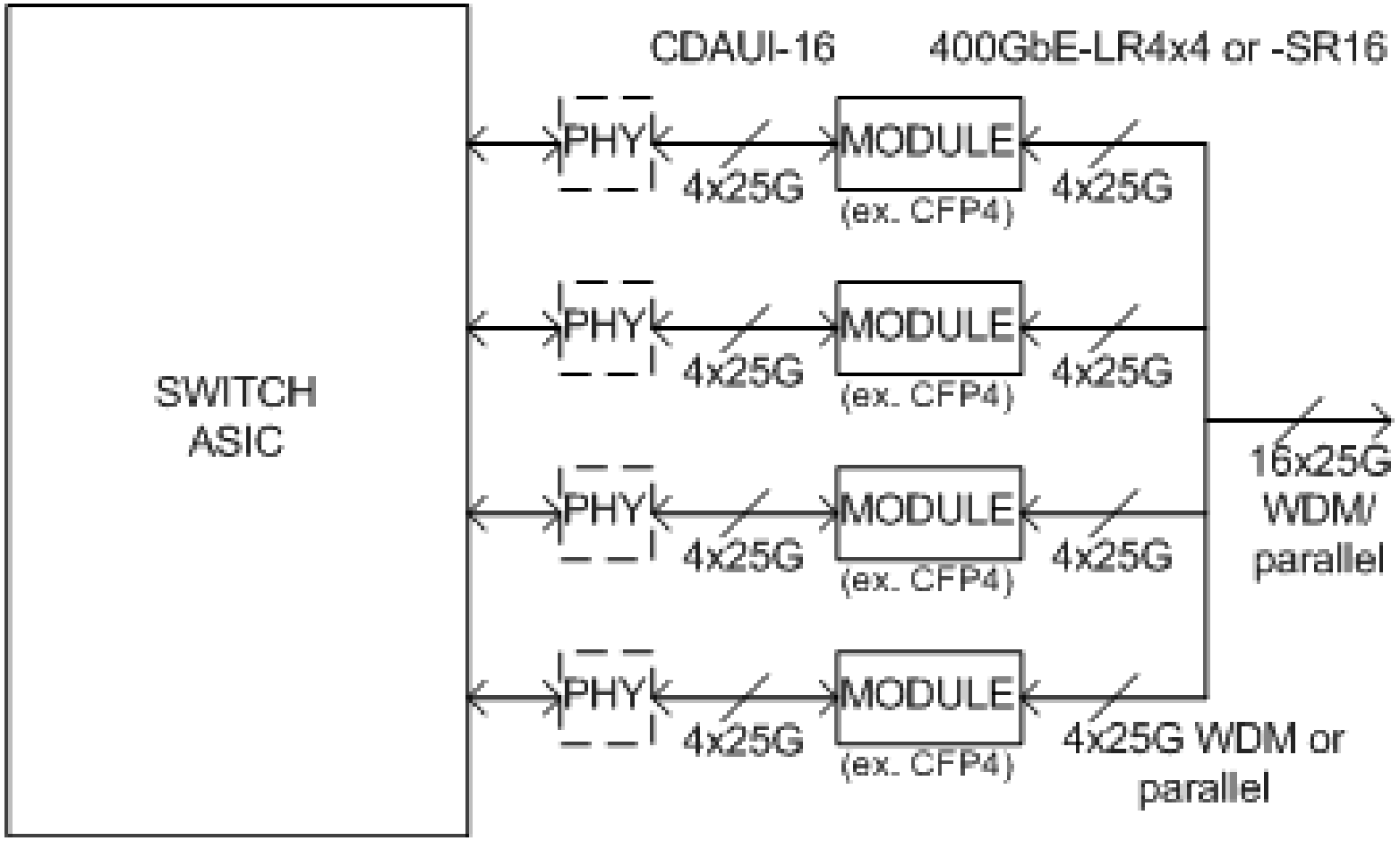
- Long-term (high-volume) 400GbE interfaces will not use 16x25G architecture because of density, size, power and cost limitations
- Long-term 400GbE interfaces will be duplex fiber
- Candidate long-term optical architectures are 8x50G WDM or 4x100G HOM (higher order modulation) & WDM
- If 4x 100GbE meets near-term 400GbE interface needs, then definition of long-term 400GbE interfaces is best deferred; we will know more in the future
- Candidate electrical I/O lane rates are 50Gb/s & 100Gb/s
- 50Gb/s chip-to-module electrical I/O is now being standardized in the OIF CEI-56G-VSR project
- There is no need for competing standards; OIF in liaison with the IEEE is well positioned to develop 50G specs.

100GbE Configuration



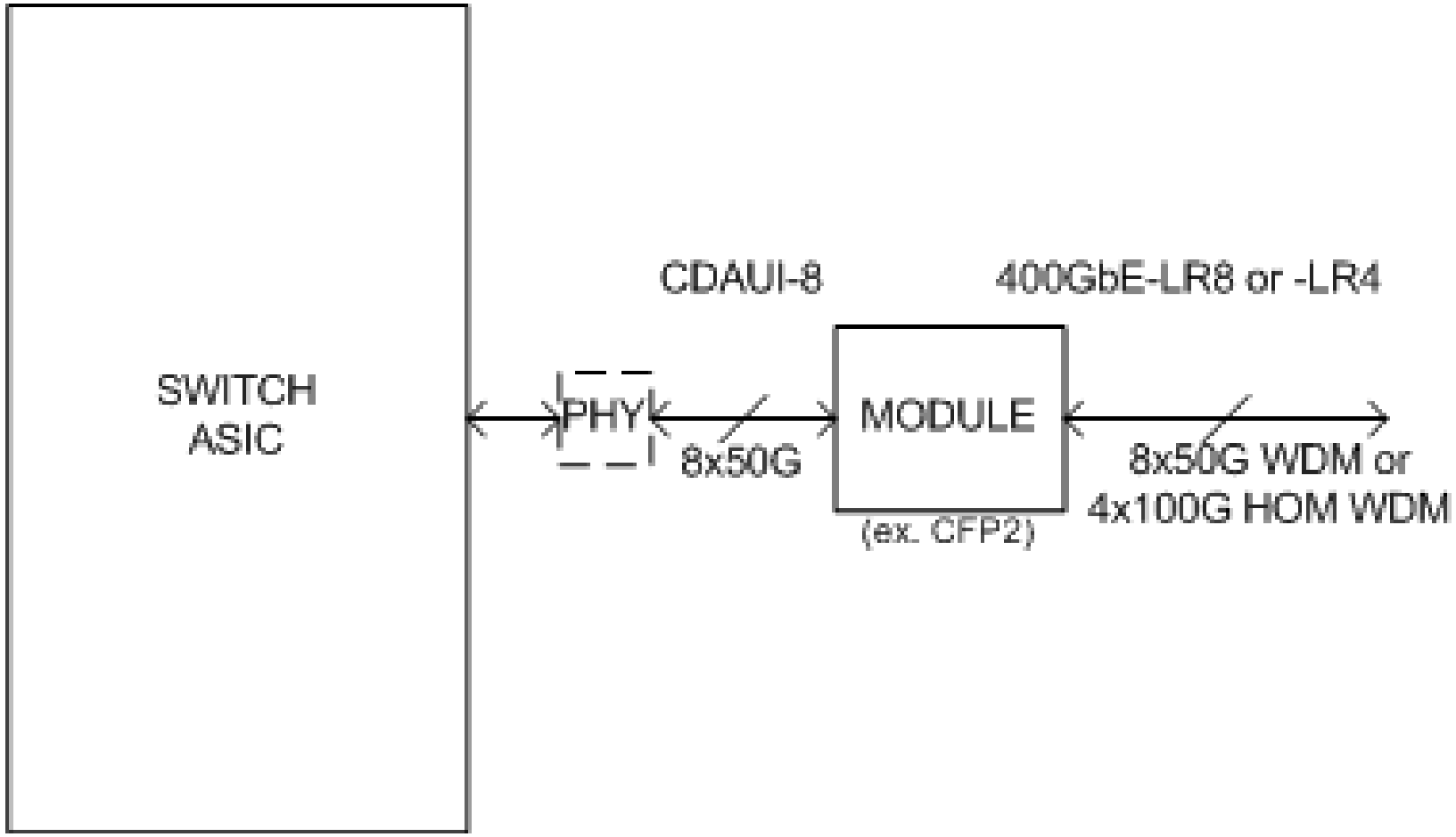
May also include 100GbE-nR4 if adopted by 802.3bm

Gen1 400GbE Configuration



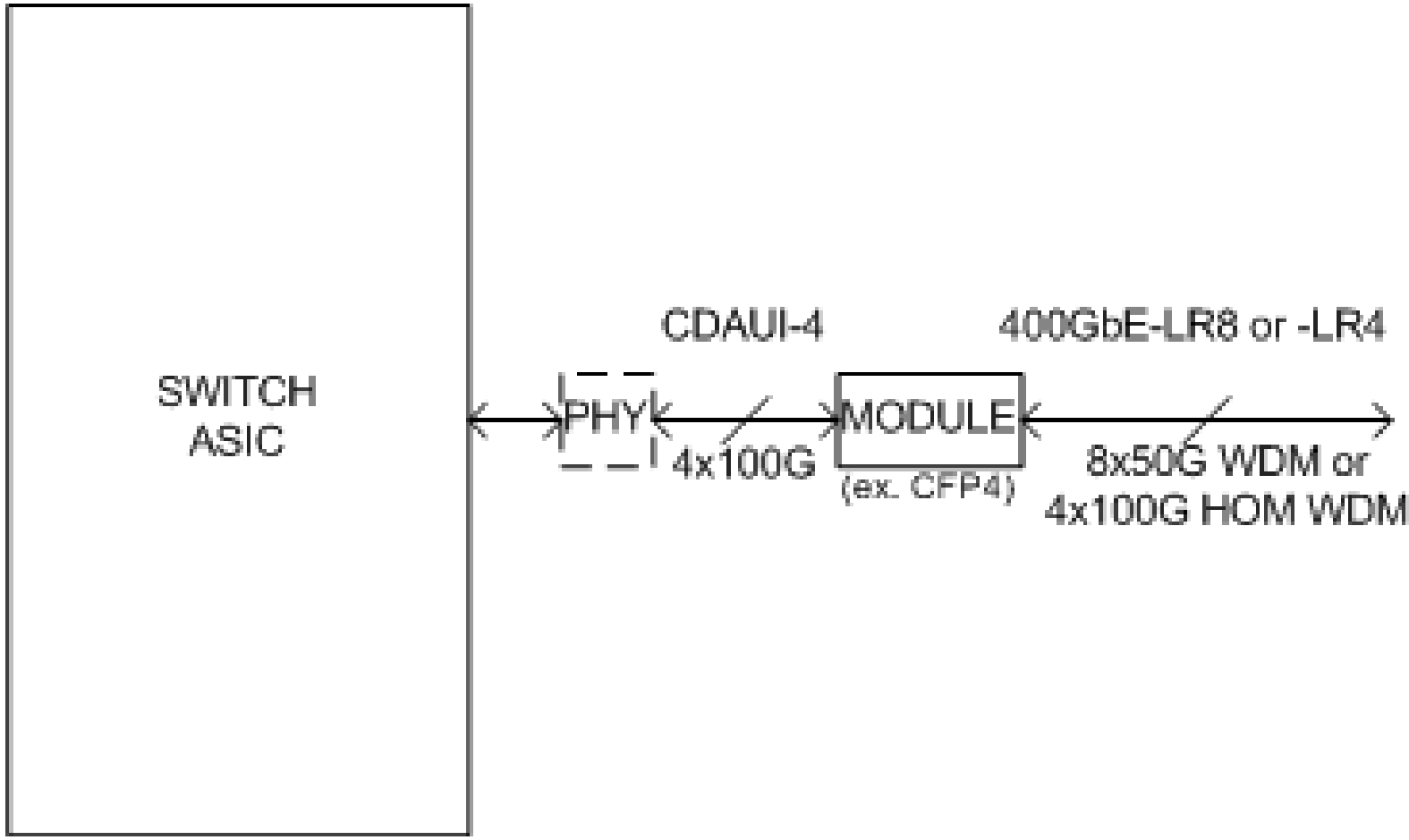
4x 100GbE ports aggregated into 400GbE port using cables

Gen2 400GbE Configuration



Possible SR8 or other parallel configurations not shown

Gen3 400GbE Configuration



Possible SR8 or other parallel configuration not shown

Possible 400Gb/s Standardization Approach

- SG Objective: specify only 400Gb/s MAC and PCS

  Define PCS to support 16x25G, 8x50G, and 4x100G lane architectures, with full interoperability between all combinations, based on 25G Virtual Lanes (VLs)

- 5C TF: describe 16x25G interfaces in an informative appendix:
  - 4x CAUI-4 (“CDAUI-16”)
  - 4x 100GbE-LR4 (“400GbE-LR4x4”)
  - 4x 100GbE-SR4 (‘400GbE-SR16”)
  - Define 1x12 & 2x16 MPO connector pin-out
- 5C TF: consider Clause 91 KR4 RS-FEC across 4x25G VLs and study coding gain loss because of reduced block size
- Develop advanced long-term 400GbE technology for standardization in a future 802.3 project