

CDAUI: Objective Proposal

Hugh Barrass, Cisco
John D'Ambrosia, Dell
Gary Nicholl, Cisco

IEEE 802.3 400 Gb/s Ethernet Study Group

IEEE 802.3 September Interim
York, UK

Introduction

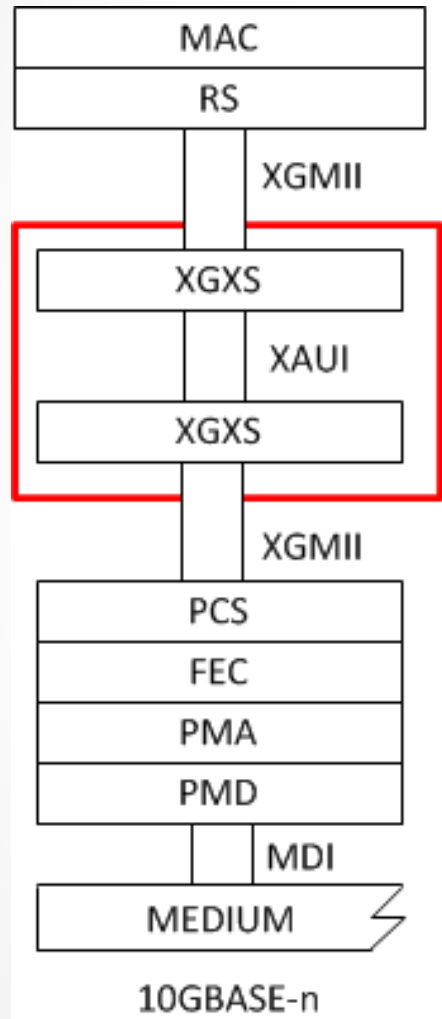
- **Initial discussions regarding FEC for PMDs has raised a number of other discussions**
 - **CDAUI:**
 - **Will FEC be needed for CDAUI?**
 - **Will FEC be same for different generations of CDAUI, i.e 16x25, 8x50, 4x100?**
 - **Will FEC for CDAUI be same as PMDs?**
 - **Interoperability between different generations of CDAUI / FEC / PMDs?**
 - **Possibility of a 100G Extender Sublayer (CDGXS)?**

Historical Perspectives

802.3ae and 802.3ba

...

10 GbE Architecture



XGXS Sub-layer

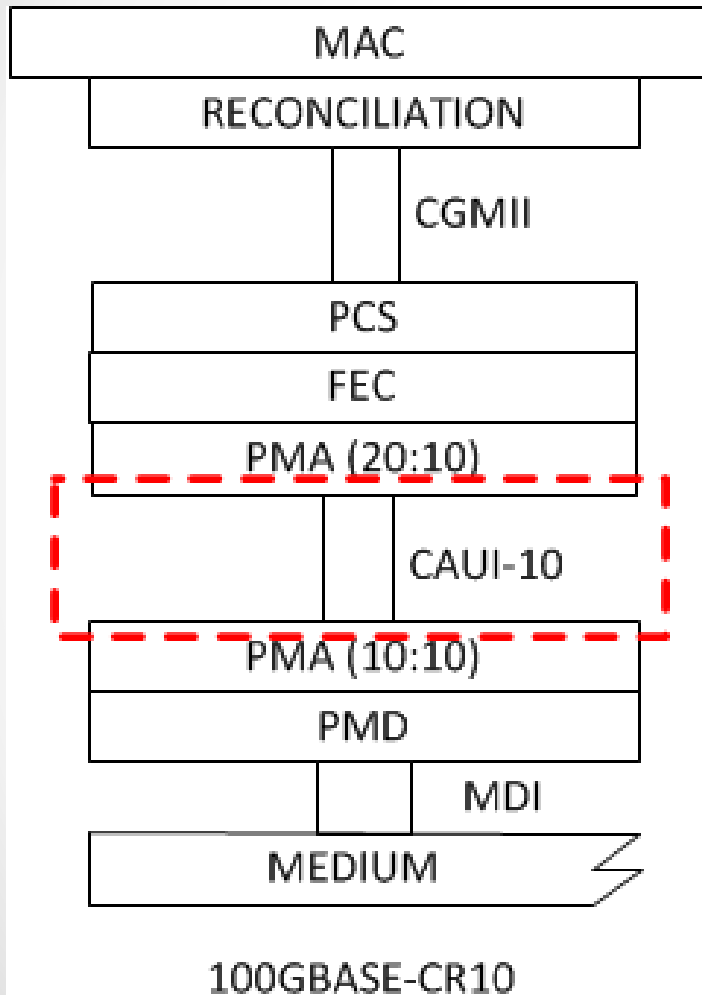
- XGMII Extender contains XAUI
- 8B / 10B encoding / decoding
- Clock / data recovery in XGXS

- XGXS encoding does not match 10 GBASE-R (64b/66b) PCS
- Added complexity
- Limited flexibility

Multiple PCS's possible

- Clauses 48 (8B/10B), 49 (64B/66B), 55 (twisted pair PCS)

802.3ba 40 / 100 GbE Architecture



CAUI-10

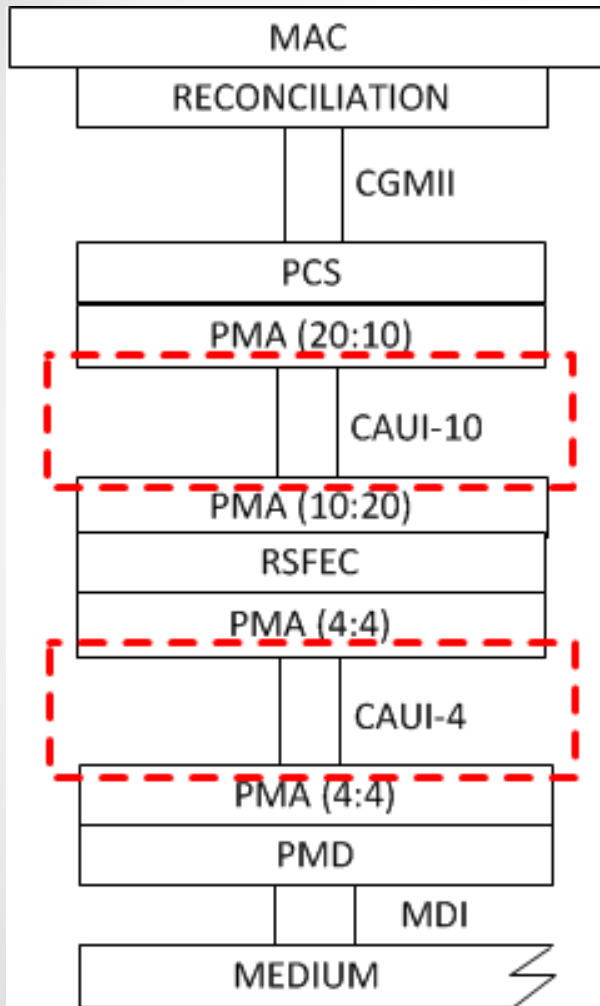
- No extender sublayer
 - No additional encoding
 - Can move between sub-layers in PHY
 - Increased flexibility
 - Reduced complexity
- Not above PCS!

802.3ba Architecture Legacy



100GBASE-CR4 and 40GBASE-T Development Efforts

100GBASE-CR4 Architecture



100GBASE-CR4

CAUI-10

- No extender sublayer
- No additional encoding
- Can only be between PCS and top FEC

RSFEC

- Transcoding
- FEC encoding
- 4 lanes

CAUI-4

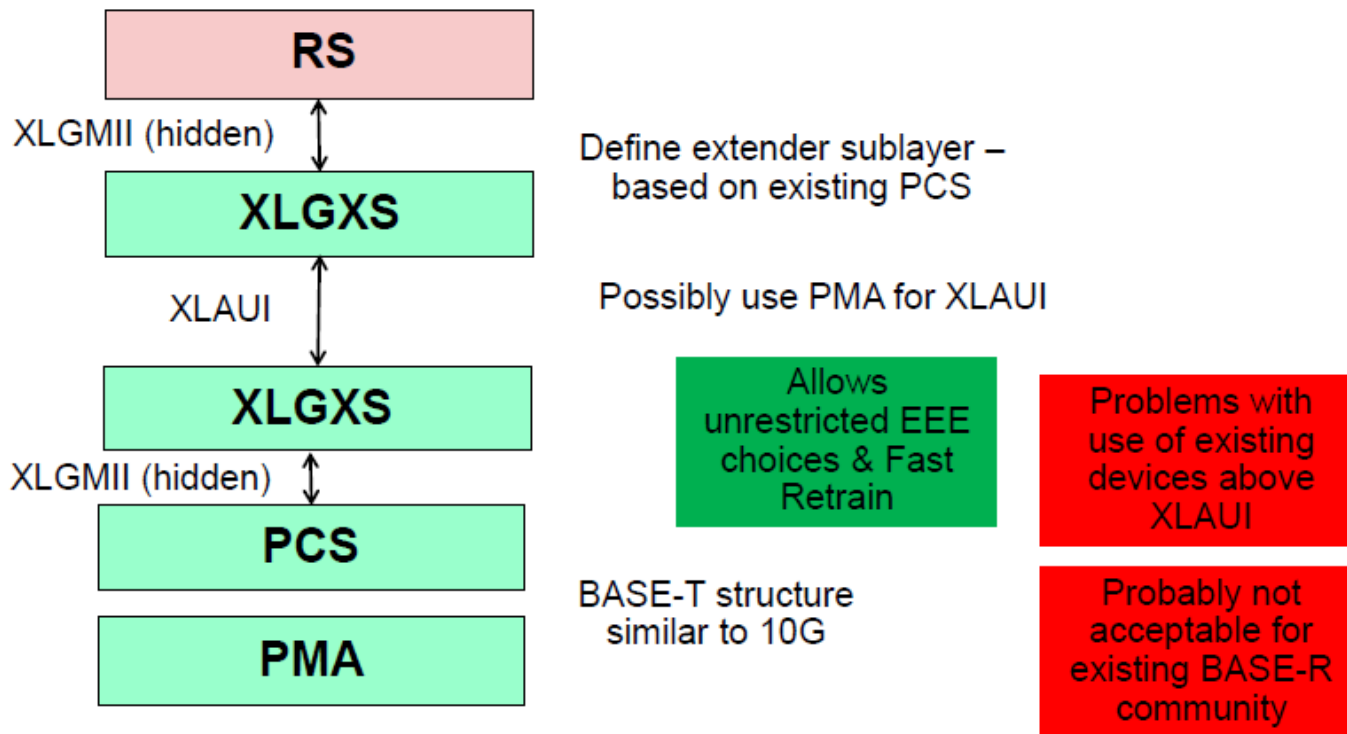
- No extender sublayer
- No additional encoding
- Can be between any sub-layers in PHY

- Added complexity / rules

Implications on 40GBASE-T (1 of 3)

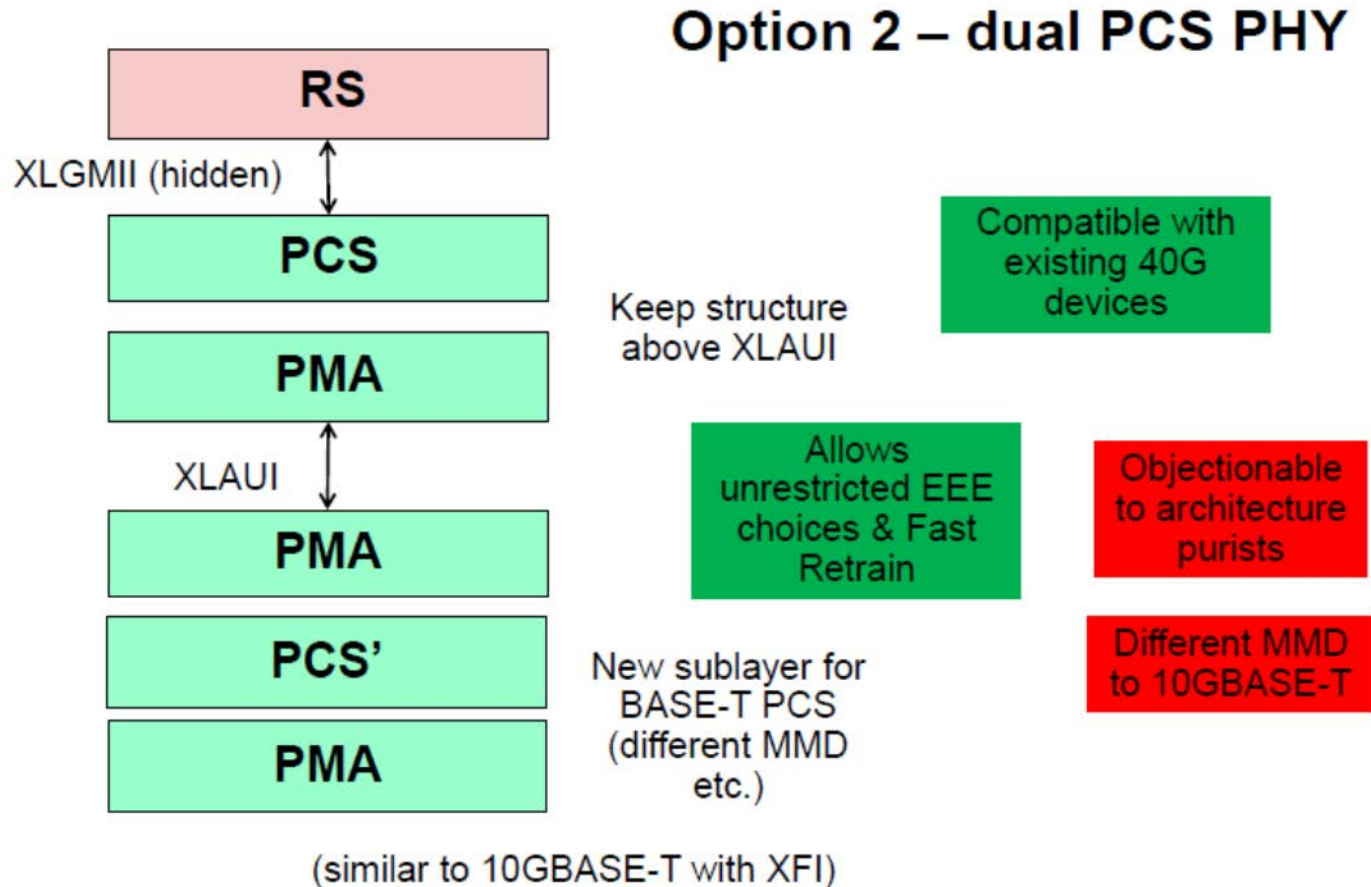
40GBASE-T solution

Option #1 – old school approach



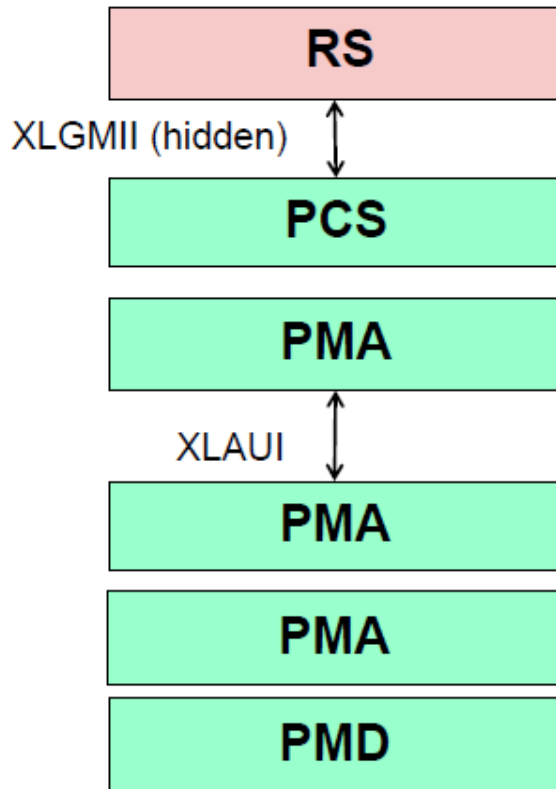
Implications on 40GBASE-T (2 of 3)

40GBASE-T solution



Implications on 40GBASE-T (3 of 3)

40GBASE-T solution



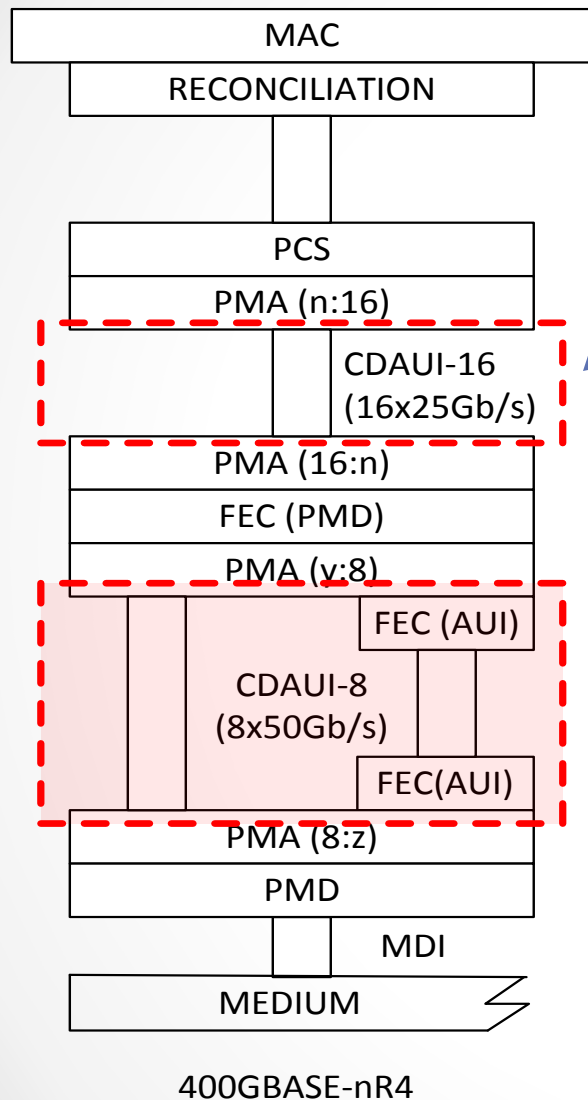
Option 3 – BASE-T PMA/PMD

- Compatible with 40G architecture
- Keep structure of 40GBASE-R
- Approach similar to 100G copper
- Define transcoding & FEC in PMA (& FEC sublayer if necessary)
- EEE behavior governed by PCS
- Fast Retrain would require Clause 82 edits

400GbE Architecture Discussions

...

Discussion Related to FEC



CDAUI-16

- No extender sublayer
- No additional encoding
- Is FEC needed to meet interface channel requirements?
- Placement may be limited by FEC (PMD)

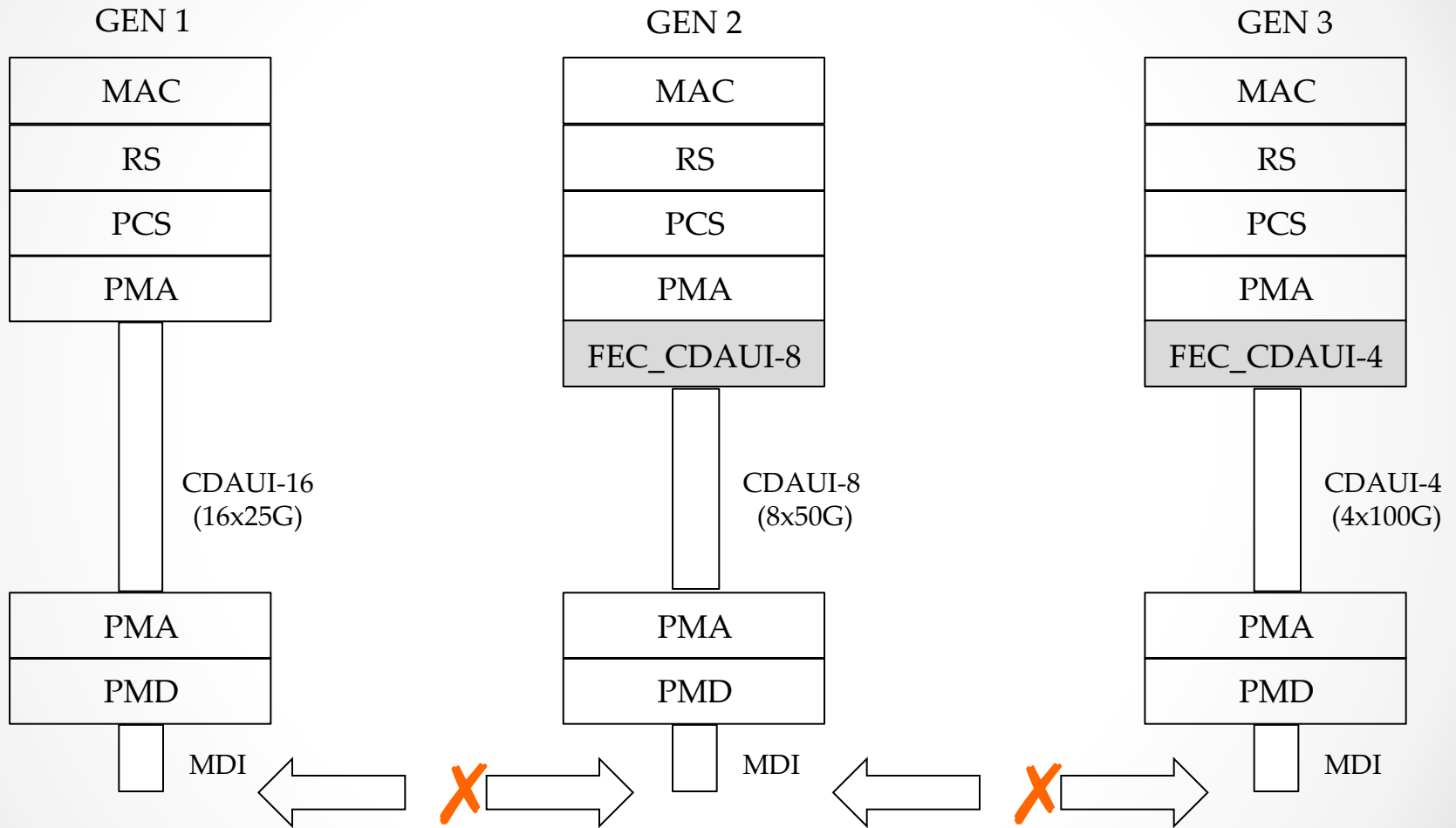
FEC (PMD)

- TBD

CDAUI-8

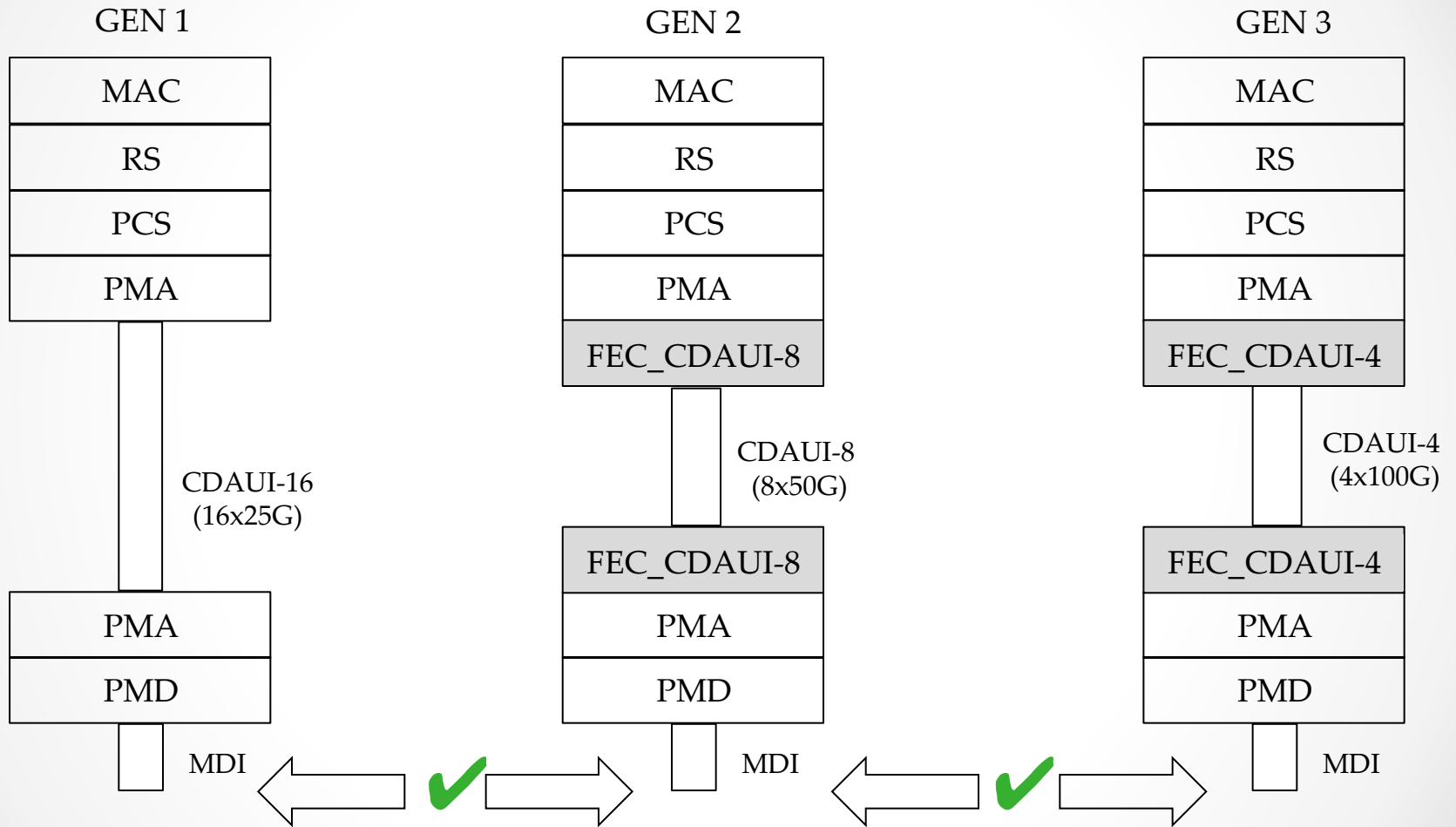
- Will FEC(AUI) be needed for this interface channel requirement?
- Do we need to reconsider an extender sub-layer concept?

CDAUI Generational Interop – The Problem



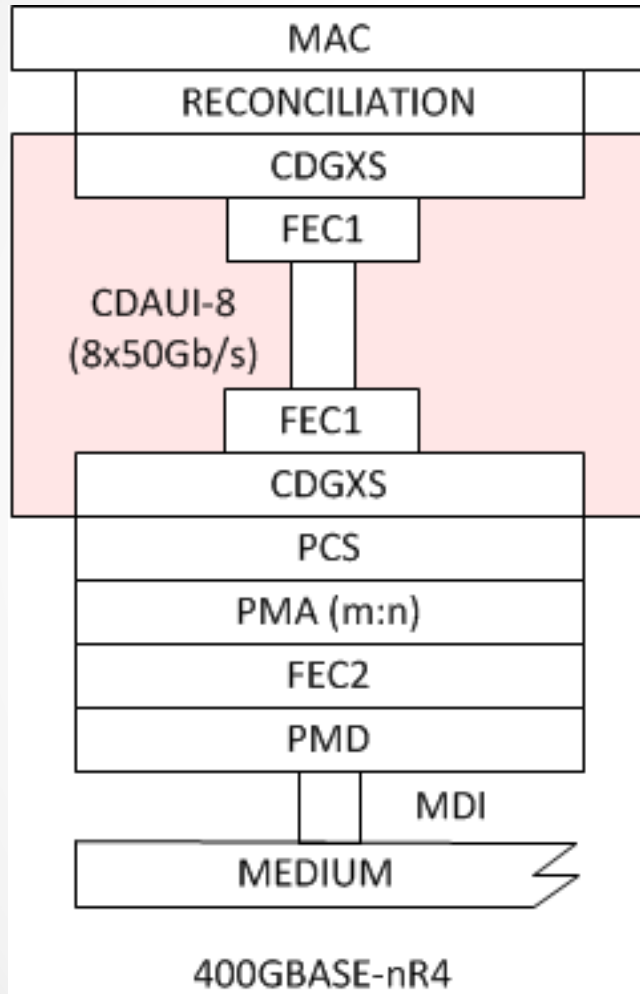
- Single PMD Type, three different generations of CDAUI (-16,-8 and -4)
- No Interop between different generations.
- Cannot simply add CDAUI FEC as a single layer into the stack !!

CDAUI Generational Interop – The Solution



- FEC/Coding for CDAUI must be localized (and not go out on the MDI)
- Full Interop between different generations !!

An Extender Sublayer above the PCS?



- Will we need multiple PCS?
 - WHO KNOWS?
- CDGXS may include
 - Encoding
 - FEC
 - CDAUI-n electrical specifications
 - Alignment markers?
- Would the FEC in CDGXS be the same FEC for the PMD?
 - Can we assume this?
 - Do we need independence?
- While part of the physical layer specification (not PHY), we suggest specific objective
 - Could be different than CAUI
 - We might define an optional physical instantiation above the PCS since XGMII / XAUI.

Summary

- **Various Issues for Discussion**
 - The CDAUI and its definition?
 - A potential extender sub-layer?
 - FEC relationships between CDAUI and PMD?
 - Potential applications?
 - Interoperability between inter-generation implementations?
 - Required FEC for future optional physical instantiations?
 - Support for multiple PCS's?
- **Recommend adding objective –**
 - Support optional CDAUI for chip-to-chip and chip-to-module applications