400Gb/s Logic Ad hoc report

IEEE 400 Gb/s Ethernet Study Group

September 2013 York

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Introduction

- The 400 Gb/s Ethernet Study Group Logic Ad hoc has:
  - Held 2 meetings on August 7th and 20th
- Reviewed 5 presentations:
  - Error performance objective for 400GbE : anslow_01_0813_logic
  - 400GbE BER Objective From Perspective of MTTFPA: song_01_0813_logic
  - 16 v 80 PCS Lanes for 400GbE, an implementer's perspective: begin_01_0813_logic.pdf
  - 400GbE PCS Architectural requirements: gustlin_01_0813_logic
  - FEC/Architecture/Extender Sublayer: dambrosia_01_0813_logic
- Meeting minutes and presentations can be found at:
  - http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml

400GbE Logic Ad hoc Priorities

- The stated charter is: Evaluate 400GbE architecture implementations to make recommendations regarding possible objectives

- The study group passed a motion adopting many of the logic related objectives in the last study group meeting, but we have yet to adopt an objective on BER (or FLR). Depending on what happens in this meeting with respect to the objectives, we will prioritize presentations that address gaps in the logic objectives going forward vs. discussing PCS options

- Dates of future Logic Ad hocs will be announced via the reflector

Possible 400GbE Logic Related Objectives

- Support a MAC data rate of 400 Gb/s
- Support full-duplex operation only
- Preserve the 802.3 / Ethernet frame format utilizing the 802.3 MAC
- Preserve minimum and maximum FrameSize of current 802.3 standard
- Provide appropriate support for OTN
- To define optional Energy-Efficient Ethernet operation for xxx PMD or interface
  - PMD type likely to define what mode(s) are supported, deep sleep vs. fast wake

- Support a (BER or frame loss ratio, pick one) better than or equal to x
  - Likely to be a lot of discussion around this objective
  - With at least some PHYs using FEC it might be better to specify frame loss ratio instead of BER

Thanks!