Simulation results for NRZ, ENRZ & PAM-4 on 16-wire full-sized 400GE backplanes

Brian Holden
Kandou Bus, S.A.
brian@kandou.com

IEEE 802.3 400GE Study Group
September 2, 2013
York, United Kingdom

KANDOU BUS

IP Disclosure

- As mentioned in the initial presentation of related material at the May and July 2013 802.3 meetings, this presentation includes technology that may be the subject of multiple patent applications, applications in process, and patents by Kandou Bus, S.A.

- Assuming that this Study Group results in a PAR, that Kandou Bus, S.A. is committed to filing an Letter of Assurance against that PAR. (IEEE Patcom will not accept a LOA against a study group.)

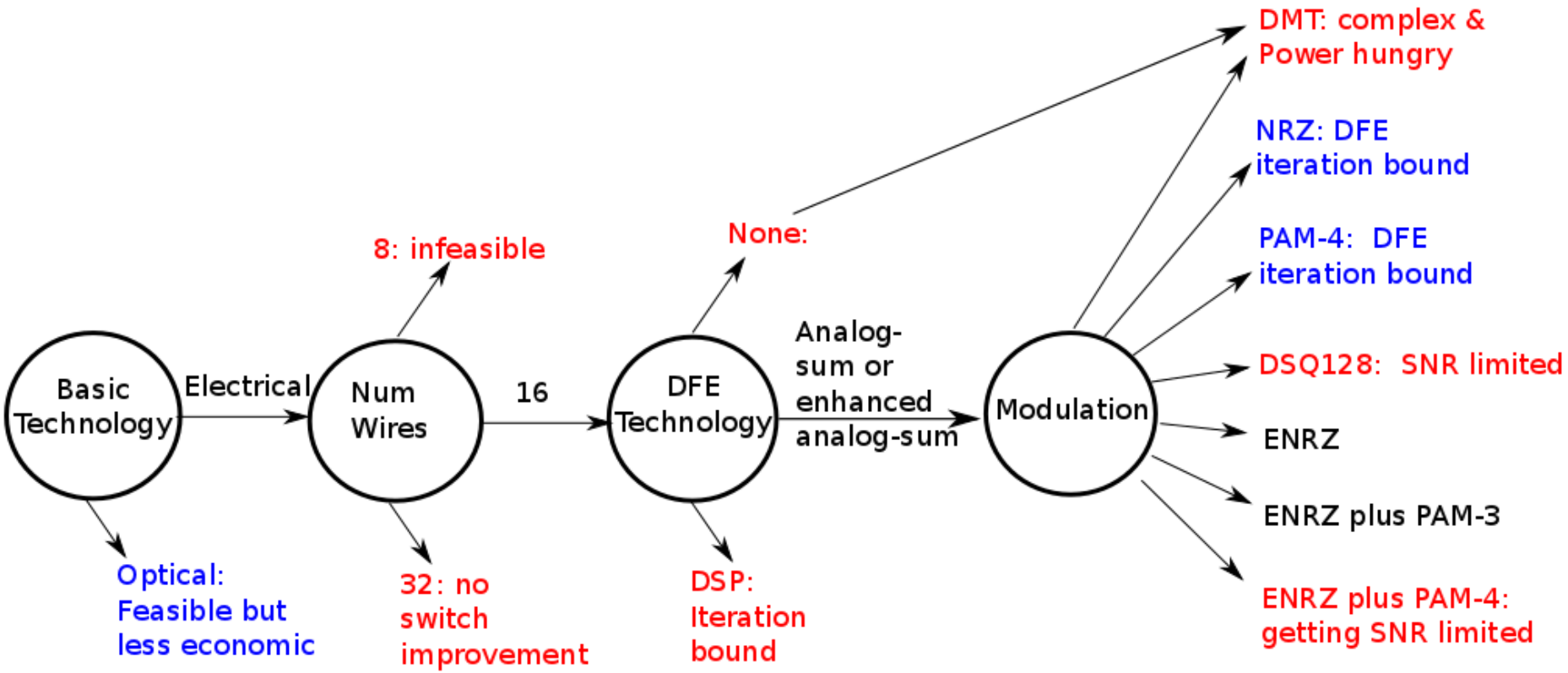
- That LOA will guarantee that licenses to patents derived from these applications will be available on a Reasonable And Non-Discriminatory basis, should Kandou's technology be adopted into the 400GE specification. Further, we pledge to be good corporate citizens.

Outline

- **This presentation contains:**
  - **Review of the 400GE backplane decision tree**
  - **Technical feasibility simulation results for NRZ, ENRZ & PAM-4 on full-sized 400GE 16-wire backplane links**
    - **Demonstrates that useful 400GE backplanes are technically feasible, completing an objective of the 400GE Study Group, since electrical backplane specifications have been an element of the previous three Ethernet speeds and their feasibility has been a question-mark for 400GE to date**
  - **Consensus building activity**
    - **Kandou will propose a new project at the next OIF meeting entitled: EEI-112/37-LR (Ensemble Electrical Interface at 112 Gbps and 37 GBaud, Long Reach)**
  - **(Time allowing) – ENRZ and the PCS layer**

Review of decision tree of the options for 400GE backplanes

- **Below is a decision tree for 400 GE backplanes (presented at the last meeting)**



Review of Ensemble NRZ

- Ensemble NRZ coding delivers 3 bits over an ensemble of 4 wires
  - The symbol rate is 2/3rds of what is required for differential NRZ for the same throughput
    - For NRZ: 51.5 GBaud
    - For ENRZ: 34.1 GBaud
  - The transmit codewords are
    - For NRZ: +/- (1, -1)
    - For ENRZ: +/- (the four permutations of 1, -1/3, -1/3, -1/3)
  - The termination line power for CML drivers is 1/3 of the two higher-speed differential NRZ channels that are otherwise needed at the same rate and throughput (the driver power is implementation dependent)
    - For 2 x NRZ: $2 \times 2 \times 1^2 = 4$
    - For 1 x ENRZ: $1^2 + 3 \times (1/3)^2 = 1.33$

- The 4 wires in the ensemble must have low intra-ensemble skew, on the same order as differential's intra-pair skew
  - Ensembles are terminated jointly to an AC ground at the receiver

Review of Ensemble NRZ continued

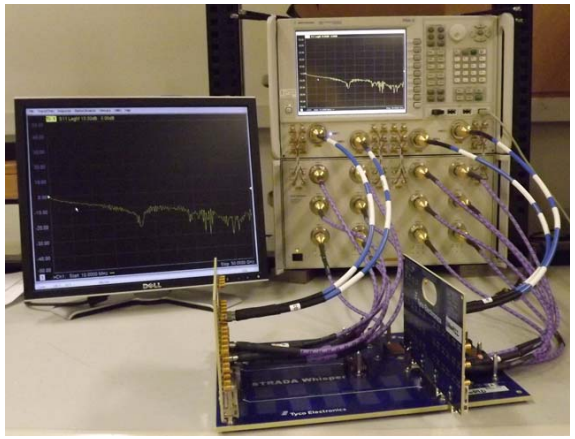
- Ensemble NRZ (ENRZ)
  - Ensemble NRZ gets 3 bits per symbol over 4 wires
    - Ensemble NRZ receivers are reference-less, like NRZ
    - The SNR degradation is 6.5dB as compared to NRZ
  - A specification similar to Clause 94's linearity requirement but extended over the channel will be needed to constrain the combination of the Tx non-linearity and channel imbalances amongst the four wires so that binary DFEs can be used
    - Imbalances cause crosstalk between the three sub-channels
    - 34.1 GBaud binary DFEs will be much easier to implement than 51.5 GBaud binary DFEs
  - Increases the throughput by 50% for a given DFE iteration bound frontier by delivering an effectively better channel
    - Four correlated wires are better than two

Simulated Channel

- **The channel used was the second channel presented by TE Connectivity at the Geneva Meeting**

STRADA Whisper™ Backplane Channel

40” Link Test Set-up



H11-H12	H14-H15	H17-H18
G11-G12	G14-G15	G17-G18
F11-F12	F14-F15	F17-F18

- All data is measured and includes 2.4mm test points
- Measurements are pair G14-G15 centric .s4p files
- 4 Near-End and 4 Far-End measurements
- Data is from 0-30GHz in 10MHz steps

DAUGHTER CARD
- Board Material = Megtron6 VLP
- Trace length = 5”
- Trace geometry = Stripline
- Trace width = 6 mils
- Differential trace spacing = 9 mils
- PCB thickness = 110mils, 14 layers
- Counterbored vias, up to 6mil stub
- Test Points = 2.4mm (included in data)

BACKPLANE
- Board Material = Megtron6 HVLP
- Trace length = 30”
- Trace geometry = Stripline
- Trace width = 7 mils
- Differential trace spacing = 9 mils
- PCB thickness = 200 mils, 20 layers
- Counterbored vias, up to 6mil stub

CONNECTORS
- Dataset 1 includes
  - Mated standard STRADA Whisper connector at each end
- Dataset 2 includes
  - Mated Embedded Capacitor STRADA Whisper connector at one end and,
  - Mated standard STRADA Whisper connector at other end

TE connectivity

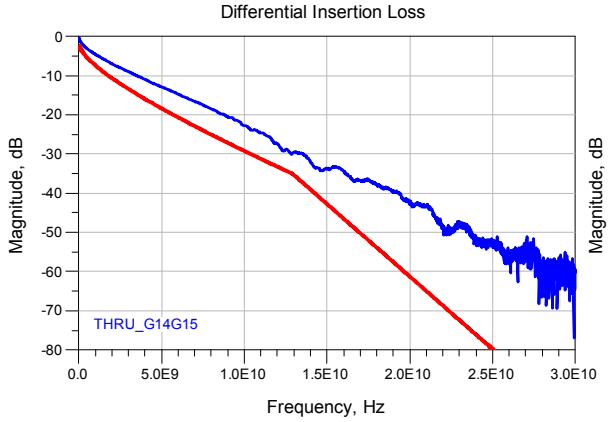
KANDOU BUS

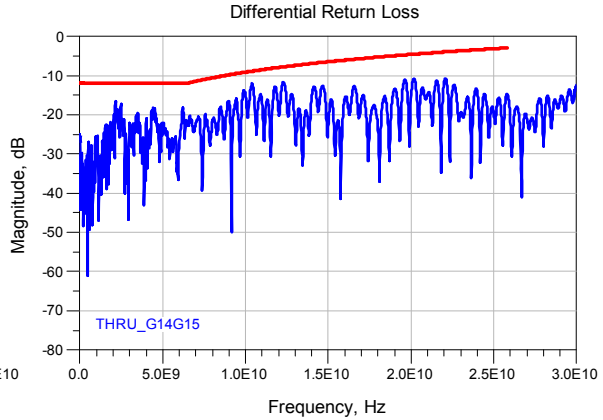
Simulated Channel

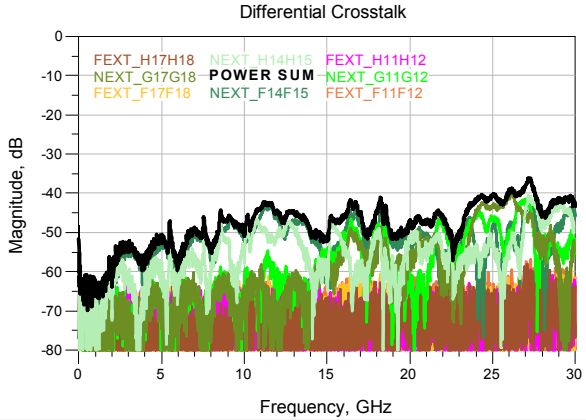
- **That channel is about 5 dBs better than the 802.3bj draft spec.**

STRADA Whisper 4.5mm System

EMBEDDED CAPACITOR







8 Crosstalk Aggressors – 4 NEXT AND 4 FEXT
Maximum Frequency = 30 GHZ

	PAM-2 [100GBASE-KR4]	PAM-4 [100GBASE-KP4]
COM*	5.663 dB	9.0487 dB

* COM = Channel Operating Margin, Figure of Merit for the channel per IEEE802.3bj Draft 2.1
Calculated using COM Matlab code provided on the IEEE 802.3bj website
Code Revision = com_d2p1_02_0613
COM needs to be >3dB for the channel to be compliant.

Skew managed pair

- The TE Connectivity connector is a pair-in-row connector, which is perfect for use with ENRZ
- Our simulation used two 4-port S-Parameter data for the two pairs:
  - The pairs had tight intra-pair backplane and daughter-card skew
  - The pairs traveled on the same row of each connector
  - The stripline pairs were independent
    - Other simulations have shown that a 3x separation is optimal for ENRZ
- The three sub-channels are:
  - (A+B)/2 vs. (C+D)/2 (weakest)
  - (A+C)/2 vs. (B+D)/2
  - (A+D)/2 vs. (B+C)/2

KANDOU BUS

Modulation-independent jitter calculation

- We calculate the modulation-technique-independent jitter magnitude
  - In order to give an apples-to-apples comparison, we assume that the same semiconductor process node and PLLs are used for all three modulation techniques

- This jitter calculation is made using the 802.3bj Clause 93 COM jitter numbers with a detector error rate of 1E-5 (assuming the use of FEC)
  - Rate (GBaud) 25.8
  - UI (ps) 38.8

- Modulation-independent Jitter
  - Dual-dirac jitter peak = 0.05UI 3.88
  - RMS jitter = 0.01UI 0.39
  - Random jitter with Q(1E-5) 3.31
- Total (ps) 7.2ps

KANDOU BUS

Simulations

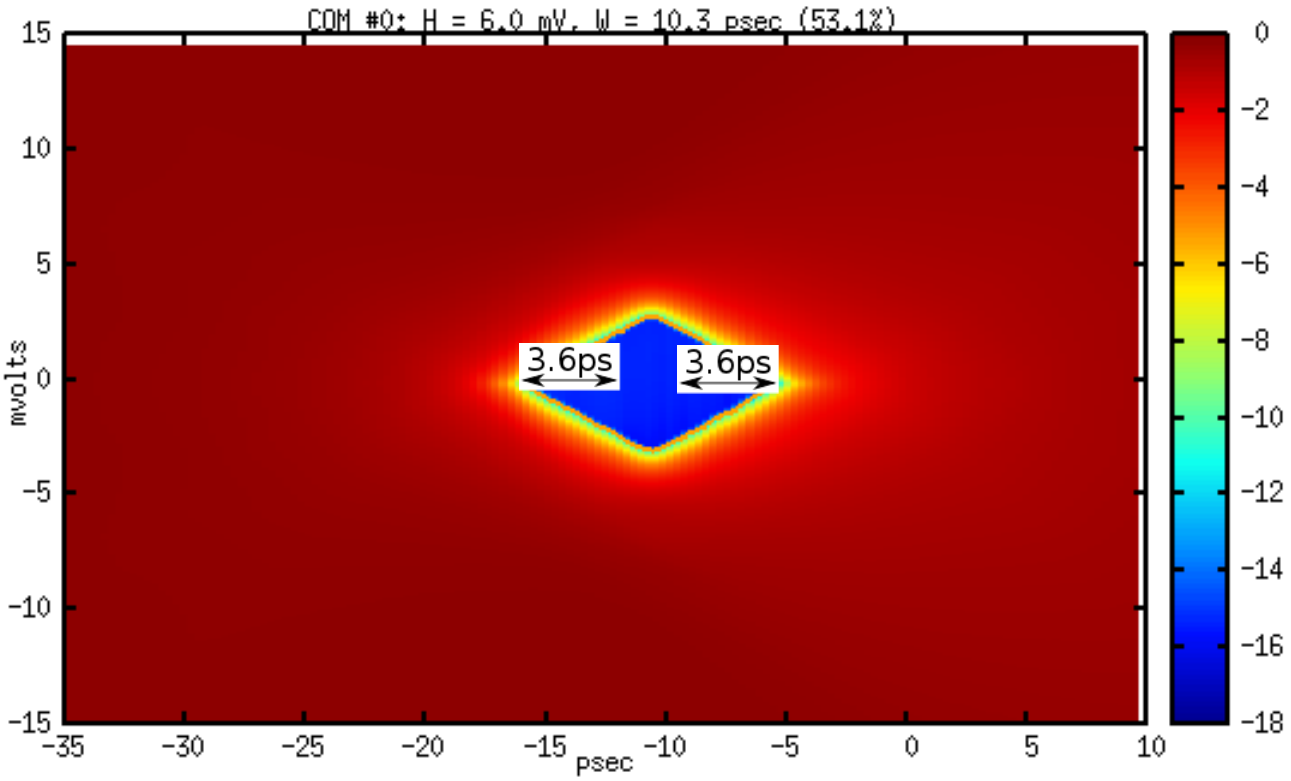
- **The following scenarios are simulated:**

• Modulation	NRZ	ENRZ	PAM-4
• Rate (GBaud)	51.5	34.1	25.8
• UI (ps)	19.4	29.3	38.8

- **The probability distribution functions are plotted**
  - **The jitter is not included in the simulation and must be subtracted from the horizontal eye opening**
- **Simulation parameters:**
  - **Transmit level = 1.2V Max V_{DiffPP} including the FIR**
  - **Transmit rise/fall time = 10ps**
  - **4 FEXT aggressors are include for each**
  - **No added Tx/Rx circuit component noise is included for any**
  - **Receiver uses a 14 Tap DFE for each**

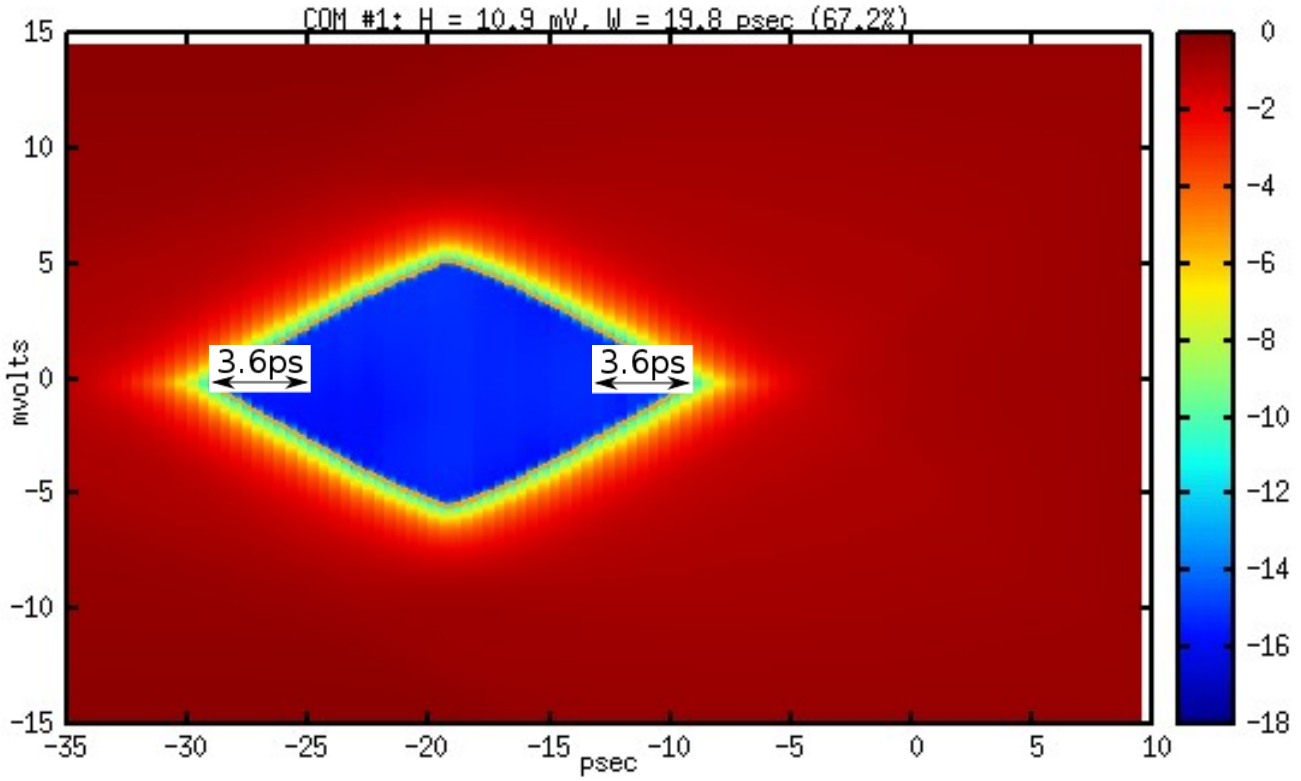
Simulated NRZ result

- Simulation at 51.5 GBaud
- The eye without jitter is 10.6 ps wide
- Subtracting 7.2 ps of jitter, **the eye is effectively closed** at 3.4 ps



Simulated ENRZ result

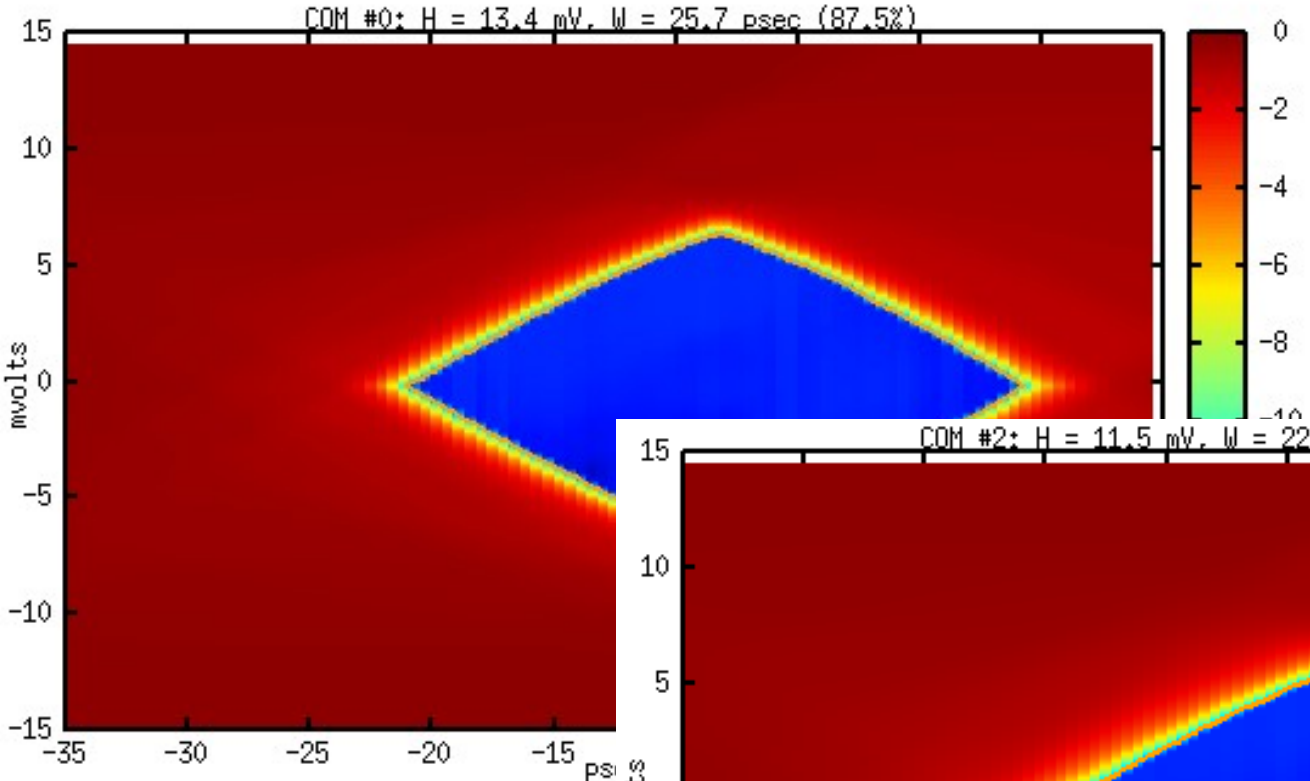
- Simulation at 34.1 GBaud
- The worst case eye (upper right) without jitter is 20.2 ps wide
- Subtracting 7.2 ps of jitter, **the eye is open** and 13 ps wide
- The eye is higher vertically than NRZ is as well

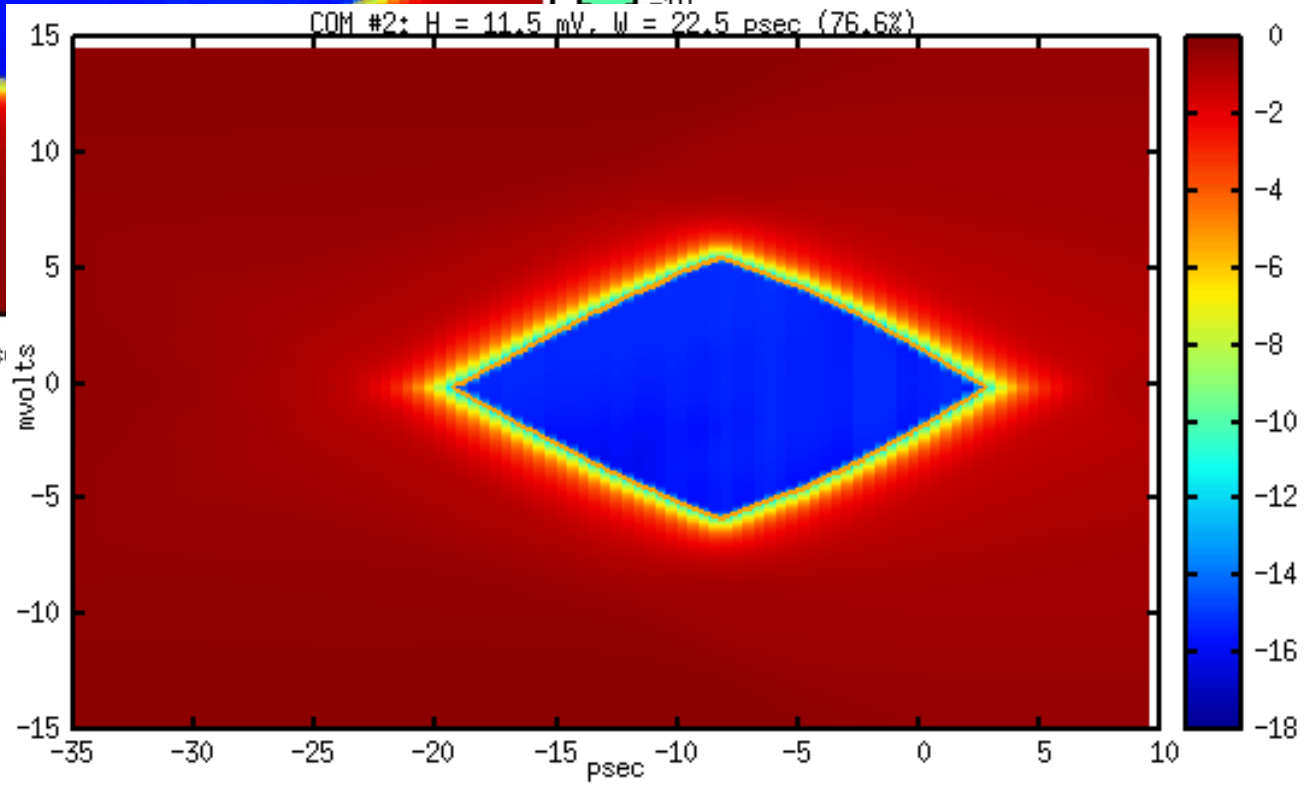


KANDOU BUS

Simulated ENRZ result

- The other two ENRZ eyes are slightly better

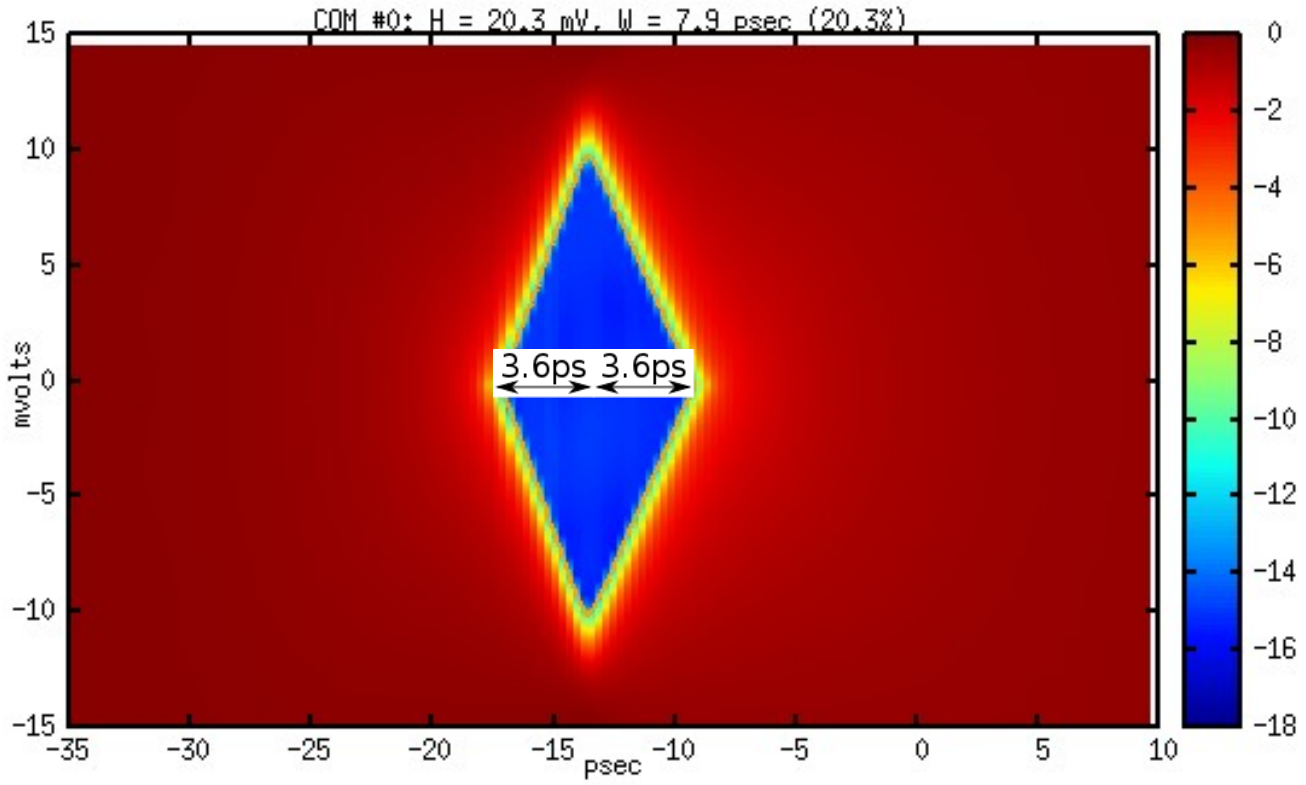




KANDOU BUS

Simulated PAM-4 result

- Simulation at 25.8 GBaud
- The worst case eye without jitter is 7.9 ps wide
- Subtracting 7.2 ps of jitter, **the eye is effectively closed** at 0.7 ps wide
  - Earlier 802.3bj presentations made similar projections about PAM-4



Consensus building

- Since ENRZ is that "strange new multi-wire technology from Switzerland", consensus building is required
- Kandou will propose to start a new project at the October OIF meeting entitled EEI-112/37-LR or (Ensemble Electrical Interface at 112 Gb/s and 37 GBaud, Long-Reach)
  - Hopefully that project will be started and help to work through the standards-related issues associated with using ENRZ long-reach links
- With luck, that output of that project will further the objectives of the 400GE Study Group (and/or the 802.3 project(s) that emerge from it) by specifying a reference-able link useful in a 16-wire full-sized 400 Gb/s backplane link

PCS layer requirements For the use of ENRZ

- Since this proposed use of Ensemble NRZ delivers three phase-associated 33 Gb/s channels, the PCS requirements for a sixteen wire 400GE backplane are that of four 100 Gb/s serial lanes.
  - There is no need to have an additional PCS multiplexing layer to de-skew and align the three 33 Gb/s channels
  - The linear H4 transform that ENRZ is based on delivers the data with no time ambiguity between the channels

- The three channels act as if they were a single 100 Gb/s serial link for alignment purposes

KANDOU BUS

PCS interworking with 25 Gb/s optics

- It seems likely that both 25 or 50 Gb/s optics will be used to support 400 GE channels
  - For these two cases, a 16-lane or 8-lane PCS layer would be used (16 x 25 or 8 x 50)

- Since a 3x33 Gb/s ENRZ link acts as if it were a single 100 Gb/s link, an additional PCS framing layer would be required after the ENRZ link to find the correct 25 Gb/s lanes for each of the optical links
  - Multiplexing layers are also needed independent of the use of ENRZ for numerous cases including when using 50 Gb/s optics with a 16-lane PCS layer

Conclusions

- This presentation showed a positive simulation result for ENRZ and a negative result for both NRZ and PAM-4 over the TE Connectivity channel shown at the June meeting
  - This demonstrates the technical feasibility of 16-wire 400GE backplane links, an important possible output of the 400GE Study Group

- ENRZ encoding may be a good choice for 16-wire 400GE backplane links
  - ENRZ reduces the excessive link rate needed by NRZ links, allowing their construction with existing and well-understood implementation techniques
  - ENRZ employs a relatively simple circuit & relies on a low-skew four wire ensemble that can be constructed with 2 correlated pairs and existing connectors
  - ENRZ's linear nature allows implementation flexibility
  - ENRZ saves a lot of power and has slightly lower EMI than NRZ does
  - No ENRZ-specific PCS layer is required as it delivers a 100 Gb/s link
  - Ensemble NRZ is much more like NRZ than PAM solutions are
  - Ensemble NRZ can use ordinary binary DFEs if the linearity/balance of the ensemble over the channel is constrained through a specification

- Kandou is proposing to start an EEI-112/37-LR project at the OIF