Technical feasibility of CMOS DMT transceiver for 400GbE SMF transmission

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Ian Dedic, Patricia Bower, Paul Little

Fujitsu Semiconductor

Supporters

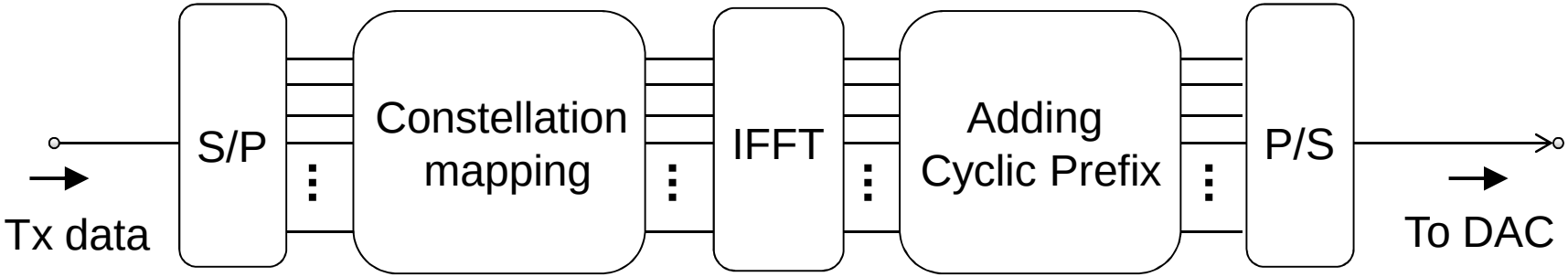
- Tomoo Takahara, Fujitsu Laboratories,
- Hideki Isono, Fujitsu Optical Components
- Tom McDermott, Fujitsu Network Communications, Inc.
- Martin Bouda, Fujitsu Laboratories America
- Beck Mason, JDSU
- David Lewis, JDSU
- Winston Way, Neophotonics
- Ilya Lyubomirsky, Finisar
- Moon S Park, OE Solutions

Outline

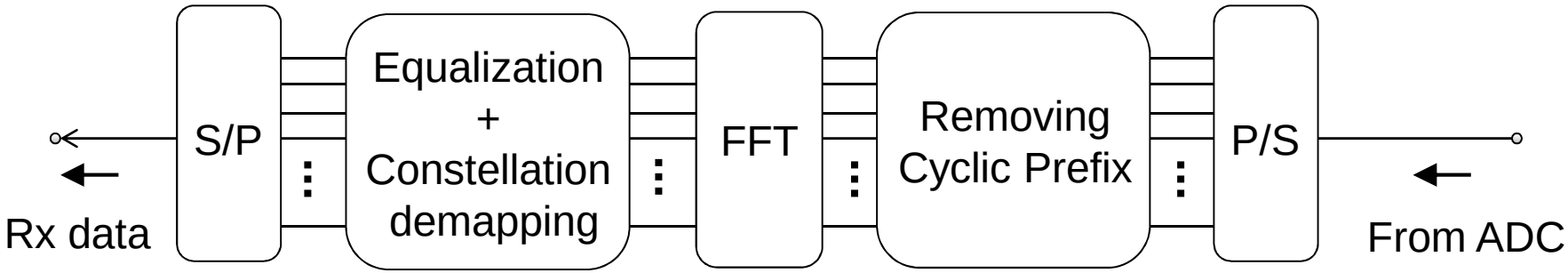
- DSP for DMT
- 400G DMT CMOS transceiver design
- 400G system implementation

Digital Signal Processing (DSP) for DMT

- DMT modulation

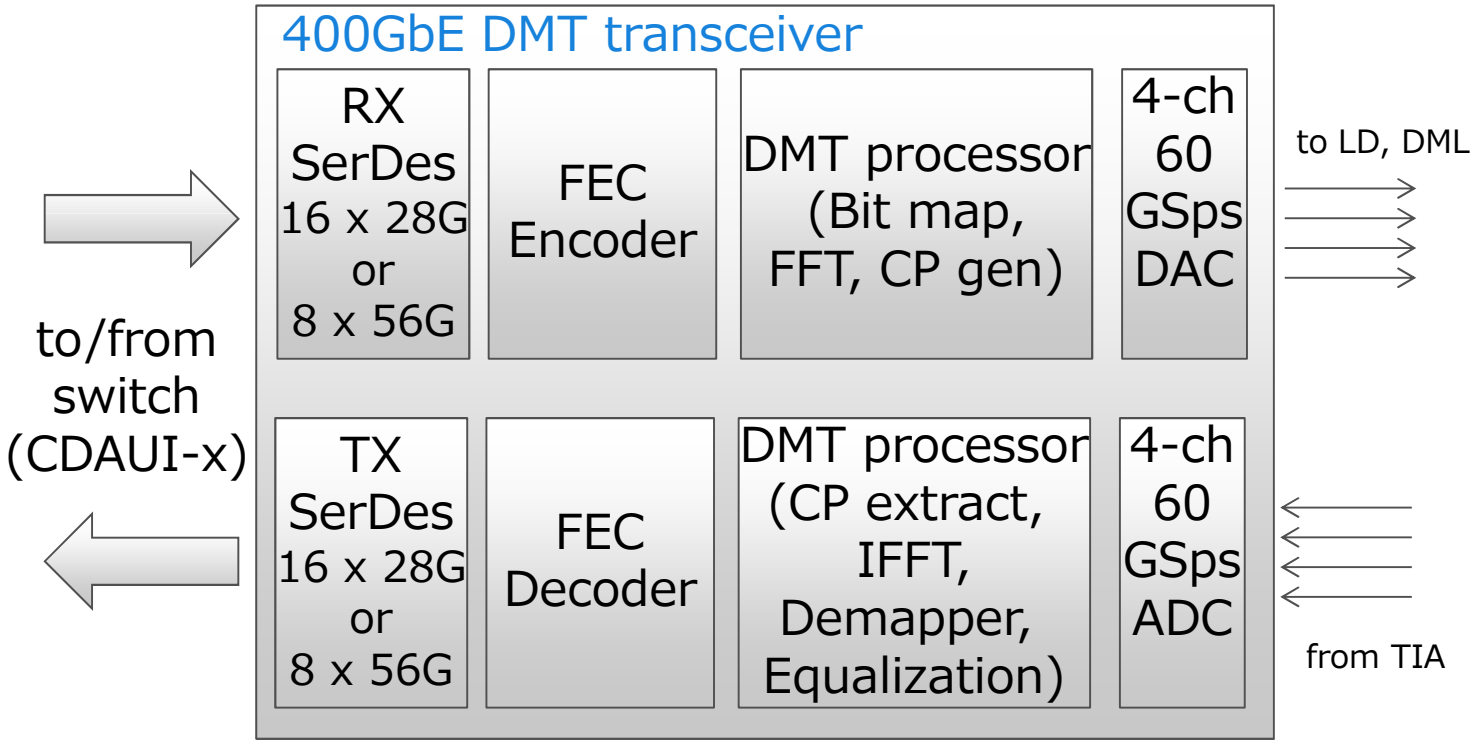


- DMT demodulation



400GbE DMT CMOS Transceiver Design

- Transceiver architecture feasibility study
  - Single, packaged device (23 x 23mm) for 400GbE
  - Power estimate*: 14W in 28nm, 7W in 14nm
  - DSP for DMT 1/10th order-of-magnitude compared to coherent DSP



*combination of silicon measurement and RTL-synthesis

400GbE System Implementation

400GbE module (LR4/ER4)

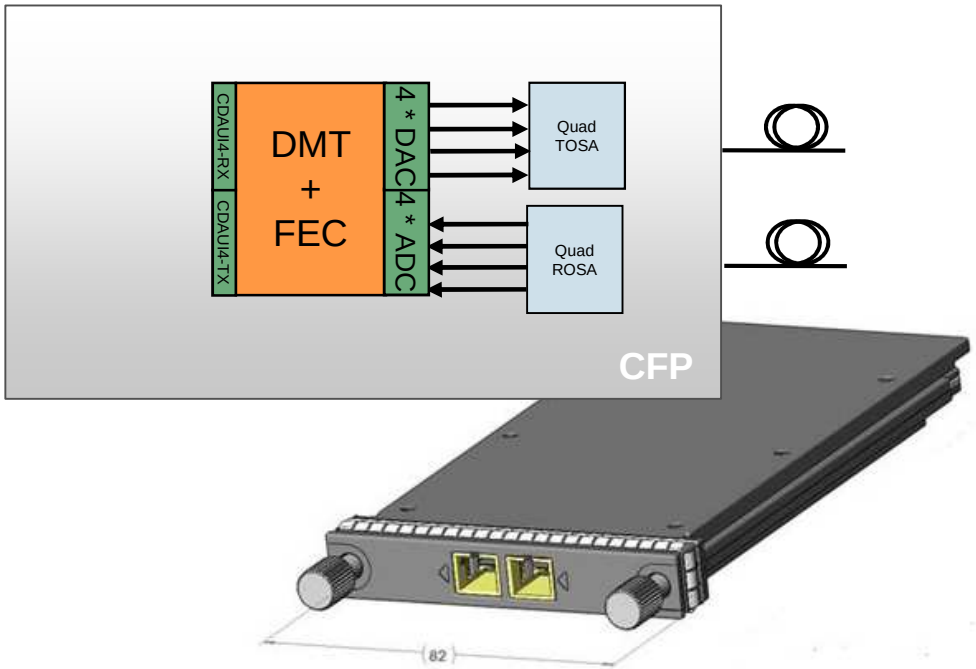
Mature CMOS process, 28nm

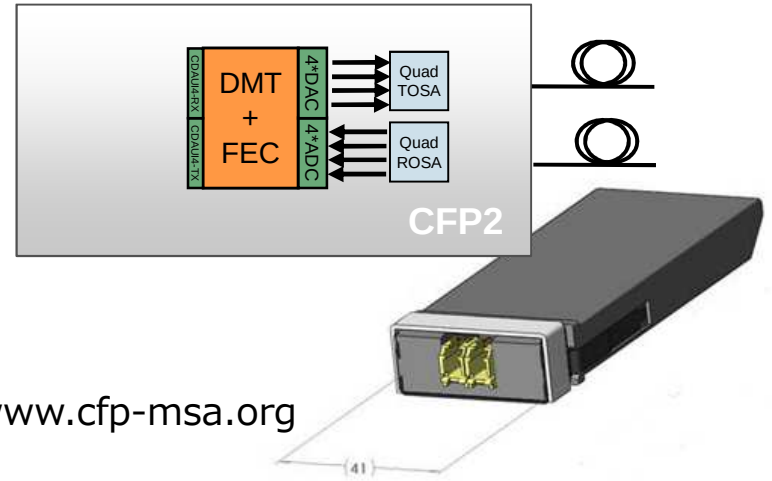
- **Power dissipation estimate:**
  - **14 W + optics**
- **CFP package power capability:**
  - **24-32 W**

400GbE module (LR4/ER4)

Next generation CMOS process, 14nm

- **Power dissipation estimate:**
  - **7 W + optics**
- **CFP2 package power capability:**
  - **12 W**





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Summary

- DMT is proposed as a candidate for 400G SG SMF PMD objectives
- Good feasibility of DMT technology for 400GbE
  - Based on feasibility study for a 400GbE DMT transceiver device in 28nm and smaller process geometries including
  - RTL synthesis for **low-complexity**, **low-power** DMT DSP
  - Package design options compatible with small form-factor optical modules

Thank you