
# Economic Feasibility of 400G Ethernet MAC/PCS/FEC

**January 2014 Indian Wells**

**Mark Gustlin - Xilinx**

# Context

This presentation addresses MAC/PCS feasibility from an FPGA perspective

## Economic Criteria: Supporting Presentations and Gaps (2)

- Known cost factors
  - Widespread presumption there could be extensive re-use of 100G PMDs "just use 4 of them" but:
    - What is the impact of the BER objective ?
    - Are there significant yield impacts upon 16 wide laser arrays cf to 10 or 4 wide arrays?
  - When supporting a 10km PMD, an approach that can use a single duplex fiber pair versus multiple pairs will likely be optimal (balanced costs)
    - Do we understand the cost of such an approach relative to widely known costs e.g. 100G SR10, LR4 or ER4 ?
  - 400G MAC and PCS functions are considered technically feasible ( there are presentations supporting this)
    - However do such potential implementations necessitate the use of the largest FPGAs or smallest available ASIC processes, such that the cost factor is significantly larger than 4x 100 ?

| Presentation | Comments |
|---|---|
| jewell_400_01_1113.pdf | MMF, 400G is equivalent to 4x100, then improves *Presenters Note: No discussion of "by 16 laser array yield"* |
| tanaka_400_01a_0913.pdf | 10km PMD *Presenters Note: Additional info available in takahara_01_0513_optx but relative cost is hard to determine* |
| welch_400_01_1113.pdf | 500m, 2km SMF module relative cost factors |
| | *Presenters Note: Need to address the impact of the BER objective?* |
| | *Presenters Note: MAC /PCS material?* |

5 | IEEE 802.3 400 Gb/s Ethernet Study Group

Economic Feasibility ad hoc conf call presentation
http://www.ieee802.org/3/400GSG/public/adhoc/econ_feas/moorwood_efa_01_14_0107.pdf

# Investigations Undertaken by Xilinx

- One building block of a 400GbE MAC is the CRC32 generation and checking logic
- Xilinx has done the work to show that 400G CRC32 generation/checking is feasible in today's FPGA technology
  - http://www.ethernetalliance.org/wp-content/uploads/2012/12/OFC-Ethernet-Alliance-talk-Brebner.pdf

## 400GbE CRC Prototype

ethernet alliance

- Results:

| Data bus word size | 1024-bit | 1536-bit | 2048-bit |
|---|---|---|---|
| Max clock frequency (MHz) | 400 | 381 | 326 |
| Maximum line rate (Gbps) | 409 | 585 | 668 |
| Latency (ns) | 17.5 | 18.4 | 21.5 |
| FPGA resources (slices) | 2,888 | 4,410 | 5,719 |

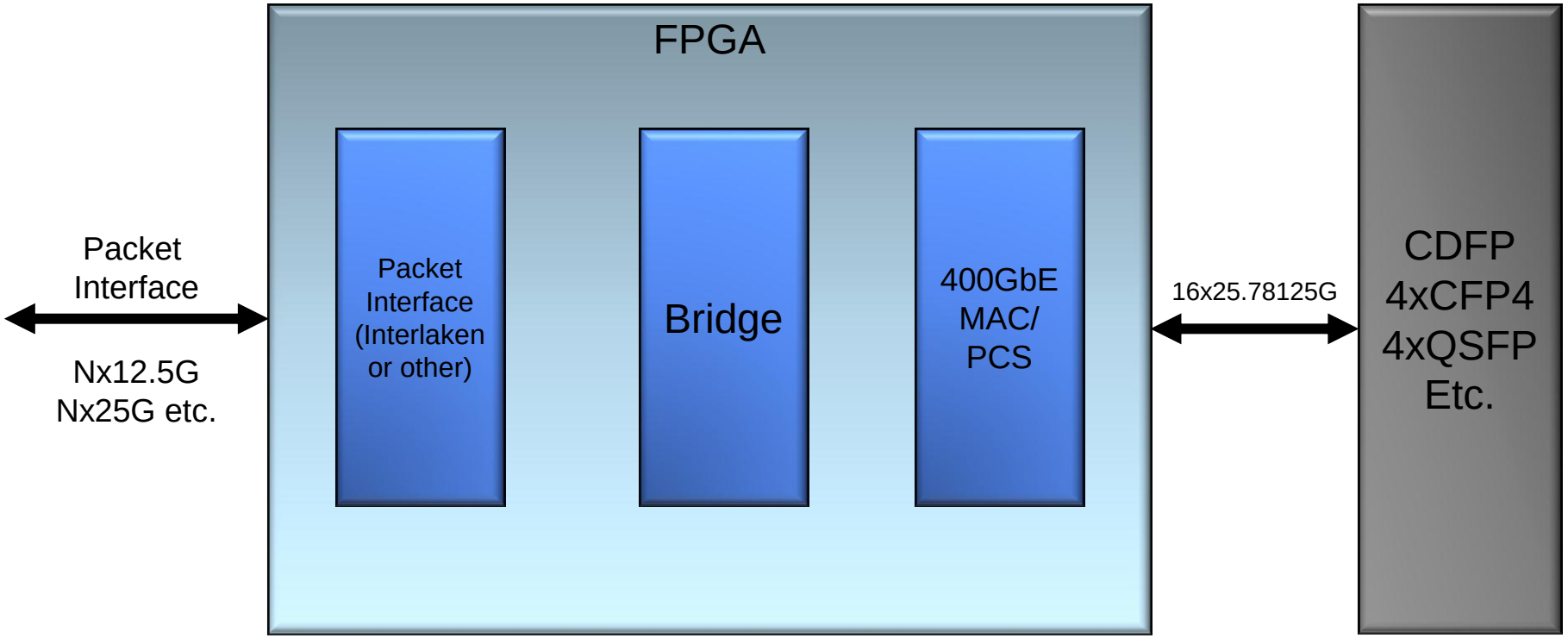
- 1024-bit width is feasible for 400GbE
- Other widths:
  - Less challenging clock frequencies
  - Demonstrate scalability beyond 400GbE

100G CRC32 ~ 1.3k Slices
400G CRC32 ~3k slices
400G = 2.3 x 100G

Logic "cost" of 400GbE is <= 4x100GbE

# FPGA Hardware for 400GbE

- FPGAs exist today that can support the presumed optical interface (28nm)
- There are devices today that support 16x25G SerDes plus nx13G SerDes as one example
- Can support 4x100GbE or 1x400GbE in the same device, cost of 1x400GbE should be at parity with 4x100GbE



# In Conclusion

- **If we assume similar complexity PCS and FEC schemes as those used in P802.3bm**
  - Then a 400GbE implementation could be realized in *<=4* times the logic of a 100GbE implementation
- **By the expected timeline of completion of this project (2H 2016?) a significant portion of FPGAs in 20 nm and below will be able to support these 400G functions in addition to other user logic**