

Opportunities for PAM4 Modulation

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- The objectives adopted by 400GbE SG include “at least 2 km over SMF” and “at least 10 km over SMF”.
- For 400GbE we will need a solution which provides the right balance between performance, cost, power and port density.

Adopted Objectives

- Support a MAC data rate of 400 Gb/s *
- Support a BER of better than or equal to 10^{-13} at the MAC/PLS service interface (or the frame loss ratio equivalent) ***
- Support full-duplex operation only *
- Preserve the Ethernet frame format utilizing the Ethernet MAC *
- Preserve minimum and maximum FrameSize of current Ethernet standard *
- Provide appropriate support for OTN *
- Specify optional Energy Efficient Ethernet (EEE) capability for 400 Gb/s PHYs *
- Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications **
- Provide physical layer specifications which support link distances of:
 - At least 100 m over MMF ***
 - At least 500 m over SMF ***
 - At least 2 km over SMF ***
 - At least 10 km over SMF ***

IEEE 802.3 400 Gb/s Ethernet Study Group

* Adopted by SG July 2013. Not approved by IEEE 802.3 WG
** Adopted by SG Sept 2013. Not approved by IEEE 802.3 WG
*** Adopted by SG Nov 2013. Not approved by IEEE 802.3WG

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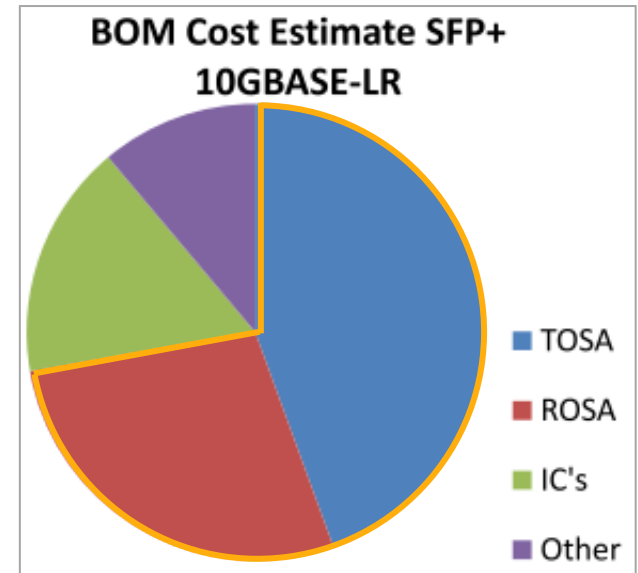
- This presentation acknowledges that increasing baud rate and/or number of lanes is not the preferred direction and considers some alternative approaches.

Options for 400GbE SMF Optical Interfaces

- According to the options listed in song_400_01_0513 there are several ways to increase the data rate to 400 Gb/s, starting from existing and proposed solutions for 100GbE and considering the objectives adopted by 400GbE:
 - Increase the number of optical wavelengths (WDM)
 - Increase the bandwidth per fiber or per lane
 - Increase the number of bits per symbol by introducing a Higher Order Modulation (HOM) format
- Both NRZ and HOM in combination with WDM are promising solutions for 400GbE, i.e. 16x25GBd NRZ, 8x50GBd NRZ, 8x25GBd HOM, 4x50GBd / 25GBd HOM etc.
- In order to limit the number of specification generations and to achieve the highest economically feasible device density for optical interfaces, we should try to reduce the number of lanes as much as possible, at least from 16 to 8 or even 4.
- We are focusing on HOM for 400GbE in this presentation.

High Order Modulation – Drivers

- According to BOM cost estimates for SFP+ 10GBASE-LR, most of the cost of an optical modules is due to the optics parts.
- For 400GbE it is expected that the dominant cost is due to optical component count (including optical coupling) and the associated RF packaging.
- “Reduction of number of components is key to achieve the lowest cost solution for data center application.” *Source: anderson_01_1111_NG100GOPTX*



Source: nowell_01_1111_NG100GOPTX

- One of the primary goals of using HOM is to move complexity into the electronics in a attempt to relax the requirements for the optics.
- The use of HOM is a promising method to reduce optical component count, relax the requirements for components (e.g. bandwidth) and get the right balance between performance, cost, power and density for different application scenarios.

High Order Modulation – What does it look like?

- High Order Modulation formats (HOM) in optics are not new and have been widely used for Line Side (Long Haul) over the past few years.
- But the requirement of HOM for Client Side is different from Line Side (Long Haul):
 - Client Side: (Testing) Cost, Power and Density.
 - Line Side: Spectral Efficiency and Performance, and minimum cost is not “essential”. High testing cost.
- By a limited introduction of HOM in Client Side modules, e.g. by using PAM4 with linear components and direct detection, we can minimize the increase of testing complexity, and thus cost, inherent to HOM.

Comparison	100G per port		400G per port	
	Line Side	Client Side	Line Side	Client Side
Modulation Format	DP-QPSK	NRZ	2 SC+PDM-16-QAM 1 SC+PDM-16-QAM ?	PAM4
Components	4x25GBaud	4x25GBaud	2SCx8x25GBaud 1SCx8x50GBaud ?	8x25GBaud 4x50GBaud

The Progress of PAM4 (1)

- Feasibility demonstrated in 802.3bj for PAM4 PHY implementation at the electrical layer; Usage of PAM4 in optics has been reported with VCSELs.
- 4-level pulse amplitude modulation (PAM4) of 850nm VCSELs has been reported in **PAPER 1** and **PAPER 2**. In **PAPER 1**, Chalmers University demonstrated **30Gb/s over 200m MMF** with real-time error measurement. In **PAPER 2**, **32Gb/s was demonstrated** by University of Cambridge with pre-distortion of the electrical signal to improve the VCSEL response.
- PAM4 to increase capacity per VCSEL was demonstrated in **PAPER 3** and **PAPER 4**. In this two papers the authors presented an experimental demonstration of high-speed 4-level pulse amplitude modulation on a 1.5 μ m VCSEL light source. **They achieved 50Gb/s per polarization by using PAM4 modulation**. PAM4, by either spatial or wavelength multiplexing, is a candidate solution to provide future standards capacity of 400Gb/s.

Paper 1: "30 Gbps 4-PAM transmission over 200m of MMF using an 850 nm VCSEL", ECOC 2011.

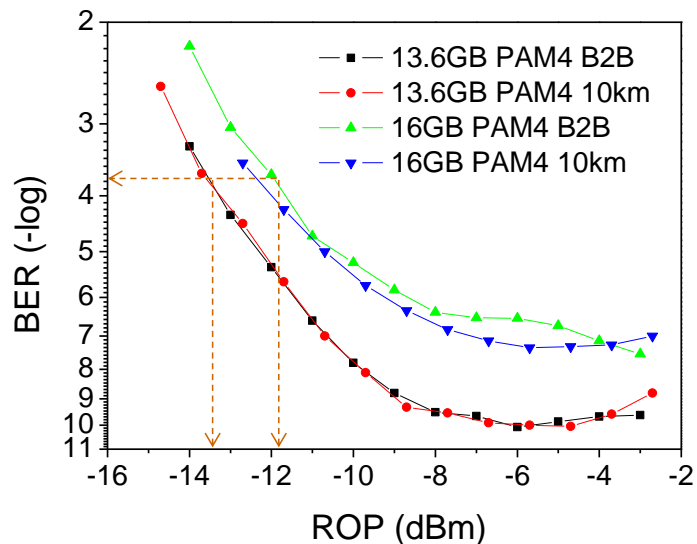
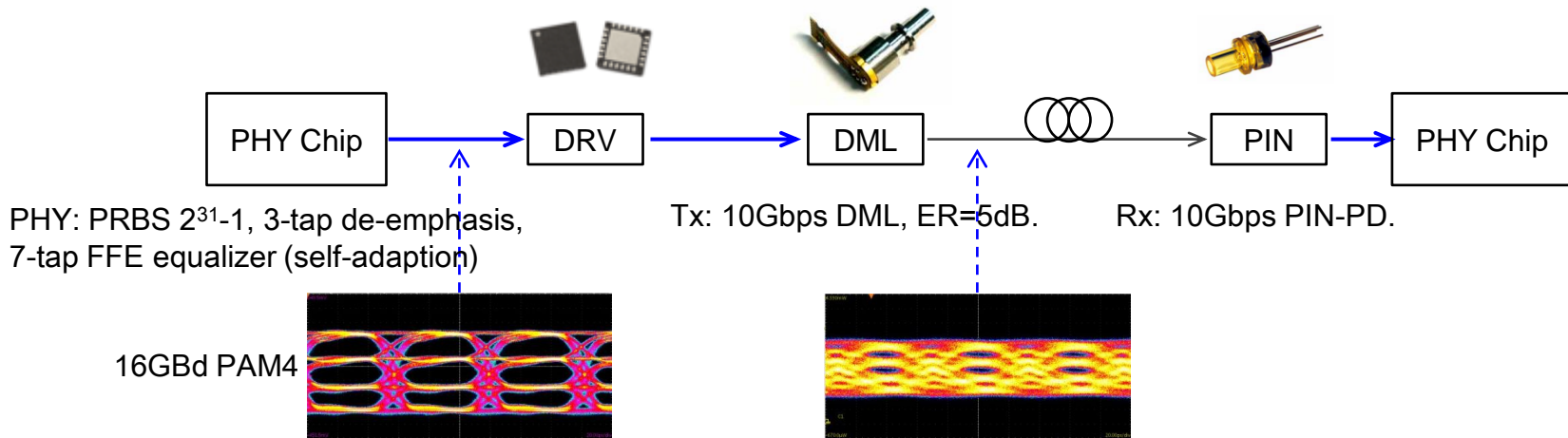
Paper 2: "32 Gb/s multilevel modulation of an 850nm VCSEL for next-generation data communication standards", CLEO 2011.

Paper 3: "100 Gb/s single VCSEL data transmission link" OFC 2012.

Paper 4: "High-speed 1550 nm VCSEL data transmission link employing 25 Gbaud 4-PAM modulation and Hard Decision Forward Error Correction" IEEE Journal of Lightwave Technology, vol. 31, no 4, pp. 689-695, 2013.

The Progress of PAM4 (2)

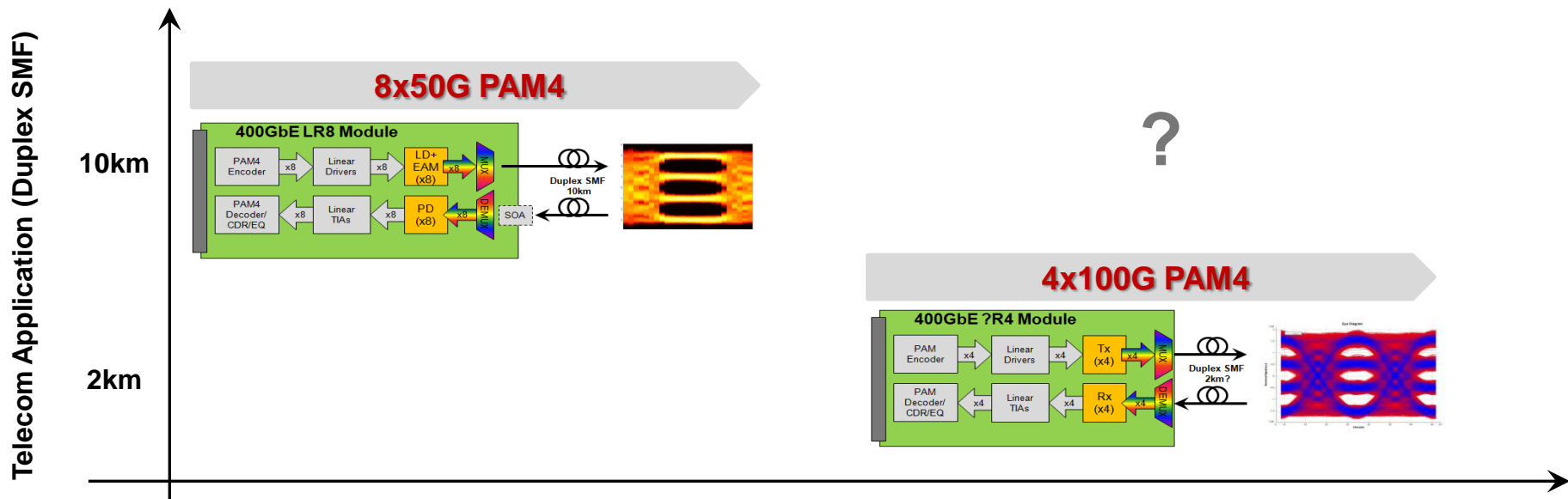
- Experimental results of 16GBaud PAM4 B2B & 10km SMF



- W/ FFE, 13.6GBd PAM4 BER error floor reach $1e-10 \sim 1e-11$.
- PAM4 Sensitivity: $-13.5\text{dBm}@13.6\text{GBd}$.
- PAM4 Sensitivity: $-11.8\text{dBm}@16\text{GBd}$.

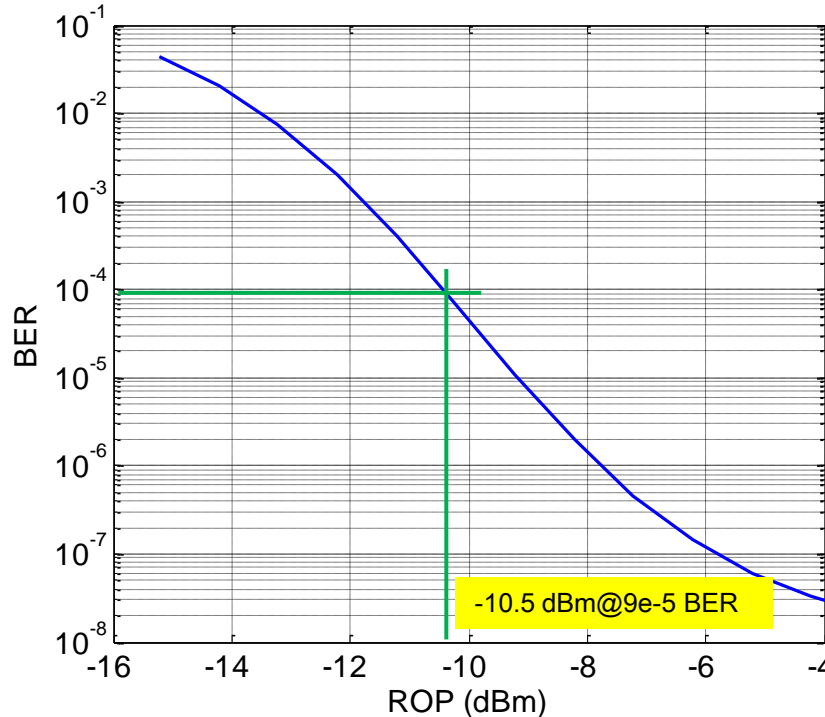
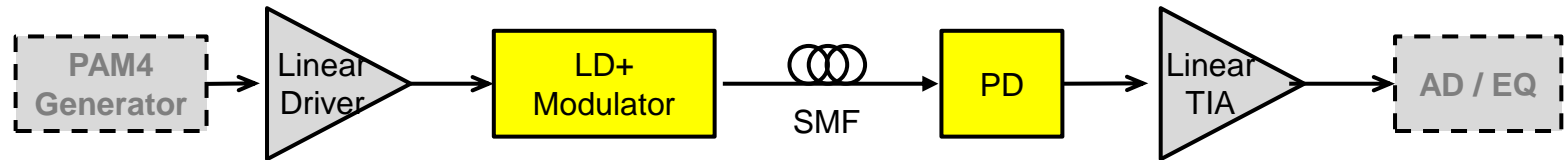
The Opportunities of PAM4

- To satisfy the objectives adopted by 400GbE SG, “at least 2km over SMF” and “at least 10km over SMF”, solutions using low bandwidth components and fewer optical channels will be promising candidates.
- To enable a quick time to the market a 8x50Gbps / 56Gbps PAM4 architecture, using mature 25Gbps / 28Gbps platforms and leveraging the technology of 100GbE generations, may be a promising candidate to satisfy the 10km SMF objective.
- In order to achieve a significantly lower cost 2km PMD we would like to investigate the possibility of a 4-lane solution based upon a 4x100Gbps PAM4 architecture, which with adequate performance should be a promising candidate solution for 2km SMF applications.



The BER Simulation of 8 Channels PAM4 (10km)

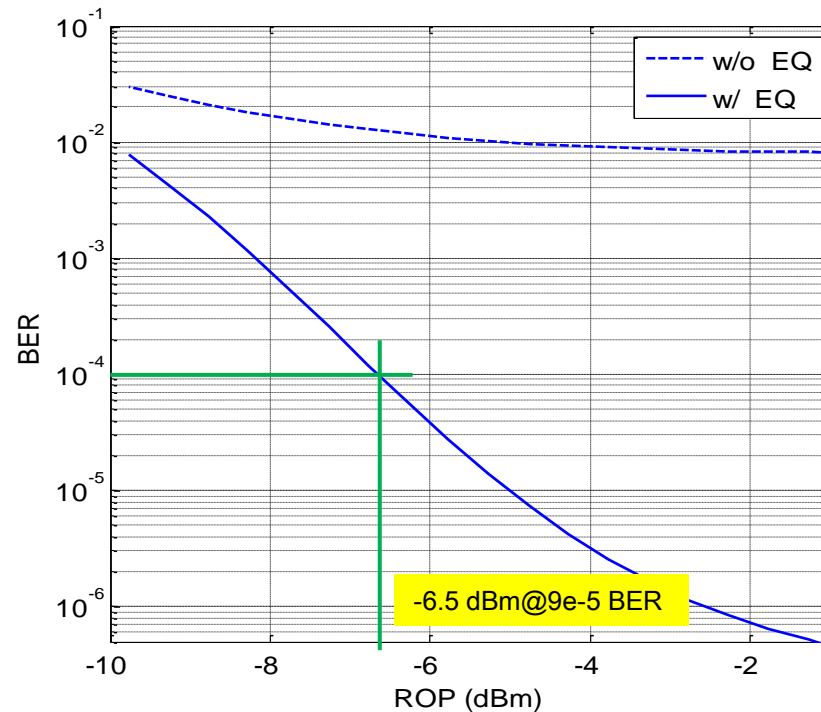
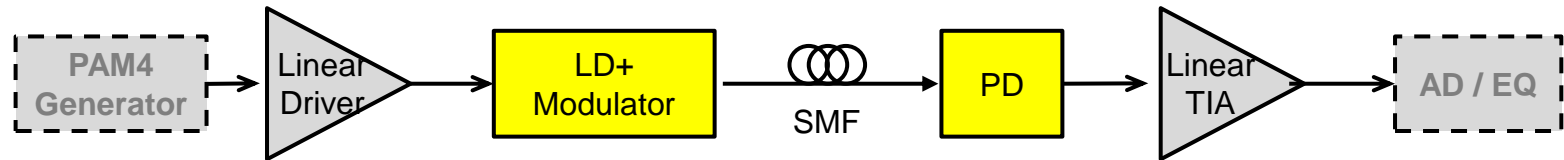
- Assumption: Rate = 28 GBaud, RJ = 300 fs, Bandwidth of Tx and Rx = 22 GHz, Tx SNR (after driver) = 21 dB, ER = 7 dB, RIN = -145 dB/Hz, Thermal Noise = 15 pA/ $\sqrt{\text{Hz}}$ for 28 Gbps components, Responsivity = 0.9 A/W.



Simulation Software: VPI Version 8.6

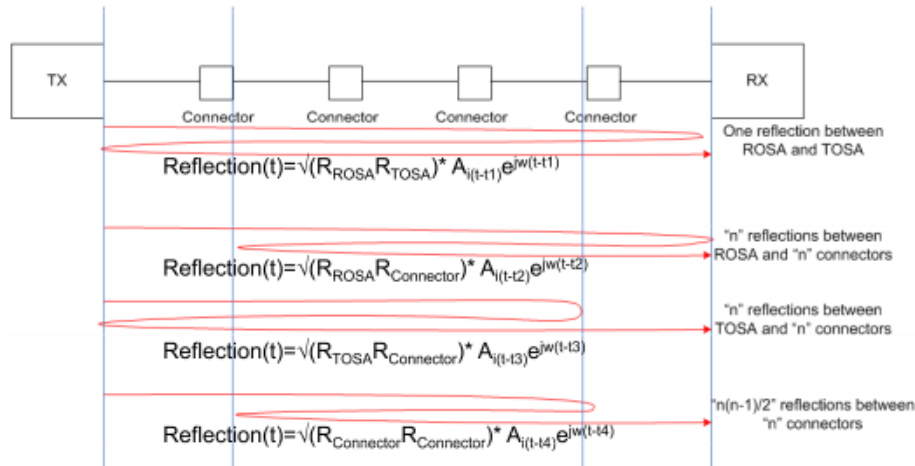
The BER Simulation of 4 Channels PAM4 (2km)

- Assumption: Rate = 56 GBaud, RJ = 300 fs, Bandwidth of Tx and Rx = 32 GHz, Tx SNR (after driver) = 21 dB, ER = 6 dB, RIN = -145 dB/Hz, Thermal Noise = 30 pA/ $\sqrt{\text{Hz}}$ for 40 Gbps components, Responsivity = 0.9 A/W.



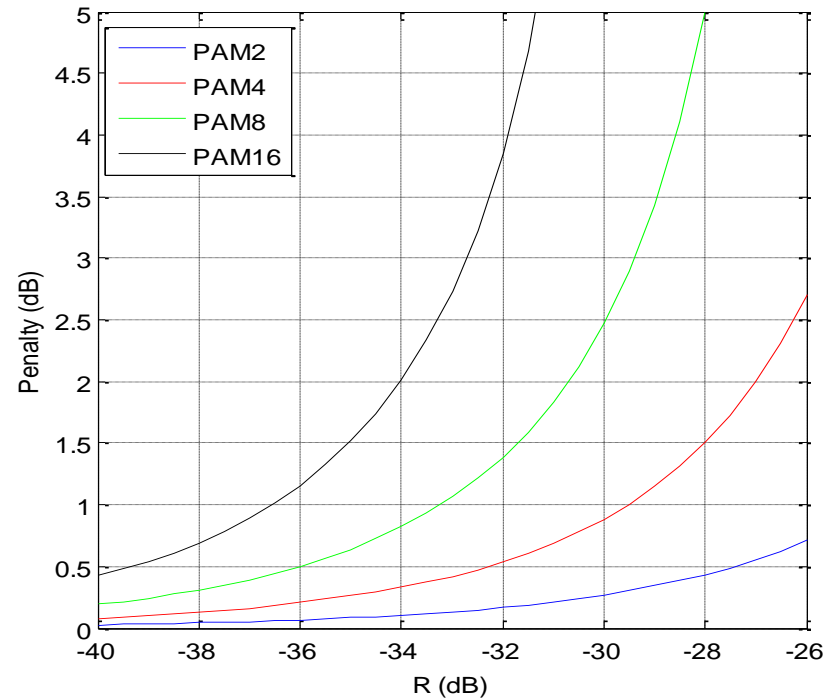
Simulation Software: VPI Version 8.6

The Analysis of PAM4 (1) --- RL / MPI Analysis



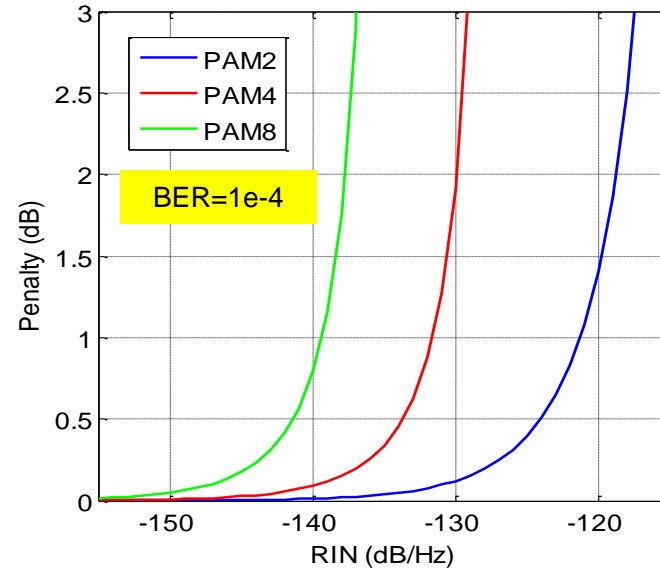
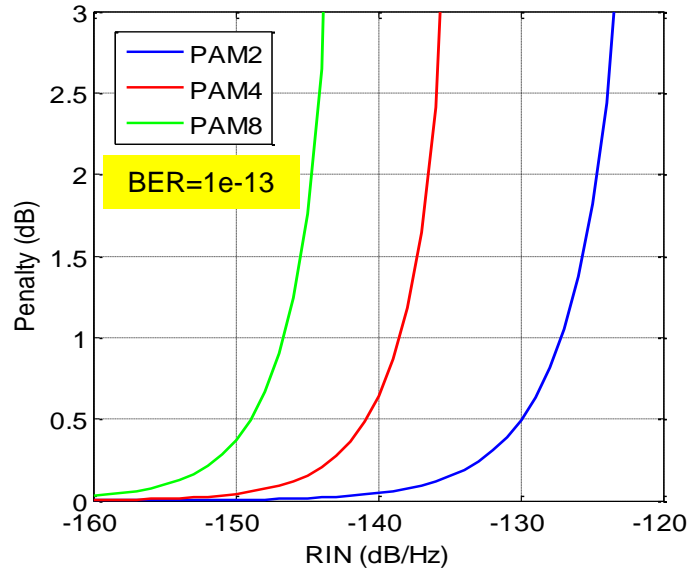
Source: farhood_01_1112_optx

- Modeling MPI as vertical eye reduction penalty, with some pessimistic assumptions and then calculate the MPI as an amplitude dependent closure of the signal eye for PAM.



- We assumed that the connector Return Loss (RL), TOSA RL and ROSA RL are close to each other, for example setting $R_{TOSA} = R_{ROSA} = R_{Connector} = R$.
- Refer to 802.3ba standard, "... this allocation supports four connections with an average insertion loss per connection of 0.5dB". Keep in mind that the more connectors the more the MPI impact, so the use of 4 connectors is a reasonable assumption here.
- Using 4 connectors and 6dB ER, attached graph shows level dependent MPI penalty. Considering 0.5dB penalty, the requirements of reflection from connectors and devices will be more stringent than PAM2: -27.5dB, PAM4: -32.5dB, PAM8: -36dB, PAM16: -39.5dB.

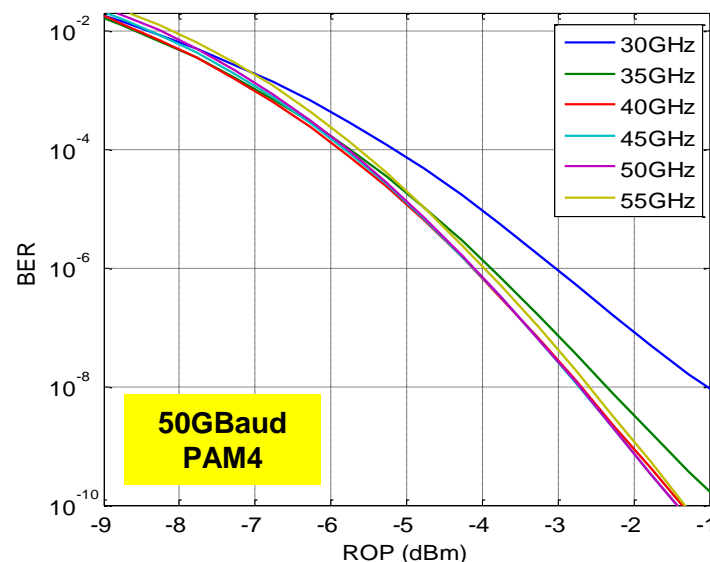
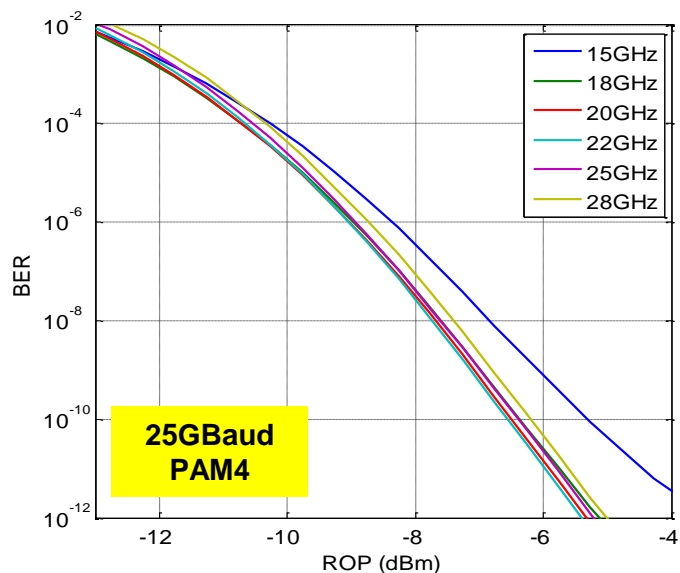
The Analysis of PAM4 (2) --- RIN Analysis



- Noise from RIN depends upon the level of PAM, in a binary signal, the 1's have RIN, 0's have no RIN (for infinite extinction), the influence of ER is ignored in this analysis.
- Assumptions: Bandwidth=20GHz, ER=100dB (ER is ignored in this analysis).

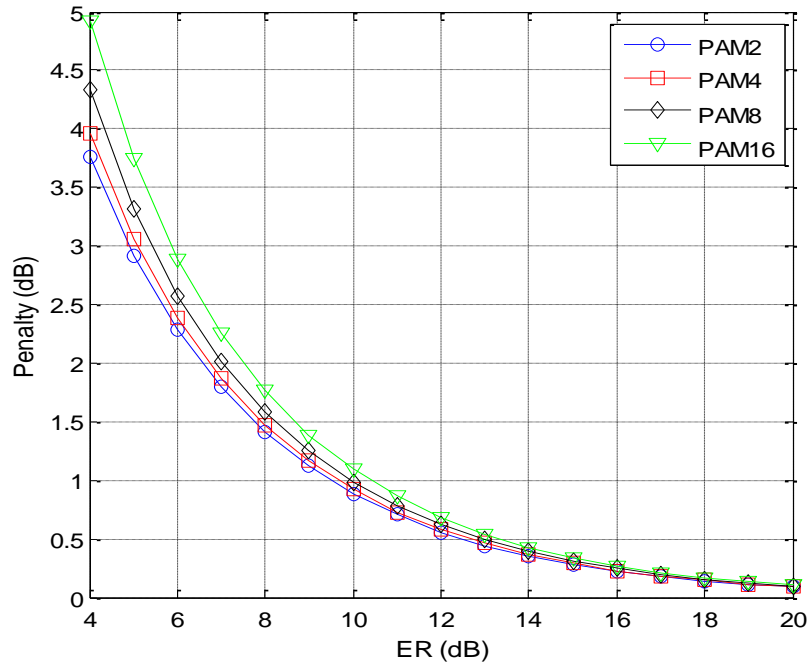
PAMn	RIN @ Power Penalty=0.5dB
n=2@1e-13	<= -130 dB/Hz
n=4@1e-13	<= -141 dB/Hz
n=8@1e-13	<= -148 dB/Hz
n=2@1e-4	<= -125 dB/Hz
n=4@1e-4	<= -134 dB/Hz
n=8@1e-4	<= -142 dB/Hz

The Analysis of PAM4 (3) --- Receiver Bandwidth Analysis



- Assumptions: 25GBaud and 50GBaud, Responsivity=0.9A/W, TIA Noise=20pA/Hz^{1/2} @22GHz and 40pA/Hz^{1/2} @40GHz, RIN=-145dB/Hz, ER=6dB, Tx Noise=30dB.
- Higher order modulation schemes are more sensitive to receiver bandwidth, the sweet spot of bandwidth can be found.
- For 25GBaud PAM4, under the simulation conditions above, the “best bandwidth” is about 22GHz, for 50GBaud PAM4, the “sweet spot” is about 40GHz.

The Analysis of PAM4 (4) --- Extinction Ratio Analysis



- Assumptions: 25GBaud, Responsivity=1A/W, Thermal Noise=20pA/Hz^{1/2}.

- Similar to PAM2, PAM4 modulation formats have sensitivity to ER, for different transmitter components, the typical ER is: DML TOSA 4~6dB, EML TOSA 6~8dB.
- If ER>12dB, the difference of penalties between different multi-level modulation formats can be neglected.

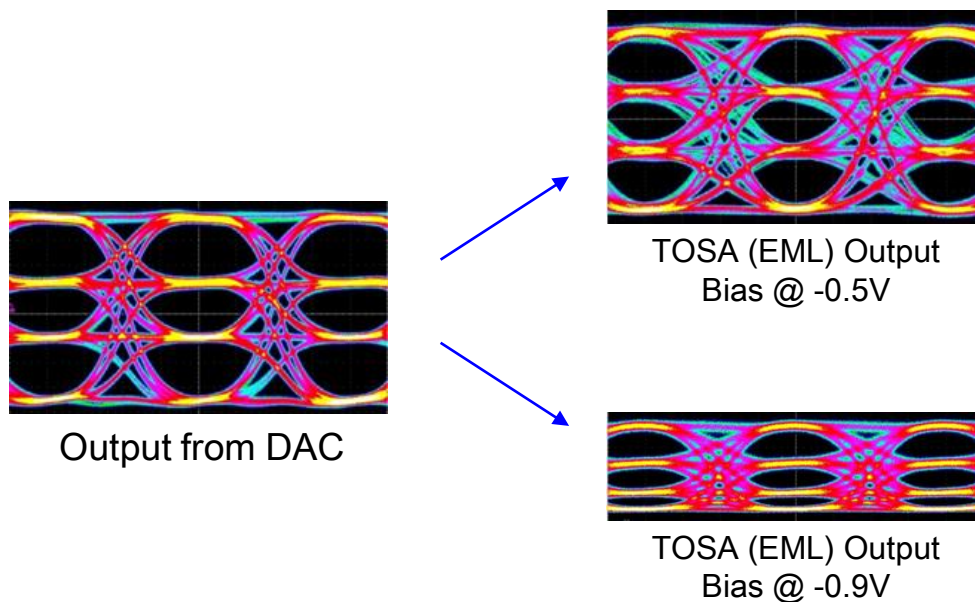
The Analysis of PAM4 (5) --- Linearity Analysis (Background)

- According to RF and microwave fiber-optic design guide, the linearity limit is usually specified by the 1dB compression or the third-order intercept.
- Third-order intercept (TOI): a specification used to characterize the small signal nonlinearity of an RF device. An extrapolation of the results of a small signal two-tone test to the point where the level of the third-order intermodulation would be equal to that of the two tones.
- 1dB Compression: refers to the nonlinear behavior of the RF device. As the input RF power is increased, the output power increases by less and less. When the output power is 1dB lower than it would be if the device were perfectly linear, the device is said to be operating at its 1dB compression point.
- Total Harmonic Distortion (THD): THD was adopted as one of the O/E properties of coherent receivers in OIF. It is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency, which is used to characterize the linearity of microwave devices.

Source: <http://jencotech.com/news/DesignGuide.pdf>

Source: IA # OIF-DPC-RX-01.2

The Analysis of PAM4 (5) --- Linearity Analysis



- With the same output performance from the DAC, the optical performance will be subject to working conditions (e.g. bias etc) of components.
- For HOM formats, non-linearity phenomenon may be observed from the eye diagram; How to evaluate this spec of optical interface will be a problem, e.g. introducing the “Parent Eye” and “Child Eye” for different levels (PAM4)? Introducing similar evaluation method like RF and microwave? ...

Summary

- ❑ According to BOM cost estimates for 10GBASE-LR implementations, it is expected that most of the cost of an optical module is due to the optics.
- ❑ For 400GbE the usage of PAM is a promising method to reduce the component count, relax the requirement of components and move complexity into the electronics (to simplify the requirements for the optics).
- ❑ Because HOM complexity and challenges increase rapidly for higher orders, we must be careful to find the right balance between complexity, performance and cost.
- ❑ Our investigations show that PAM4 is an promising solution.
- ❑ Results from simulations and experiments (at lower speeds) indicate that we need to consider several factors when introducing PAM4.
- ❑ Further experimental work (e.g. eye closure penalties, SNR performance, available loss budget) is needed to confirm simulations and performance requirements.

Future Works

- ❑ Consider the requirement of link budget for different applications.
- ❑ Technical Feasibility (TF)
 - ✓ Carry out experiments on PAM4 system to demonstrate the TF.
 - ✓ Analyze the TF of PAM4 via testing, modeling, simulation, etc, and find out the source of penalty according to the comparison of theoretical simulations and experiments.
 - ✓ The compensation method of the penalty i.e. FEC, EQ etc.
 - ✓ Consider the architecture of transmitter and receiver components.

Thank you