Darshan_04_0917.pdf (PSE state machine **Part A**- Using CLASS_PROBE in Figure 145-15/16***)***

Comment (i-198, i-269, i-406)

Some PSE architectures are generating sequences of detection + classification events and waiting for the host to decide when to power on the port. This require the class probe functionality and exit to IDLE in the classification state machines (for single-signature and dual-signature). Single-signature has global pse_reset input to IDLE so in this case, PSE can go to IDLE at any time. It is not the case in dual-signature.

As a result, we need to:

(1) Add CLASS_PROBE_PRI/SEC functionality for primary and secondary.

(2) Add global exit to IDLE_PRI/SEC by using pse_reset_pri/sec by changing the input to IDLE_PRI to sism*(iclass_lim_det_pri+pse_reset_pri) it will do two things: pse_reset_pri and multi-true issue with IDLE_PRI and ENTRY_PRI. To implement same changes for secondary.

Notes: There are additional two issues that will be addressed separately:

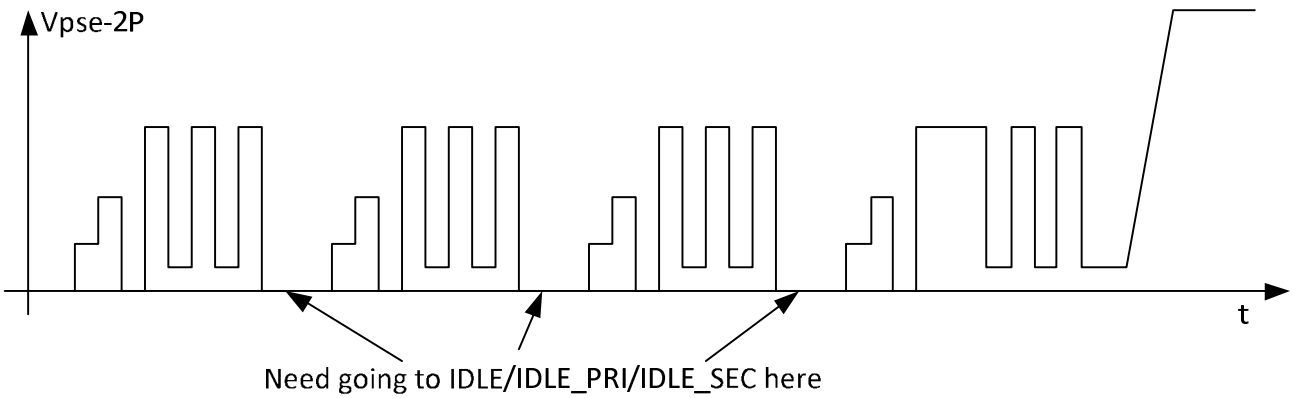
a) Currently, in the state machine, finding the class code by issuing 3 class events and finding 4PID done by separate process that do the same process and with the same reliability and confidence. This redundancy which cause using twice the long class event timer. This will be address in darshan_14_0917.pdf.

b) There is an issue that cause the state machine to be stuck in ENTRY_SEC in case primary detection has failed or dtet_timer_pri_done.

In addition, in the transition from IDLE_SEC to START_DETECT_SEC when pwr_app_pri=0 we stuck in IDLE_SEC if in (CC_DET_SEC=3) and det_star_pri=0 due to invalid_sig once or didn't start yet.

This will also prevent doing cycles of detection + classification.

See proposed solutions in darshan_13_0917.pdf.



Baseline starts here

Proposed Remedy

1. Make the following changes to the pse_reset variable definition:

pse_reset

Controls the resetting of the PSE state diagram (Figure 145-13). Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.

Values:

FALSE: Do not reset the PSE state diagram.

TRUE: Reset the PSE state diagram.

2. Add the following variables to 145.2.5.4

pse_reset_pri

Controls the resetting of the PSE state diagram on Alternative A (Figure 145-15). Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE Alternative A functionality.

Values:

FALSE: Do not reset the PSE state diagram.

TRUE: Reset the PSE state diagram.

pse_reset_sec

Controls the resetting of the PSE state diagram on Alternative B (Figure 145-16). Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE Alternative B functionality.

Values:

FALSE: Do not reset the PSE state diagram.

TRUE: Reset the PSE state diagram.

option_class_probe_sec

This variable indicates if the PSE should determine the PD requested Class when pse_avail_pwr_sec is less than 4. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying VReset for at least TReset to the PI (see Table 145– 14), followed by a normal classification procedure.

Values:

FALSE: The PSE will not probe for the PD requested Class.

TRUE: The PSE probes for the PD requested Class.

option_class_probe_pri

This variable indicates if the PSE should determine the PD requested Class when pse_avail_pwr_pri is less than 4. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying VReset for at least TReset to the PI (see Table 145– 14), followed by a normal classification procedure.

Values:

FALSE: The PSE will not probe for the PD requested Class.

TRUE: The PSE probes for the PD requested Class.

3. Add the following functions to 145.2.5.6

do_class_probe_pri

This function discovers the dual_signature PD requested Class by producing a number of class events on the primary alternative. The class events produced are limited to CLASS_EV1_LCE_PRI to MARK_EV3_PRI. The tlce_timer_pri in CLASS_EV1_LCE_PRI may be replaced with the tcle2_timer_pri to allow abbreviated class timing duration. This function returns the following variables:

pd_req_pwr_pri: This variable contains the dual-signature PD requested Class per Table 145-25.

Values:

1: Class 1

2: Class 2

3: Class 3

4: Class 4

5: Class 5

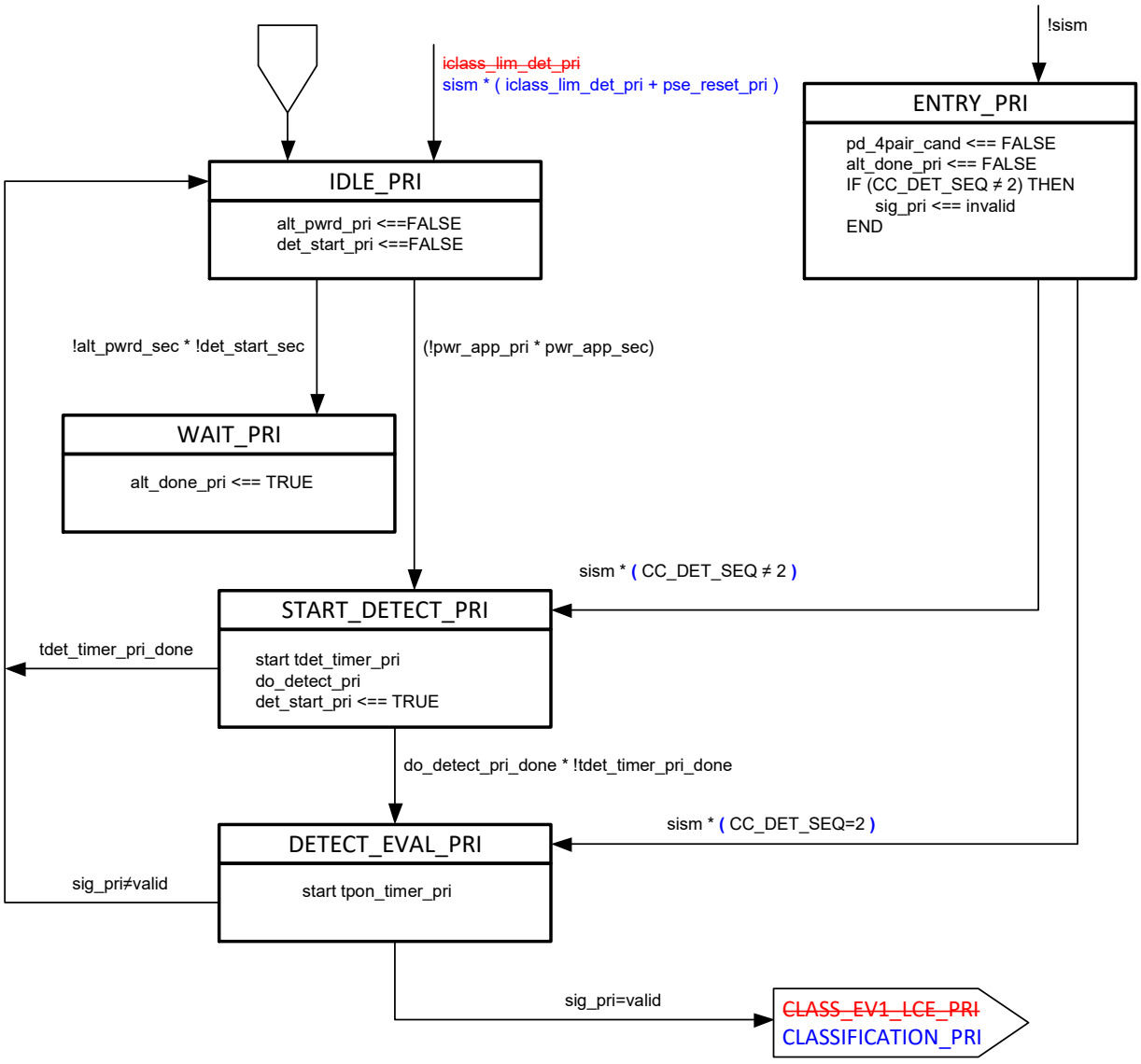
do_class_probe_sec

This functions discovers the dual_signature PD requested Class by producing a number of class events on the secondary alternative. The class events produced are limited to CLASS_EV1_LCE_SEC to MARK_EV3_SEC. The tlce_timer_sec in CLASS_EV1_LCE_SEC may be replaced with the tcle2_timer_sec to allow abbreviated class timing duration. This function returns the following variables:
pd_req_pwr_sec: This variable contains the dual-signature PD requested Class per Table 145-25.
Values:

1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5

4. *Make the following changes to the state machine in page 132*

Note part of the baseline
Global pse_reset_pri was inserted in the same way we did for single-signature. *The variable sism was added as a condition for both iclass_lim_det_pri and pse_reset_pri. From logical operation point of view, sism is not required as a condition for iclass_lim_det_pri since iclass_lim_det_pri =TRUE only if we have do_classification_pri which can happen only if sism=TRUE, however we keep it as proposed for now until confirmation from simulation.*



5. Make the following changes to Figure 145-15 page 133

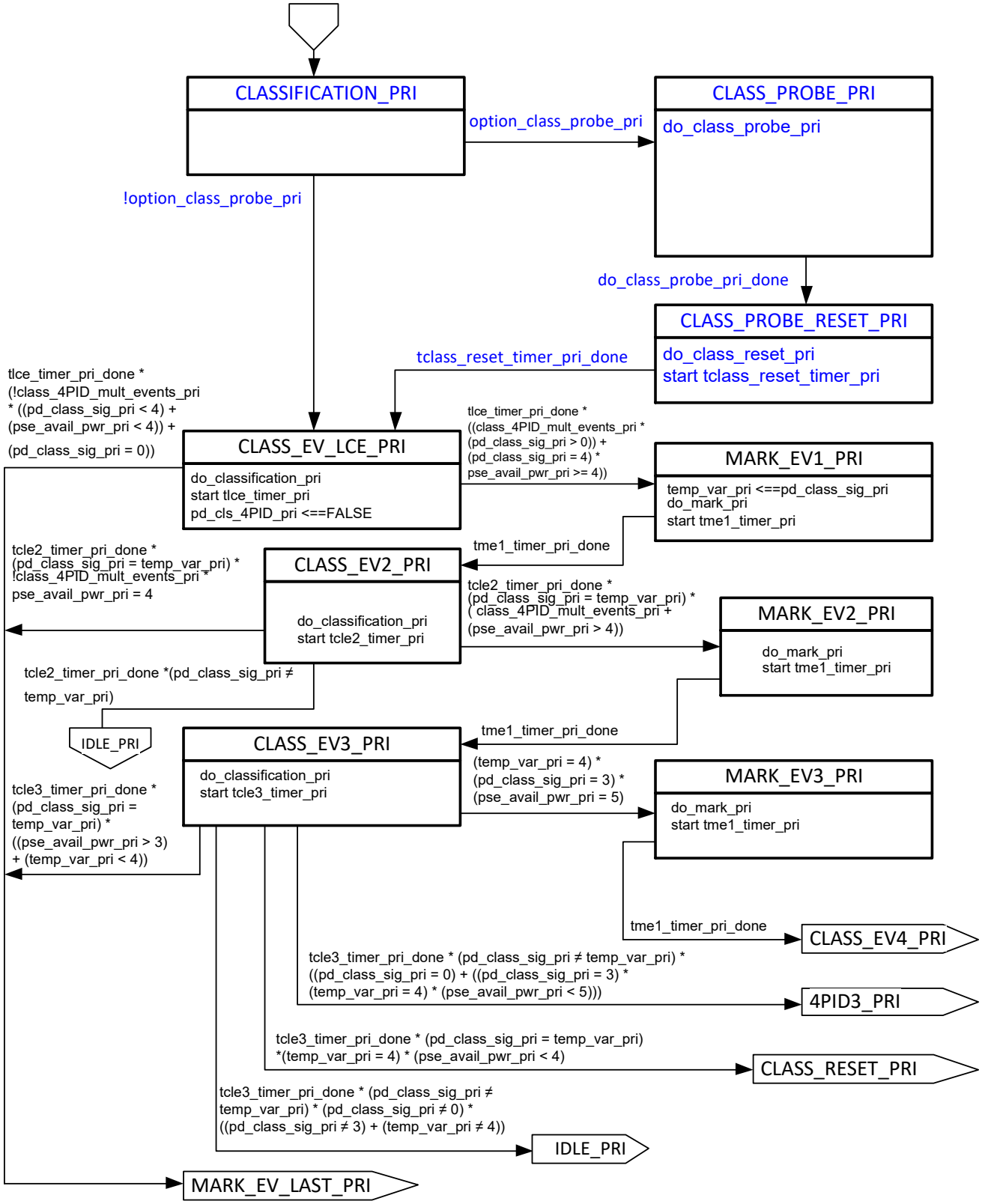
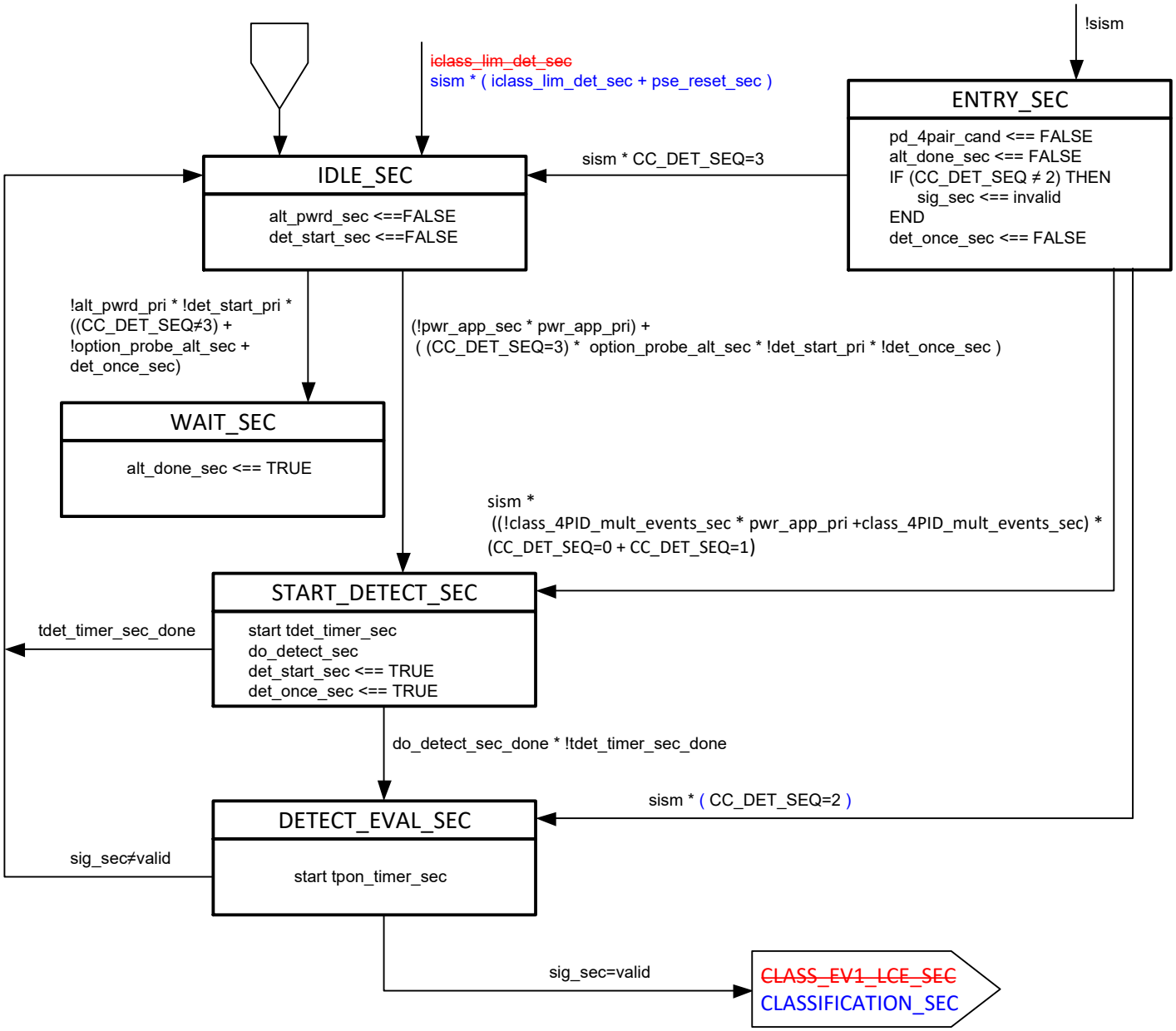


Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram (continued)

6. *Make the following changes to the state machine in page 136*



7. Make the following changes to Figure 145-15 pages 137

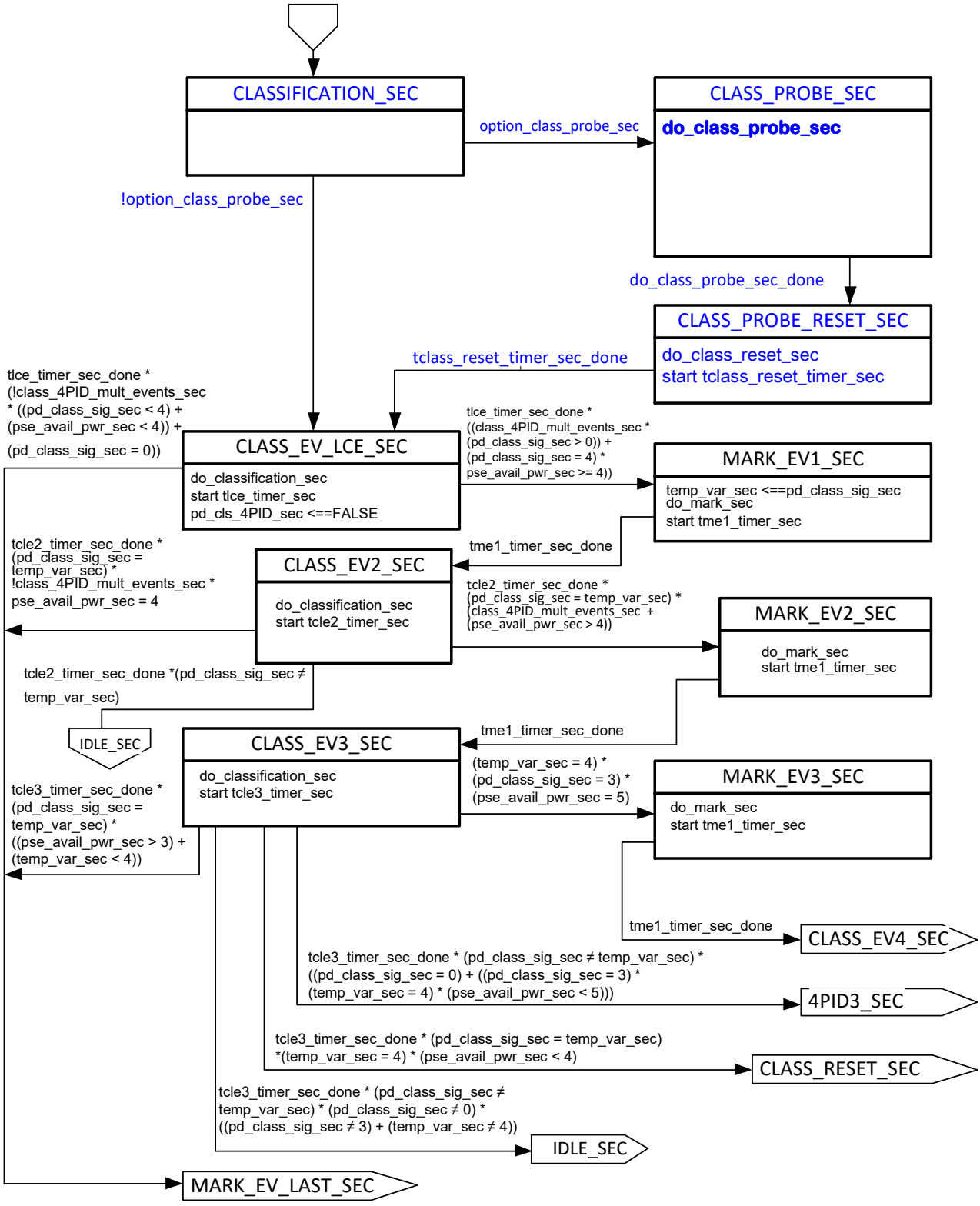


Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram (continued)

End of Baseline