Resistive Imbalance Specification Issues and Limitations

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Resistive Imbalance Ad Hoc

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Overview

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- A goal of the Ad Hoc has been to determine and limit Current Imbalance by specifying behavior of each contributing element (PSE, Channel, PD)
  - Current imbalance would be used to determine max. current per pair
- Based upon a basic implementation
  - Single PD (Bridge outputs tied together)
  - Single-source PSE
  - No balance correction
- Resistive Imbalance is the parameter used for the Channel, and has been suggested as a specification requirement for the PSE and PD Interfaces
- Limitations of this method are presented herein

System Imbalance

- **The following is a Resistive imbalance equation for determining current imbalance between pairs (Single source, single PD)**

$$\frac{\sum R_{max} - \sum R_{min}}{\sum (R_{max} + R_{min})}$$

- **This can be separated into contributions of the PSE, PD and Channel:**

$$\frac{R_{pseRmax} - R_{pseRmin}}{\sum (R_{max} + R_{min})} + \frac{R_{CableRmax} - R_{CableRmin}}{\sum (R_{max} + R_{min})} + \frac{R_{pdRmax} - R_{pdRmin}}{\sum (R_{max} + R_{min})}$$

PI Imbalance Specification Problem

- The contribution of each is dependent upon the overall resistance
  - PSE PI Runbalance contribution is not the same as PSE PI Runbalance

$$\frac{R_{pseRmax}-R_{pseRmin}}{\sum(R_{max}+R_{min})} \neq \frac{R_{pseRmax}-R_{pseRmin}}{R_{pseRmax}+R_{pseRmin}}$$

  - PD PI Runbalance contribution is not the same as PD PI Runbalance

$$\frac{R_{pdRmax}-R_{pdRmin}}{\sum(R_{max}+R_{min})} \neq \frac{R_{pdRmax}-R_{pdRmin}}{R_{pdRmax}+R_{pdRmin}}$$

- Changes in total resistance can change derived Runbalance requirements for either or both PIs
  - An Runbalance spec at the PSE PI and PD PI will not directly correlate with current imbalance

PSE Runbalance Calculation, Simulation

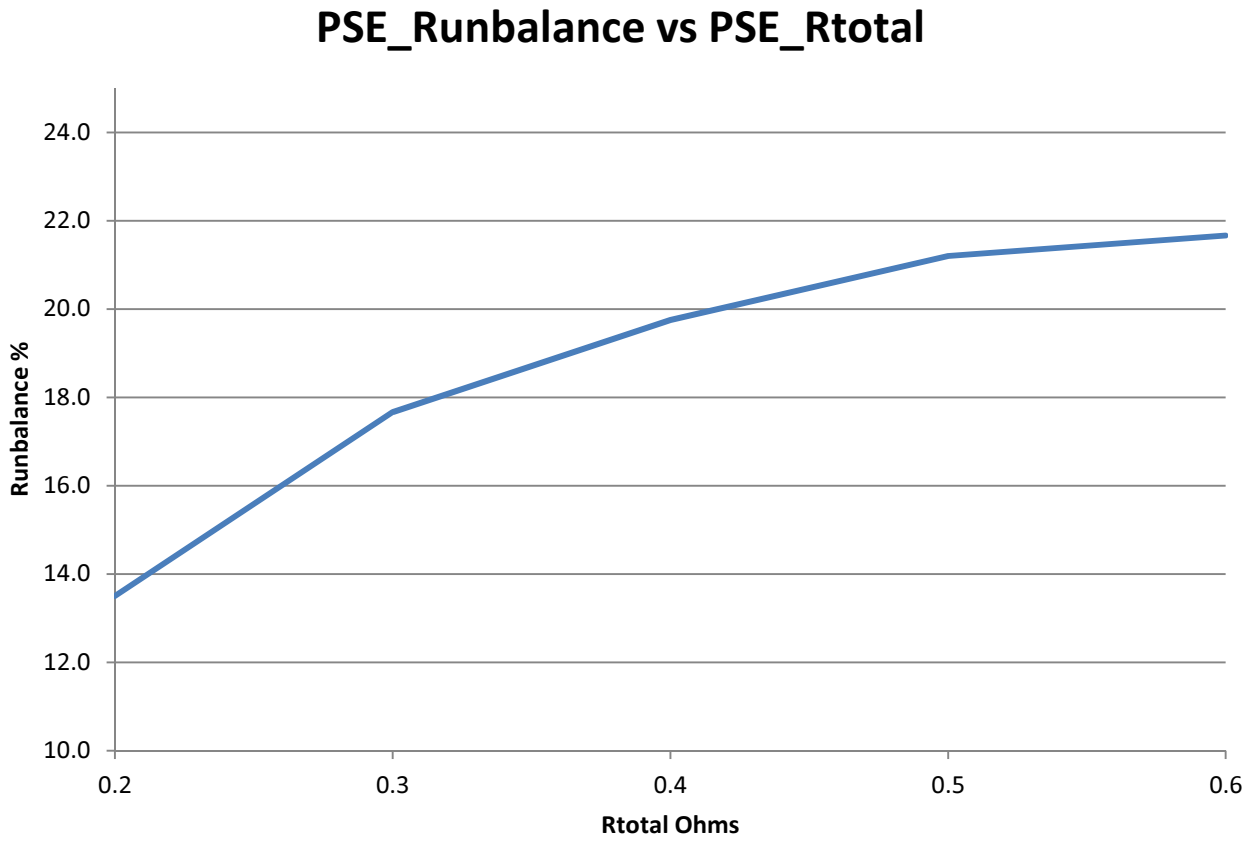
- **Simulation Conditions common to each:**
  - **~1M Cable, worst case model used to arrive at ~26%**
  - **PD with Diode Bridge**
  - **PD, Channel fixed, PSE varied**

	PSE Runbal		Channel		PD Runbal	
Rpse other	0.001	0.001				
Rtrans	0.06	0.065				
Rconn	0.015	0.03	0.015	0.03		
Wire			0.0275	0.0285		
Rconn			0.015	0.03	0.015	0.03
Rtrans					0.06	0.065
Rdiode					0.8557	1.537
Unbalance	0.1163	12%	0.2123	21%	0.2737	27%
System Runbalance						
	0.26115	26.1%				
Simulation Iunbalance Result						
(mA)	658.35	385.65	0.261207	26.1%		

	PSE Runbal		Channel		PD Runbal	
Rpse other	0.23	0.392				
Rtrans	0.06	0.065				
Rconn	0.015	0.03	0.015	0.03		
Wire			0.0275	0.0285		
Rconn			0.015	0.03	0.015	0.03
Rtrans					0.06	0.065
Rdiode					0.8557	1.537
Unbalance	0.2298	23%	0.2123	21%	0.2737	27%
System Runbalance						
	0.26118	26.1%				
Simulation Iunbalance Result						
(mA)	658.35	385.65	0.261207	26.1%		

PSE Runbalance can vary significantly for a fixed total Runbalance

PSE Runbalance Requirement VS PSE total resistance (Channel, PD, and System Runbalance unchanged)



PD Simulation of Diode vs FET bridge

- **Simulation Conditions common to each:**
  - PSE, Channel (~1M Cable), from worst case models, held constant
  - System Imbalance = 26.12%
- **Diode Case:**
  - 26.12% Iunbalance in simulation
  - Vdiode/Idiode + Rtransf + Rconn → $\frac{R_{pdRmax}-R_{pdRmin}}{R_{pdRmax}+R_{pdRmin}}$
    - Result: 27.45% PD PI Runbalance
- **FET Case:**
  - Simulations used to arrive at 26.12% Iunbalance
  - FET resistances: .04 min and 1.45 max Ohms
  - Rds + Rtransf + Rconn → $\frac{R_{pdRmax}-R_{pdRmin}}{R_{pdRmax}+R_{pdRmin}}$
    - Result: 34.18% PD PI Runbalance

Voltage Unbalance and Diode Models

Three Diode Models Simulated

- **1: Spice Model of Schottky STPS2H100**
- **3: Ad Hoc Model Vdiode = 0.46 + 0.25 (id)**
- **2: Diode Effective Resistance, determined by V/I at balanced Voltage Condition**

- **Conditions for simulations:**
  - **Voltage Offset Varied in one pair, +/-0.4V relative to the other pair**
  - **Worst Case Cable, Connector, Transformer Unbalance**
    - Short (1M), Long (~80M) Cables, 5% unbalanced
  - **Diodes Matched (same model in each pair)**
  - **50V Source, 50W Load**

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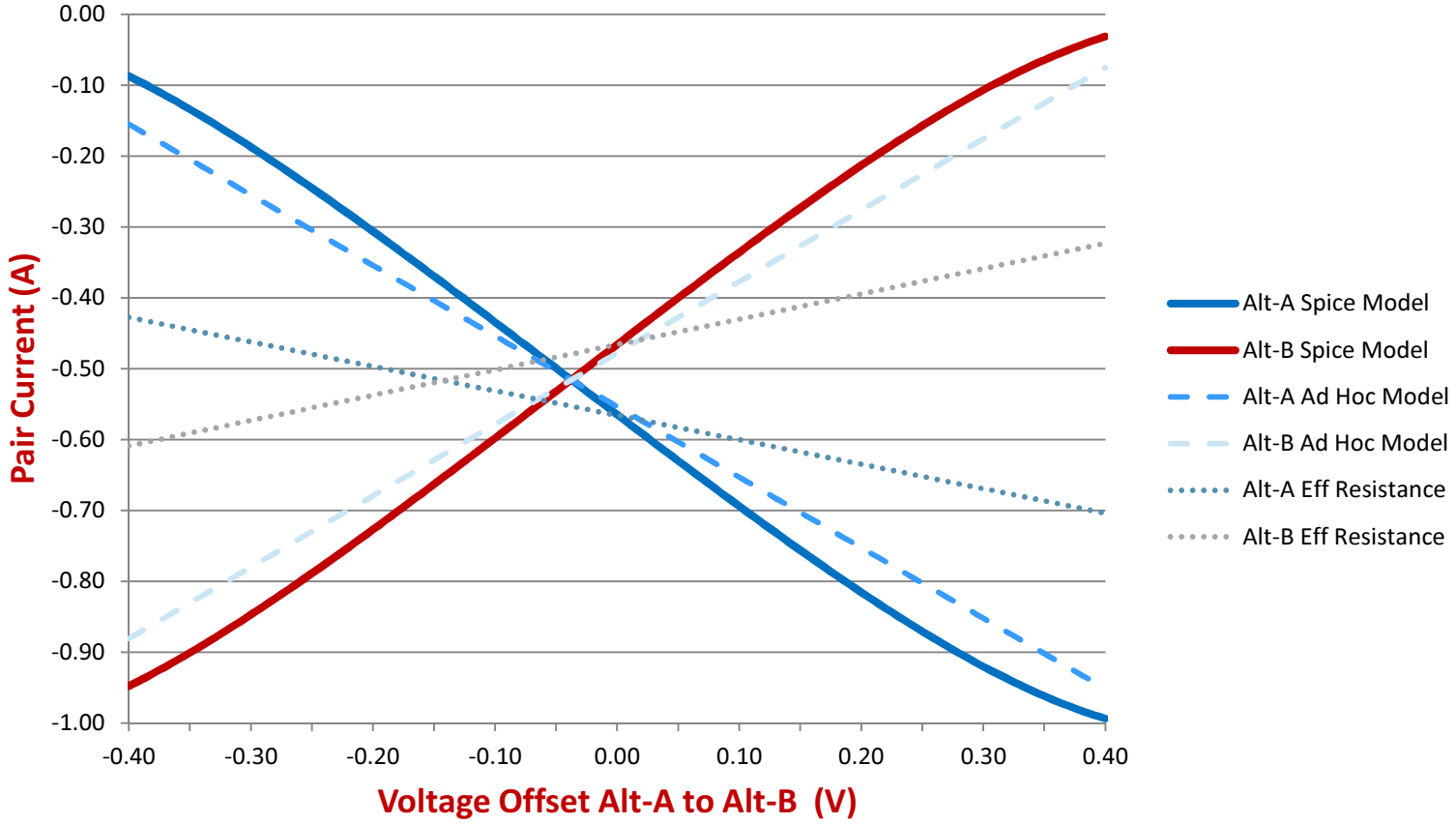
Pair currents versus PSE V_offset, matched bridge diodes. (Worst case conns, SHORT cable, transformers)



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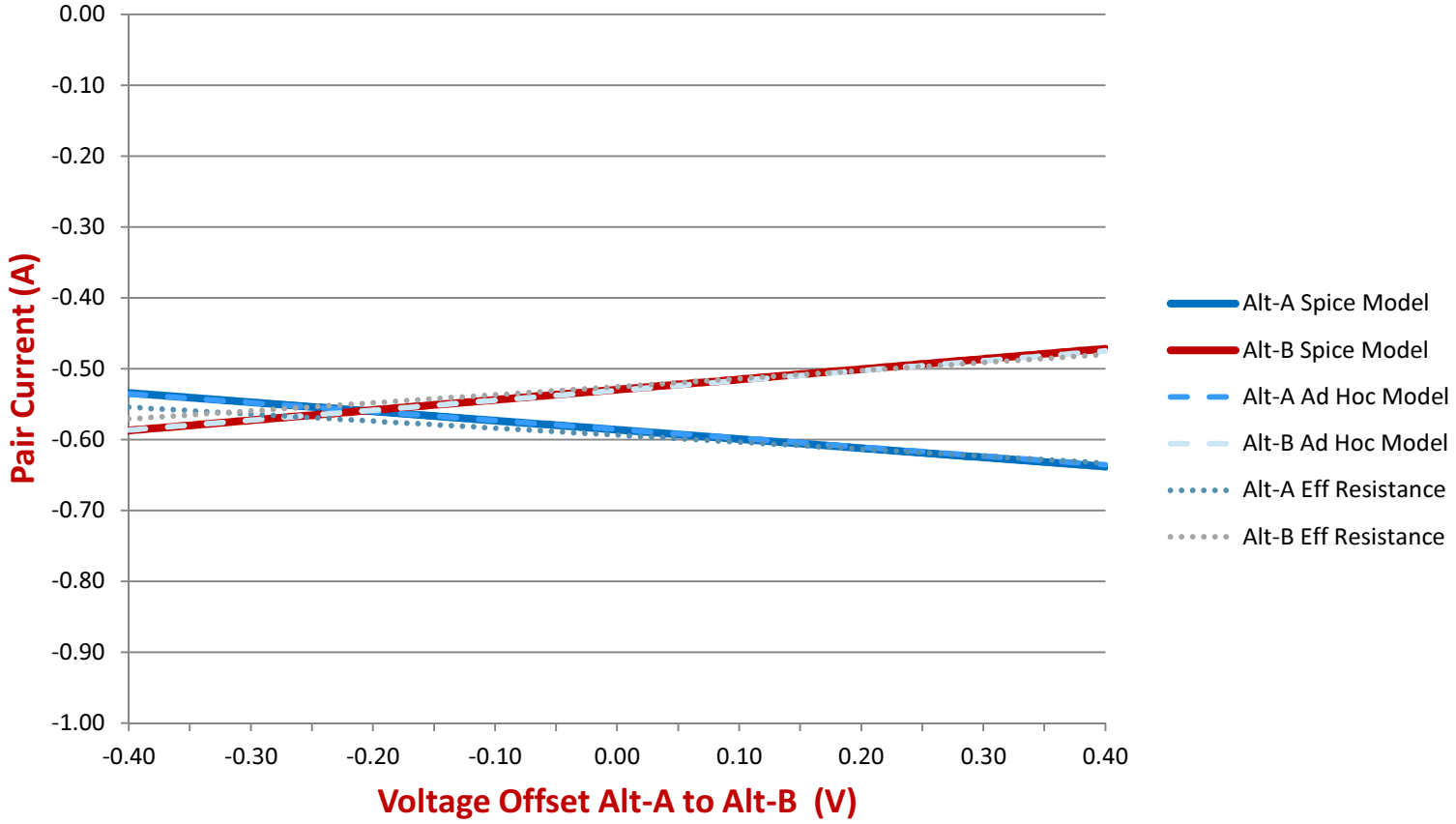
Pair currents versus PSE V_offset, matched bridge diodes. (Worst case conns, LONG cable, transformers)



Summary

- **Worst Case Runbalance of each PI doesn't just depend upon Worst Case System Runbalance**
  - PI Rtotal has a strong influence
- **Specifying Runbalance based upon the worst case can be too restrictive for other valid implementations**
  - And inapplicable to others
- **Actual Current imbalance can be worse than indicated by Ad Hoc models**
  - And *significantly* worse than indicated by effective resistance, as may be determined in a test for compliance
- **Worst case current per pair in a link cannot be accurately predicted with a PSE or PD PI Runbalance spec**
  - However worst case models *do* indicate:
    - *Worst case current occurs in a positive pair*
    - *Positive pair current is not sensed*

Annex A - Simulated Circuit Example