Resistive Imbalance Specification Issues and Limitations

Ken Bennett – Sifos Technologies, Inc.

Resistive Imbalance Ad Hoc

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Overview

- **A goal of the Ad Hoc has been to determine and limit Current Imbalance by specifying behavior of each contributing element (PSE, Channel, PD)**
  - **Current imbalance and resistance unbalance would be used to determine max. current per pair**

(Yair: in order to decide on what parameter to look you need to do calculation first of Runb. In any case Iunbalance=Runb[%]*Total current. Runb is the cause)

- **Based upon a basic implementation**
  - **Single PD (Bridge outputs tied together)**
  - **Single-source PSE**
  - **No balance correction**

- **Resistive Imbalance is the parameter used for the Channel, and has been suggested as a specification requirement for the PSE and PD Interfaces**

  Yair: when you say "channel" do you mean to end to end channel pair to pair resistance unbalance OR channel which is only cables and connectors? If it is just the channel in which we had motion last time, it must be only Runb terms.

- **Limitations of this method are presented herein**

(Yair: Regarding PSE and PD PI P2PRUN, there is general consensus that we need to specify voltage unbalance as well. So th two parameters voltage and resistance specifies all what we need. We can't specify only current Unbalance since it implies implementation such the need for current sharing/balancing techniques etc. it also not solving the issue of PD with deliberately different loads on Mode A and B e.g. 100mA and 180mA….)

System Imbalance

- **The following is a Resistive imbalance equation for determining current imbalance between pairs (Single source, single PD)**

(Yair: please make it clear that ou are discussion end to end channel pair to pair resistance unbalance. Please use the "Acronyms used in the ad-hoc activity" slides of the ad-hoc material.)

$$\frac{\sum R_{max} - \sum R_{min}}{\sum (R_{max} + R_{min})} \qquad (1)$$

- **This can be separated into contributions of the PSE, PD and Channel:**

$$\frac{R_{pseRmax} - R_{pseRmin}}{\sum (R_{max} + R_{min})} + \frac{R_{CableRmax} - R_{CableRmin}}{\sum (R_{max} + R_{min})} + \frac{R_{pdRmax} - R_{pdRmin}}{\sum (R_{max} + R_{min})} \qquad (2)$$

Yair: this is correct but we can't use it. Wwhen we will determine the PSE PI and PD PI unbalance requirements , they will be a function of the end to end channel P2PRUNB as in equation (1).

PI Imbalance Specification Problem

- **The contribution of each is dependent upon the overall resistance**
  - **PSE PI Runbalance contribution is not the same as PSE PI Runbalance**

  (Yair. This statement is correct and we are not doing it. So not clear is the point to show incorrect equality and present it as a problem?)

$$\frac{R_{pseRmax}-R_{pseRmin}}{\sum(R_{max}+R_{min})} \neq \frac{R_{pseRmax}-R_{pseRmin}}{R_{pseRmax}+R_{pseRmin}}$$

  - **PD PI Runbalance contribution is not the same as PD PI Runbalance**

$$\frac{R_{pdRmax}-R_{pdRmin}}{\sum(R_{max}+R_{min})} \neq \frac{R_{pdRmax}-R_{pdRmin}}{R_{pdRmax}+R_{pdRmin}}$$

  (Yair. Same for the PD. This statement is correct and we are not doing it. So not clear is the point to show incorrect equality and present it as a problem?)
- **Changes in total resistance can change derived Runbalance requirements for either or both Pis.** (Yair: Correct)
- An Runbalance spec at the PSE PI and PD PI will not directly correlate with current imbalance. (Yair: The PSE PI and PD PI Runb will correlate with current unbalance when all parts of the system will be connected (PSE, PD, CHANNEL). We will show the technique during this meeting or next meeting.)

PSE Runbalance Calculation, Simulation

- **Simulation Conditions common to each:**
  - **~1M Cable, worst case model used to arrive at ~26%**
  - **PD with Diode Bridge**
  - **PD, Channel fixed, PSE varied**

Yair: This result is incorrect. It should be less than 10%

	PSE Runbal		Channel		PD Runbal	
Rpse other	0.001	0.001				
Rtrans	0.06	0.065				
Rconn	0.015	0.03	0.015	0.03		
Wire			0.0275	0.0285		
Rconn			0.015	0.03	0.015	0.03
Rtrans					0.06	0.065
Rdiode					0.8557	1.537
Unbalance	0.1163	12%	0.2123	21%	0.2737	27%
System Runbalance						
	0.26115	26.1%				
Simulation Iunbalance Result						
(mA)	658.35	385.65	0.261207	26.1%		

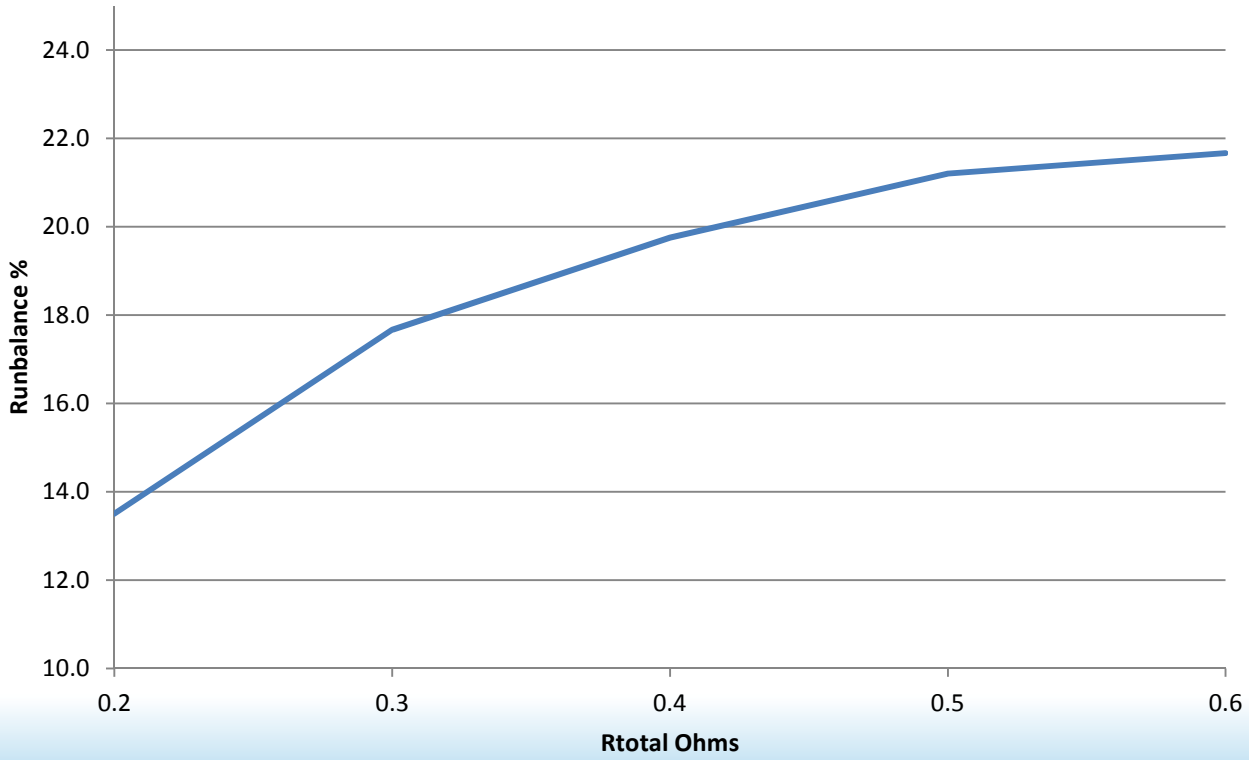
	PSE Runbal		Channel		PD Runbal	
Rpse other	0.23	0.392				
Rtrans	0.06	0.065				
Rconn	0.015	0.03	0.015	0.03		
Wire			0.0275	0.0285		
Rconn			0.015	0.03	0.015	0.03
Rtrans					0.06	0.065
Rdiode					0.8557	1.537
Unbalance	0.2298	23%	0.2123	21%	0.2737	27%
System Runbalance						
	0.26118	26.1%				
Simulation Iunbalance Result						
(mA)	658.35	385.65	0.261207	26.1%		

PSE Runbalance can vary significantly for a fixed total Runbalance

(Yair. Agree. This is how it works. PSE PI Runb can be increased and yet system unbalance remains almost the same. This is a desired behavior. It gives design flexibility to the PSE side. I will explain why at the adhoc.)

PSE Runbalance Requirement VS PSE total resistance (Channel, PD, and System Runbalance unchanged)

(Yair: This is unbalance between positive and negative pairs correct?.
-You need to show also between negative and negative
-positive and positive
-And use also Rpse in positive rails for complete picture of it.



PD Simulation of Diode vs FET bridge

- **Simulation Conditions common to each:**
  - PSE, Channel (~1M Cable), from worst case models, held constant
  - System Imbalance = 26.12%
- **Diode Case:**
  - 26.12% Iunbalance in simulation
  - Vdiode/Idiode + Rtransf + Rconn → $\frac{R_{pdRmax}-R_{pdRmin}}{R_{pdRmax}+R_{pdRmin}}$
    - **Result: 27.45% PD PI Runbalance**
- **FET Case:**
  - Simulations used to arrive at 26.12% Iunbalance
  - FET resistances: .04 min and 1.45 max Ohms
  - Rds + Rtransf + Rconn → $\frac{R_{pdRmax}-R_{pdRmin}}{R_{pdRmax}+R_{pdRmin}}$
    - **Result: 34.18% PD PI Runbalance**

Yair: Same comments as in PSE side.

Yair: do you mean using MOSFETS INSTEAD DIODES? If yes , these numbers are totally incorrect. Using Mosfets are much better for balance. You assume discrete MOSFETs which is wrong.

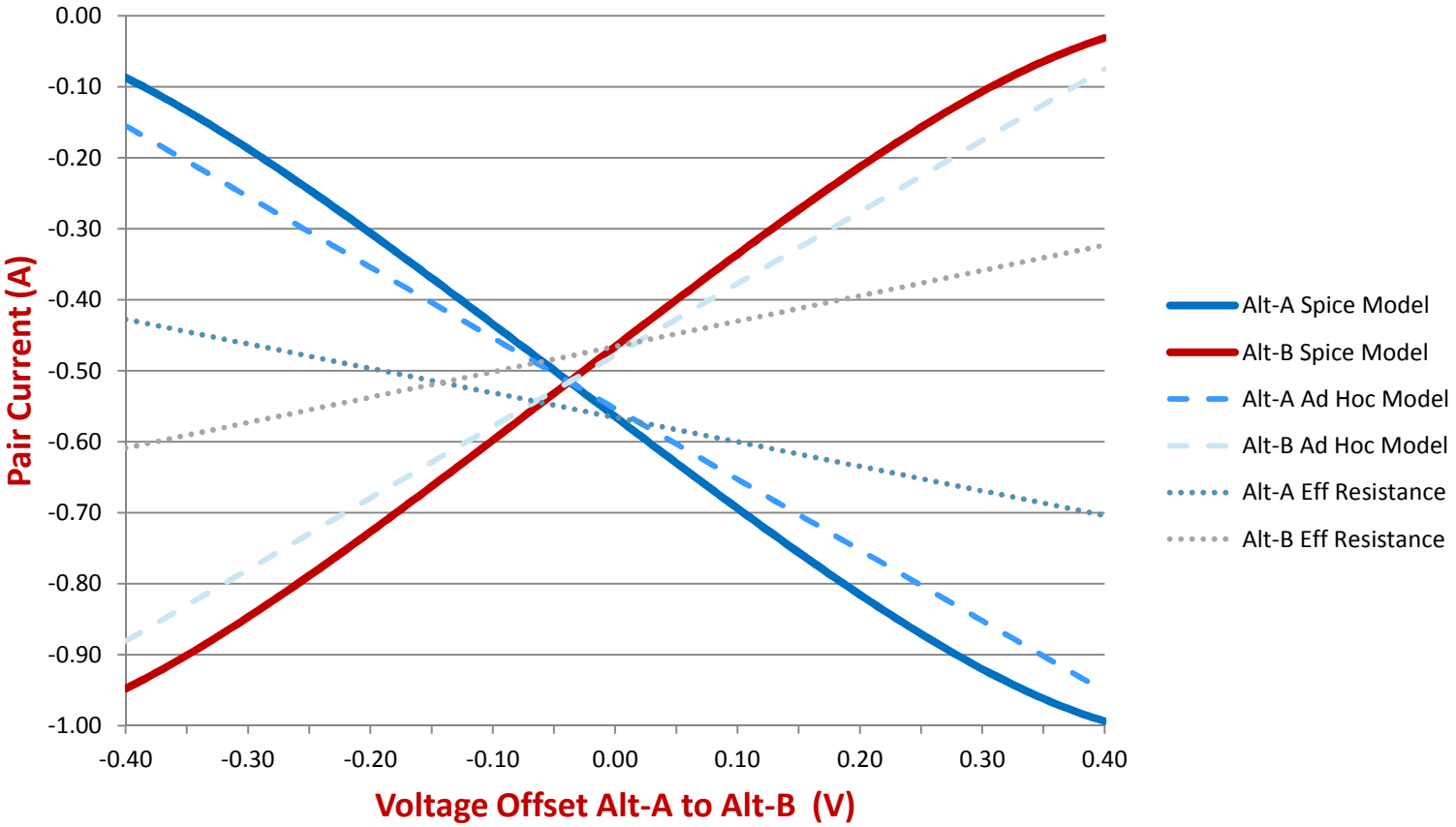
Voltage Unbalance and Diode Models

Three Diode Models Simulated

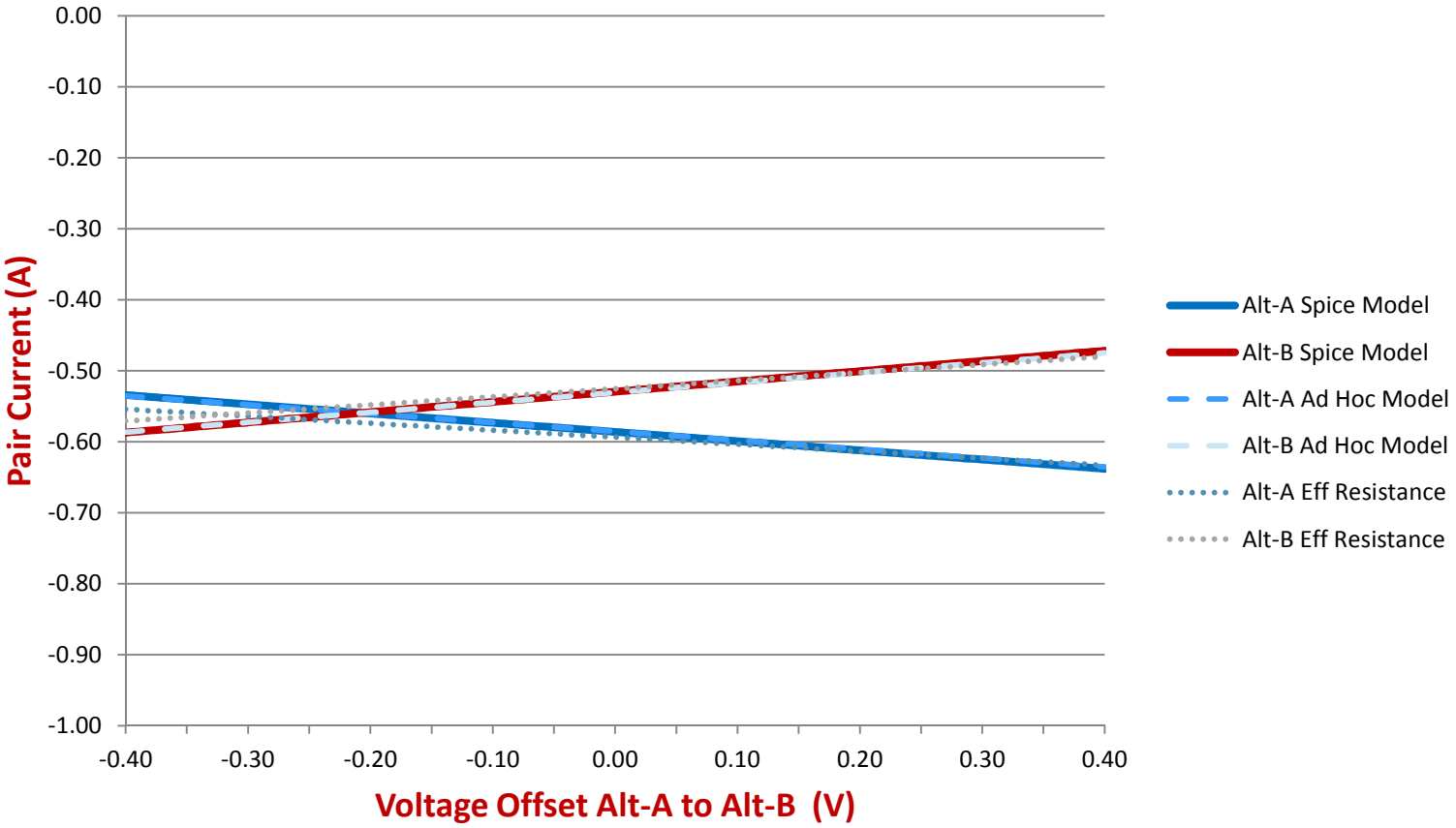
- **1: Spice Model of Schottky STPS2H100**
- **3: Ad Hoc Model Vdiode = 0.46 + 0.25 (id)**
- **2: Diode Effective Resistance, determined by V/I at balanced Voltage Condition**

- **Conditions for simulations:**
  - **Voltage Offset Varied in one pair, +/-0.4V relative to the other pair**
  - **Worst Case Cable, Connector, Transformer Unbalance**
    - Short (1M), Long (~80M) Cables, 5% unbalanced
  - **Diodes Matched (same model in each pair)**
  - **50V Source, 50W Load**

Pair currents versus PSE V_offset, matched bridge diodes. (Worst case conns, SHORT cable, transformers)



Pair currents versus PSE V_offset, matched bridge diodes. (Worst case conns, LONG cable, transformers)



Summary

- **Worst Case Runbalance of each PI doesn't just depend upon Worst Case System Runbalance (**Yair: Runb_max of each PI specification is derived from system Runb_max that we can live with. E.g. PSE PI Runb may be set to X and PD PI Runb may be set to Y so (1) X>Y (this is the practical case. And If Z is the total end to end unbalace requirement than: X>Z, Y<Z. All the numbers will correlate eventually to current unbalance because we will built it to behave as such.)
  - PI Rtotal has a strong influence
- **Specifying Runbalance based upon the worst case can be too restrictive for other valid implementations** (Yair: This is a standard. Once numbers are specified it may be good/bad to some implementation, not clear it will be bad for what?. we can use statistical analysis too after we conclude the worst case analysis. Do you have other proposals?)
  - And inapplicable to others
- **Actual Current imbalance can be worse than indicated by Ad Hoc models**
  - And *significantly* worse than indicated by effective resistance, as may be determined in a test for compliance (Yair: Please explain it. You didn't adresse it in your presentation and yet have a conclusion)
- Yair: This conclusion is impossible if you have used the same data base and model. It is obvious if you use different numbers you will get different results.
- **Worst case current per pair in a link cannot be accurately predicted with a PSE or PD PI Runbalance spec. Yair: With PSE PI, PD PI and Channel we can get good predictions if we are doing it correctly.)**
  - However worst case models *do* indicate:
    - *Worst case current occurs in a positive pair (Yair: Only if Rmin is in th epositive pairs..)*
    - *Positive pair current is not sensed (Yair: This is implementation. Positive current may be sensed too. In a worst case conditions we have to assume that they are not sensed.)*

Annex A - Simulated Circuit Example

Yair: In your model, it is not clear that you have used constant power sink. You have to use constant power sink. It works for us.