

1 Revised Table for improved clarity. No technical changes **except what marked in RED.**

2 Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

#	Parameter	Symbol	Units	Min	Max	PSE Type	Additional Information
5	Total output current of both pairsets of the same polarity in POWER_UP state as function of the assigned class.						
	Single Signature PD class 0-4.	I _{inrush}	A	0.4	0.45	All	See 33.2.7.5. See max value definition in figure 33-13.
	Single Signature PD class 5-8 5-6 . Dual Signature PD with the same class per pairset , class 1-5 1-4 .			0.4	0.9	3,4	
Single Signature PD class 7-8 . Dual Signature PD with the same class per pairset , class 5.	0.8			0.9	4	See 33.2.7.5. See max value definition in figure 33-13. See 33.2.7.5.1 for conditions to use lower than I_{inrush_min} current values.	
5a	Output current per pairset in POWER_UP state as function of the assigned class.						
	Dual signature PD class 0-4 with different class over each pairset.	I _{inrush-2P}	A	0.4	0.45	3,4	See 33.2.7.5 See max value definition in figure 33-13.
	Single Signature PD class 5-8 5-6 . Dual Signature PD with the same class per pairset , class 5 1-4 .			0.15	0.6	3,4	
Single Signature PD class 7-8 . Dual Signature with the same class per pairset , class 5.	0.4			0.6	4	See 33.2.7.5. See max value definition in figure 33-13. See 33.2.7.5.1 for conditions to use lower than I_{inrush_2P_min} current values.	

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10 **33.2.7.5 Output current in POWER_UP mode**

11 *Editor's Note: Timing requirements for 4-pair power to be added to this section.*

12 Editor Notes:

13 ~~1. To verify that in dual signature PD with same class i.e. same load, the PD startup is guaranteed if one of the~~
14 ~~pairsets has $I_{nrush-2P_minz}$ and the 2nd has the rest of the current. If both pairsets are turned on at the same~~
15 ~~time, there is no issue at all.~~

16 ~~2.1. To update the definition of dual signature PD with the same class signature that it is a single load PD as opposed~~
17 ~~to dual signature PD with different class that has isolated different loads and hence end to end pair to pair~~
18 ~~resistance unbalance is zero. This will simplify the spec and make it clearer.~~

19 ~~3. Table 33-11 item 5a-5d: to verify that PSE is allowed to do inrush limit with 2P mode.~~

21 **Change the text of 33.2.7.5 as follows:**

22 POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and
23 either the expiration of $T_{Inrush-2P}$ or, for Type 1 and Type 2 PSEs that make use of legacy powerup, the conclusion of
24 PD inrush currents on that pairset, (see 33.3.7.3 [and legacy powerup variable in 33.2.4.4](#)).

26 Type 3 and Type 4 PSEs that apply power to both pairsets when connected to a single-signature PD shall reach
27 POWER_ON state on both pairsets within $T_{Inrush-2P_max}$, starting with the first pairset transitioning into the
28 POWER_UP state. ~~See legacy powerup variable in section 33.2.4.4 for more information on the POWER_UP to~~
29 ~~POWER_ON transition.~~

31 The PSE shall limit ~~the maximum current sourced per pairset ($I_{nrush-2P}$) and the total inrush current (I_{nrush})~~ during
32 POWER_UP per the requirements of Table 33-11, ~~item 5 or items 5a and item 5b or items 5c and item 5d.~~ The
33 maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset PSE inrush template in Figure
34 33-13 and Equation (33-5), ~~when operating class 0-4 PDs and Figure 33-13 and equation (33-5a) when operating~~
35 ~~single signature PDs with class 5 and above or when operating dual signature PDs with the same class over each pairset.~~

36 The minimum value of $I_{nrush-2P}$ includes the effect of end to end pair to pair resistance unbalance.

37 **Replace Figure 33-13 with the following:**

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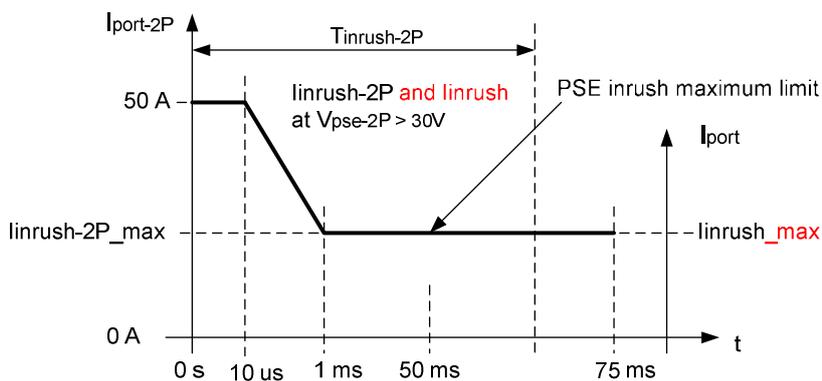


Figure 33-13 – $I_{nrush-2P}$ and I_{nrush} current and timing limits, per pairset in POWER_UP

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41 The PSE inrush maximum limit, $I_{PSEIT-2P}$, is defined by the following segments:

42 Replace equation 33-5 with the following:
 43

$$I_{PSEIT-2P}(t) = \left. \begin{array}{ll} 50.0 & \text{for } 0 < t < 10.0 \times 10^{-6} \\ \text{TBD=function of} & \text{for } 10.0 \times 10^{-6} \leq t < 0.001 \\ \text{(t, Iinrush-2P_max)} & \\ \text{Iinrush-2P_max} & 0.001 \leq t < 0.075 \end{array} \right\} \text{A} \quad (33-5)$$

$$I_{PSEIT-2P}(t) = \left. \begin{array}{ll} 50 & \text{for } 0 < t < 10 \times 10^{-6} \\ y1 + \frac{(50 - y1) \times (0.001 - t)}{99 \times 10^{-5}} & \text{for } 10 \times 10^{-6} < t < 0.001 \\ y1 & \text{for } 0.001 < t < 0.075 \end{array} \right\} \quad (33-5)$$

47
 48 The variable y1 is the maximum value of Iinrush-2P or Iinrush provide in Table 33-11.

49 Where t is the time in seconds

50 ~~Editor Note: To update the TBD in equation 33-5. Add Equation 33-5a after equation 33-5 to describe the template of~~
 51 ~~figure 33-13 for Iinrush.~~

52 The minimum inrush requirement is a function of pairset voltage and is as follows:

- 53 a) During POWER_UP, for pairset voltages between 0 V and 10 V, the minimum Iinrush-2P requirement is 5 mA.
 54 b) During POWER_UP, for pairset voltages between 10 V and 30 V, the minimum Iinrush-2P requirement is 60 mA.
 55
 56 c) During POWER_UP ~~for class 4 and below~~, for pairset voltages above 30 V, the minimum Iinrush and Iinrush-2P
 57 requirement ~~is are as~~ specified in Table 33-11 items 5 and 5a.
 58
 59 ~~During POWER_UP for class 5 and above, for pairset voltages above 30 V, the minimum Iinrush-2P and Iinrush~~
 60 ~~requirement are as specified in Table 33-11 item 5a and item 5b or as specified in Table 33-11 items 5c and 5d.~~
 61
 62 d) For Type 1 PSE, measurement of minimum Iinrush-2P requirement to be taken after 1ms to allow startup transients. A
 63 Type 2 PSE that uses Single-Event Physical Layer classification, and requires the 1 ms settling time, shall power up a
 64 Class 4 PD as if it used Multiple-Event Physical Layer classification.
 65

66 33.2.7.5.1 Iinrush-2P minimum and Iinrush minimum requirements

67 ~~Type 4 PSEs supporting Class 7 and 8 when implementing Iinrush-2P and Iinrush requirements per Table 33-11~~
 68 ~~items 5a and 5b and when connected to single signature PD through channel resistance of 0.1Ω to 12.5Ω per pairset,~~
 69 ~~shall successfully power up within 50msec without startup oscillations a PD with Cport per pairset as defined in~~
 70 ~~33.3.7.3 in parallel to a Class 2 load during POWER_UP period in addition to the other requirements of 33.3.7.~~

71 A Type 4 PSE, when connected to a single signature PD with assigned Class 7 or 8, may optionally implement a
 72 minimum Iinrush-2P and Iinrush lower than defined in Table 33-11 item 5a and 5 but not less than 0.15A and 0.4A
 73 respectively. When Type 4 PSE is connected to a single signature PD with assigned Class 7 or 8 and use lower Iinrush-
 74 2P and Iinrush than defined in Table 33-11 it shall successfully power up a single-signature PD comprised of a parallel
 75 combination of Cport per pairset as defined in 33.3.7.3 and a Class 2 load within Tinrush-2p min without startup
 76 oscillations during the POWER_UP period, when connected to the PD through channel resistance of 0.1Ω to 12.5Ω per
 77 pairset.

78 Table 33-18 per D1.5 with editing changes for simplifying the table

79 **Table 33–18—PD power supply limits**

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
Input Inrush current							
5+5a <u>5</u>	Single signature PD class 0-40-6 . Single Signature PDs Class 5-6 Dual Signature PDs with the same class, <u>class 1-4</u> .	Inrush-PD	A		0.4	1,2 <u>All</u>	Peak value see 33.3.7.3
5e	Single Signature PDs Class 7-8. Dual Signature PDs with the same class, <u>class 5</u> .	<u>Iinrush-PD</u>			<u>0.8</u>	<u>4</u>	
Input Inrush current per pairset							
Was part of 5	Dual signature PDs with different class over each pairset.	Inrush-PD-2P			0.4	<u>3</u>	Peak value see 33.3.7.3
5b <u>5a</u>	Single Signature PDs Class 5-6 Dual Signature PDs with the same class.				0.3/ TBD	3,4	
5d	Single Signature PDs Class 7-8. Dual Signature PDs with the same class, <u>class 5</u> .				<u>0.6</u>	<u>4</u>	

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82 **33.3.7.3 Input inrush current**

83 *Replace first paragraph of Section 33.3.7.3 with the following g:*

84 Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant
85 with Vport_PD-2P requirements as defined in Table 33–16a, and ending when CPort has reached a steady state and is
86 charged to 99% of its final value. This period shall be less than TInrush-2P min per Table 33–11. All PDs shall
87 consume maximum of ~~Class 3~~Type 1 power for at least Tdelay-2P min. This allows the PSE to properly complete
88 inrush.

89

90 *Editor’s Note: This paragraph has changed as a result of MR1277. Do not change this paragraph without
91 consulting the request of MR1277.*

92

93 *Change second, third and fourth paragraph of Section 33.3.7.3 as follows:*

94 Tdelay-2P for each pairset starts when VPD-2P crosses the PD power supply turn on voltage, VOn_PD. This delay is
95 required so that the Type 2, Type 3 and Type 4 PD ~~does~~ not enter a high power state before the PSE has had time to
96 switch current limits on each pairset from IInrush-2P to ILIM-2P.

97

98 Input inrush current at startup Iinrush-PD and Iinrush-PD-2P ~~is~~are limited by the PSE if CPort per pairset < 180 μF for:

99 a) single-signature PDs assigned Class 0-6 or

100 b) dual-signature PDs assigned class 1-5.

101 and if CPort per pairset < 360uF for single-signature PDs assigned Class 7-8, as specified in Table 33–11.

102 If CPort per pairset is larger ~~is~~ ≥ 180 μF, input inrush current shall be limited by the PD so that IInrush_PD and Iinrush-
103 PD-2P max is satisfied.

104

105 ~~For Type 3 and 4 PDs operating class 1–5 dual-signature PDs:~~

106 ~~Input inrush current at startup is limited by the PSE if CPort per pairset < 180 μF, as specified in Table 33–11.~~

107

107 ~~If CPort per pairset $\geq 180 \mu\text{F}$, input inrush current shall be limited by the PD so that $I_{\text{nrush_PD}}$ and $I_{\text{nrush_PD-2P max}}$~~
108 ~~is satisfied.~~

110 ~~For Type 4 PDs operating class 7 and 8 single signature PDs:~~

111 ~~Input inrush current at startup is limited by the PSE if CPort per pairset $< 360 \mu\text{F}$, as specified in Table 33–11.~~

112 ~~If CPort per pairset $\geq 360 \mu\text{F}$, input inrush current shall be limited by the PD so~~

113 ~~that $I_{\text{nrush_PD}}$ and $I_{\text{nrush_PD-2P max}}$ is satisfied.~~

114 ***Insert the following note at the end of section 33.3.7.3 as follows:***

115 NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches
116 99% of steady state or after $T_{\text{nrush-2p}}$ min. See 33.2.7.4 for details.

117
118 CPort in Table 33–18 is the total PD input capacitance during POWER_UP and POWER_ON states that a PSE
119 encounters when operating one or both pairsets, when connected to a single-signature PD. When PSE is connected to
120 dual-signature PDs, CPort value requirements are specified in 33.3.7.6.

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123 ***** END OF BASELINE TEXT *****

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126 **Annex A: D1.5 : Table 33-11 for reference.**

#	Parameter	Symbol	Units	Min	Max	PSE Type	Additional Information
5	Output current in POWER_UP state	Iinrush	A	0.4	0.45	All	For Class 0-4 single signature PDs. For dual signature PDs with different class over each pairset, this requirement applies over each pairset. See 33.2.7.5. See max value definition in Figure 33- 13.
5a	Output current in POWER_UP state	Iinrush	A	0.4	0.9	3,4	For \geq class 5 single signatures PD. For dual signature PD with the same class per pairset. Total current for both pairsets. See 33.2.7.5. See max value definition in Figure 33-13.
5b	Output current per pairset in POWER_UP state	Iinrush-2P	A	0.150	0.6	3,4	For \geq class 5 single signatures PD. For dual signature PD with the same class per pairset. See 33.2.7.5. See max value definition in Figure 33-13.
5c	Output current in POWER_UP state	Iinrush	A	0.8	0.9	4	For class 7 and 8 PDs For dual signature PD with the same class per pairset. Total current for both pairsets See 33.2.7.5. See max value definition in Figure 33-13.
5d	Output current per pairset in POWER_UP state	Iinrush-2P	A	0.4	0.6	4	For class 7 and 8 For dual signature PD with the same class per pairset. See 33.2.7.5. See max value definition in Figure 33-13

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Table 33-18 per D1.5 with Typo corrections

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Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
5	Input Inrush current	Iinrush-PD	A		0.4	1,2. All	Peak value see 33.3.7.3 For single signature PD class 0-4.
	Input Inrush current <u>per pairset</u>	Inrush-PD-2P			0.4	All	For dual signature PDs with different class over each pairset, this requirement applies over each pairset.
5a	Total Inrush current	Iinrush-PD			0.4	3,4	Peak value see 33.3.7.3 Single Signature PDs Class 5-6 Dual Signature PDs with the same class.
5b	Total inrush current Input Inrush current <u>per pairset</u>	Iinrush-PD_2P			0.3/ TBD	3,4	Peak value see 33.3.7.3 Single Signature PDs Class 5-6 Dual Signature PDs with the same class.
5c	Total Inrush current	Iinrush-PD			0.8	4	Peak value see 33.3.7.3 Single Signature PDs Class 7-8. Dual Signature PDs with the same class.
5d	Input Inrush current <u>per pairset</u>	Iinrush-PD_2P			0.6	4	Peak value see 33.3.7.3 Single Signature PDs Class 7-8. Dual Signature PDs with the same class.

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