Comment i-262

1. Make the following changes.
2. In addition, Remove TEST_MODE, TEST_MODE_PRI and TEST_MODE_SEC components/variable from clause 145.

30.9.1.1.4 aPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PSE disabled
searching	PSE searching
deliveringPower	PSE delivering power
test	PSE test mode
fault	PSE fault detected
otherFault	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.5 and 145.2.6.

The enumeration "disabled" indicates that the PSE State diagram (Figure 33–9) is in the state DISABLED. The enumeration "deliveringPower" indicates that the PSE State diagram is in the state POWER_ON. The enumeration "test" indicates that the PSE State diagram is in the state TEST_MODE. The enumeration "fault" indicates that the PSE State diagram is in the state TEST_ERROR. The enumeration "otherFault" indicates that the PSE State diagram is in the state IDLE due to the variable error_condition = true. The enumeration "searching" indicates the PSE State diagram is in a state other than those listed above. ~~If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.5.1.2.11.~~

NOTE—A derivative attribute may wish to apply a delay to the use of the "deliveringPower" enumeration as the PSE state diagram will enter then quickly exit the POWER_ON state if a short-circuit or overcurrent condition is present when power is first applied.

30.9.1.1.4 aPSEPowerDetectionStatusS

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PSE disabled
searching	PSE searching
deliveringPower	PSE delivering power
~~test~~	~~PSE test mode~~
~~fault~~	~~PSE fault detected~~
otherFault	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.5 and 145.2.6.

The enumeration “disabled” indicates that the PSE State diagram (Figure 33–9) is in the state DISABLED. The enumeration “deliveringPower” indicates that the PSE State diagram is in the state POWER_ON. ~~The enumeration “test” indicates that the PSE State diagram is in the state TEST_MODE. The enumeration “fault” indicates that the PSE State diagram is in the state TEST_ERROR.~~ The enumeration “otherFault” indicates that the PSE State diagram is in the state IDLE due to the variable error_condition = true. The enumeration “searching” indicates the PSE State diagram is in a state other than those listed above. ~~If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.5.1.2.11.~~

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPower” -enumeration as the PSE state diagram will enter then quickly exit the POWER_ON state if a short-circuit or overcurrent condition is present when power is first applied.

30.9.1.1.4a aPSEPowerDetectionStatusA

Not part of the baseline
TEST MODE was deleted in from Type 3 and 4 state machine and variable definitions

ATTRIBUTE
APPROPRIATE SYNTAX:

searchingAltA	PSE searching
deliveringPowerAltA	PSE delivering power
~~testAltA~~	~~PSE test mode~~
~~faultAltA~~	~~PSE fault detected~~
otherFaultAltA	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 145.2.6.

The enumeration “deliveringPowerAltA” indicates that the PSE State diagram is in the state POWER_ON_PRI. ~~The enumeration “testAltA” indicates that the PSE State diagram is in the state TEST_MODE_PRI. The enumeration “faultAltA" indicates that the PSE State diagram is in the state TEST_ERROR_PRI.~~ The enumeration “otherFaultAltA indicates that the PSE State diagram is in the state IDLE_PRI due to the variable error_condition_pri = true. The enumeration “searchingAltA” indicates the PSE State diagram is in a state other than those listed above.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPowerAltA” enumerations as the PSE state diagram will enter then quickly exit the POWER_ON_PRI state if a short-circuit or overcurrent condition is present when power is first applied;

30.9.1.1.4b aPSEPowerDetectionStatusB
ATTRIBUTE
APPROPRIATE SYNTAX:

searchingAltB	PSE searching
deliveringPowerAltB	PSE delivering power
~~testAltB~~	~~PSE test mode~~
~~faultAltB~~	~~PSE fault detected~~

otherFaultAltB PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 145.2.6.

The enumeration “deliveringPowerAltB” indicates that the PSE State diagram is in the state POWER_ON_SEC. ~~The enumeration "testAltB indicate that the PSE State diagram is in the state TEST_MODE_SEC. The enumeration faultAltB" that the PSE State diagram is in the state TEST_ERROR_SEC.~~ The enumeration "otherFaultAltB” indicates that the PSE State diagram is in the state IDLE_SEC due to the variable error_condition_sec = true. The enumeration “searchingAltB” indicates the PSE State diagram is in a state other than those listed above.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPowerAltB” enumerations as the PSE state diagram will enter then quickly exit the POWER_ON_SEC state if a short-circuit or overcurrent condition is present when power is first applied;

30.9.1.1.6 aPSEInvalidSignatureCounter
ATTRIBUTE
APPROPRIATE SYNTAX: Generalized nonresettable counter.
This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the Type 1 and Type 2 PSE state diagram (Figure 33-9) enters the state SIGNATURE_INVALID. ~~This counter is not defined for Type 3 and Type 4 PSEs. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.5.1.2.6.;~~

30.9.1.1.6a aPSEInvalidSignatureCounterS
ATTRIBUTE
APPROPRIATE SYNTAX: Generalized nonresettable counter.
This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the Type 3 and Type 4 PSE state diagram (Figure 145-13) enters the state IDLE due to sig_pri ≠ valid or sig_sec ≠ valid

30.9.1.1.6b aPSEInvalidSignatureCounterA
ATTRIBUTE
APPROPRIATE SYNTAX: Generalized nonresettable counter.
This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the Type 3 and Type 4 PSE state diagram (Figure 145-15) enters the state IDLE_PRI due to sig_pri ≠ valid.

30.9.1.1.6c aPSEInvalidSignatureCounterB
ATTRIBUTE
APPROPRIATE SYNTAX: Generalized nonresettable counter.
This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the Type 3 and Type 4 PSE state diagram (Figure 145-16) enters the state IDLE_SEC due to sig_sec ≠ valid.

Comment i-263 (30.9.1.1.7 *P* 37 *L* 25)
The PSEPowerDeniedCounter is only specified for Type 1 and Type 2 state machine references. It is not clear if this was intention or if references to Type 3 and Type 4 should be added.
Currently:
This counter is incremented when the PSE state diagram (Figure 33-9) enters the state POWER_DENIED.

Proposed Remedy
Make the following changes:
30.9.1.1.7 aPSEPowerDeniedCounter
ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second. BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–9) enters the state POWER_DENIED. ~~If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.5.1.2.4.;~~

30.9.1.1.7a aPSEPowerDeniedCounterS
ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second. BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–13) enters the state POWER_DENIED.

30.9.1.1.7b aPSEPowerDeniedCounterA
ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second. BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–15) enters the state POWER_DENIED_PRI.

30.9.1.1.7c aPSEPowerDeniedCounterB
ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second. BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–16) enters the state POWER_DENIED_SEC.

Comment i-264 (**30.9.1.1.8** P37, L41)
Comment i-33 (**30.9.1.1.8** P37, L33)

Proposed Remedy:

Make the following changes:

30.9.1.1.8 aPSEOverLoadCounter

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–9) enters the state ERROR_DELAY~~_OVER. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.5.1.2.8.;~~

30.9.1.1.8a aPSEOverLoadCounterS

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–13) enters the state ERROR_DELAY

30.9.1.1.8b aPSEOverLoadCounterA

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–15) enters the state ERROR_DELAY_PRI.

30.9.1.1.8c aPSEOverLoadCounterB

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–15) enters the state ERROR_DELAY_SEC.

Comment i-265 (30.9.1.1.11 *P* 38 *L* 2)

Proposed Remedy:

Make the following changes:

30.9.1.1.11 aPSEMPSAbsentCounter

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted. ~~If a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.5.1.2.9.;~~

30.9.1.1.11a aPSEMPSAbsentCounterS

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–13) transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted.

30.9.1.1.11b aPSEMPSAbsentCounterA

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–15) transitions directly from the state POWER_ON_PRI to the state IDLE_PRI due to tmpdo_timer_pri_done being asserted.

30.9.1.1.11c aPSEMPSAbsentCounterB

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.
BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 145–16) transitions directly from the state POWER_ON_SEC to the state IDLE_SEC due to tmpdo_timer_sec_done being asserted.