Remedies for comments #105, #106, #107
IEEE802.3bt Draft 2.1 Annex 33C

rev.: 1.1

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Connection Check seguence diagrams

comments #106,107

33C.1 Type 3 and Type 4 CC_DET_SEQ timing diagrams

Each of the following sample timing diagrams shows a PSE performing a sequence of connection check, detection, classification, power up and power on events. A PSE implements one or more of the four defined CC_DET_SEQ sequence based on the results of detection, connection check and 4PID.

When the result of the connection check is dual the alternatives are controlled by the semi-independent dual-signature state machine. In this case – depending on the detection, classification and power up are may not synchronized between the alternatives.

CC_DET_SEQ=0 when the result of connection check is **dual** and Class_4PID_mult_events_sec is TRUE

comments #106,107

Figure 33C-2 in Draft 2.1

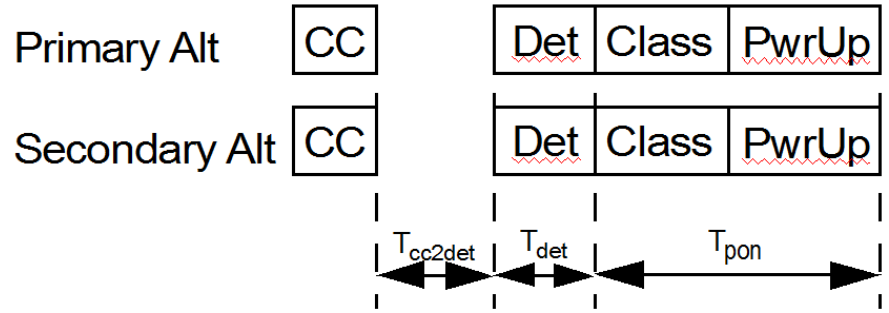

Figure 33C–2—PSE implementing CC_DET_SEQ=0, do_cxn_chk result is dual, simultaneous power on

Proposed new Figure 33C-2

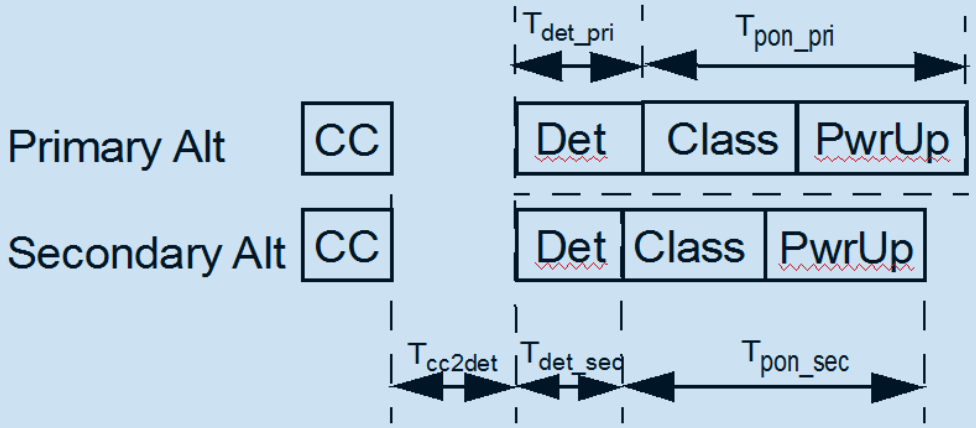

Figure 33C–2—PSE implementing CC_DET_SEQ=0, do_cxn_chk result is dual

Single-Event classification

comment #105

Figure 33C-13 in Draft 2.1

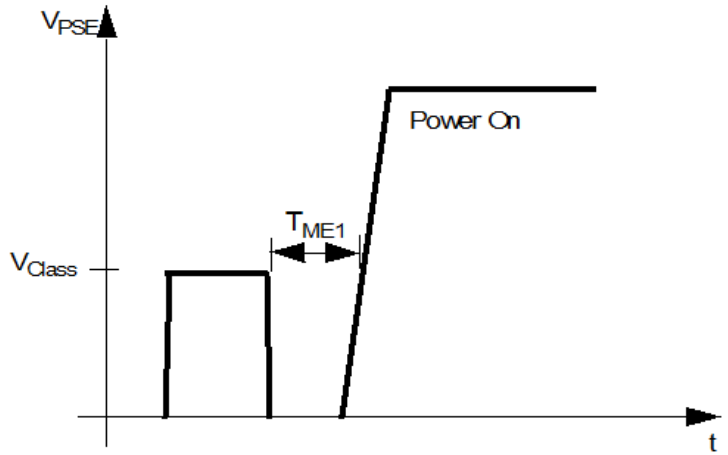

Figure 33C–13—PSE Single-Event Physical Layer classification

Proposed new Figure 33C-13

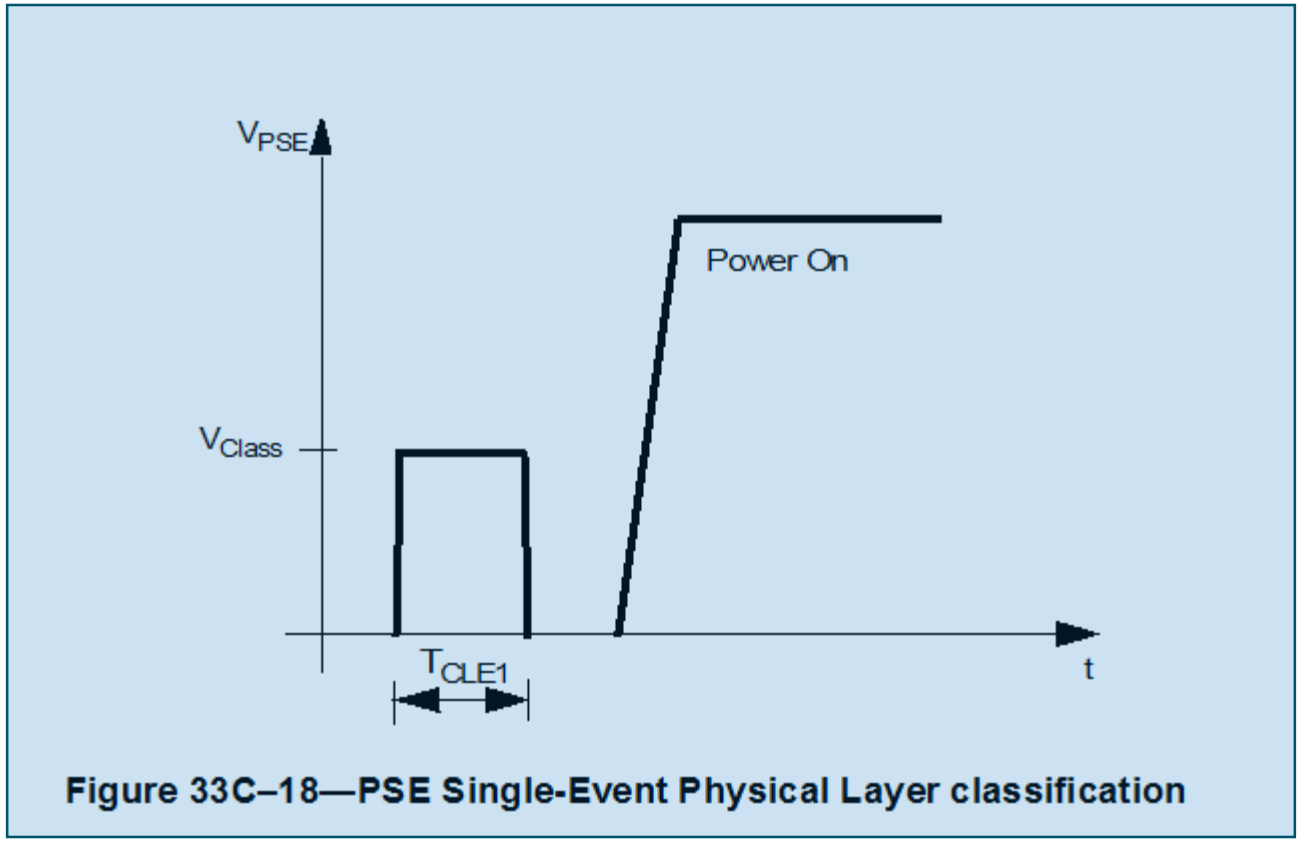

Figure 33C–18—PSE Single-Event Physical Layer classification

Thank You!