Backfeed v230

Info (not part of baseline)

Changelog:

v230 Added PSE requirement to limit current to I_{rev}, different level depending on V_{PSE}, PD 3P spec reduced to detection range only.

v220 Changes:

- Replace the construct “are not required” by “may” (both in PD and PSE section)
- Replace “cause current to flow” by “source” (unless the PD is sourcing power, it’s impossible for current to be sunk into a negative pair).
- Only allow 3P-backfeed from 21 V and up for PDs, but exclude 3P-after-4P
- Cleanup of PSE requirement (got rid of incomprehensible ‘range of potentials’)

v212 As presented during the ad-hoc call of May 7

145.2.4 PSE PI

A PSE device may provide power via one or both of the two valid four-conductor connections, named pairsets. A pairset consists of a pair at the positive V_{PSE} and a pair at the negative V_{PSE}. The two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 145–12, in conjunction with Table 145–3, illustrates the pairsets, which for PSEs are named Alternative A and Alternative B.

PSE are required to switch the negative pairs, and may switch the positive pairs as defined in 145.4.1.1.1. This may lead to both positive pairs providing current in 2-pair mode.

145.2.10 Power supply output

Add new item to Table 145–16 as follows:

Item	17a
Parameter	Unpowered negative pair sourced current
Symbol	I_{rev}
Unit	A
Min	—
Max	0.0013 (split: when highest $V_{PSE} > 21$ V)
Max	0.0005 (split: when highest $V_{PSE} \leq 21$ V)
PSE Type	3, 4
Additional information	See 145.2.10.3a

Insert new subclause after 145.2.10.3 as follows:

145.2.10.3a Reflected voltage

When a 4-pair capable PSE provides power in 2-pair mode, whereby two pairs are connected to the positive V_{PSE}, and one pair is connected to the negative V_{PSE}, a single-signature PD may reflect a voltage of up to V_{PSE} back onto the unpowered pairset. See 145.3.8.8. The PSE shall not source a current higher than I_{rev}, as defined in Table 145–20, on the negative pair of a pairset when the voltage of that pairset is equal to or lower than the voltage of the other pairset.

Irev is not defined in Table 145-20. With the new text, not clear why Table 145-20 is needed.

Same old comment. The PSE alternative that is OFF, can't source current. It can only sink current.

-Not clear. The previous text was better with the "cause".
-How much current is allowerd to "source" when the external voltage is higher that the internal voltage?. It should be zero and it is not specified. There is no spec for internal PD circutry that prevents boosting the reflected voltage.

145.3.2 PD PI

Change the note at the bottom of Table 145–20 as follows:

PSEs are required to switch the negative pairs, ~~but not required to~~ and may switch the positive pairs as defined in 145.4.1.1.1. This may lead to both positive pairs providing current in 2-pair mode.

145.3.8 PD power

Change item 18 such that:

- ***Parameter: Reflected voltage***
- ***Symbol: V_{refl}***

145.3.8.8 ~~Backfeed~~ Reflected voltage

Replace the contents of 145.3.8.8 as follows:

For a single-signature PD, when any voltage in the range of 0 V to $V_{Port\_PD\text{-}2P}$ max is applied per any of the valid 2-pair configurations, defined in Table 145–20, that have only a single pair connected to positive V_{PSE} (see Figure 145–29a), the voltage on the Mode not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29.

For a single-signature PD, when any voltage in the range of 0 V to 10.1 V is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive V_{PSE} (see Figure 145–29a), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29. This requirement does not apply if a voltage greater than 10.1 V has been applied on either Mode until the voltage on both Modes has been less than V_{Reset} for at least T_{Reset}.

For a dual-signature PD, when any voltage in the range of 0 V to $V_{Port\_PD\text{-}2P}$ max is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive V_{PSE} (see Figure 145–29a), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29.

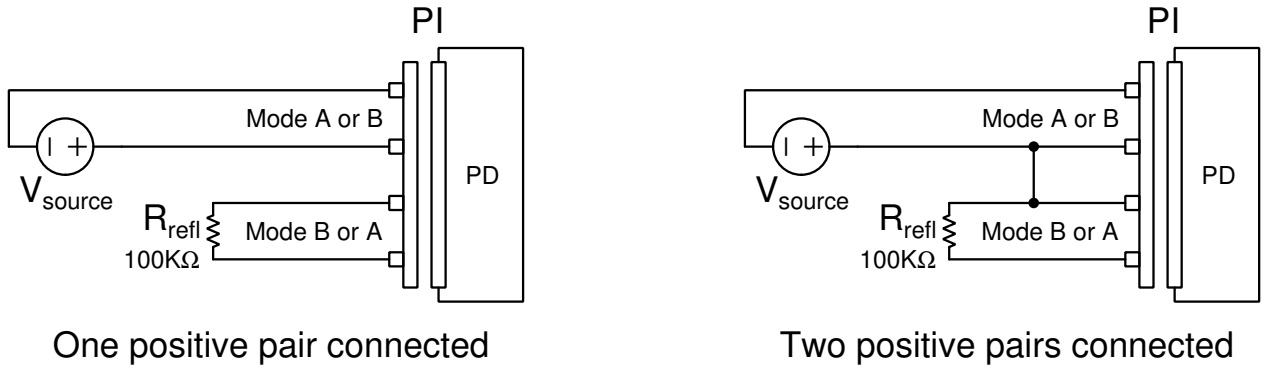

Figure 145–29a — Reflected voltage requirements

Update PICS to reflect changes.