PD $I_{Port\_RMS\_max}$ requirement

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PD Input power/current requirements

A PD has a number of input power / input current requirements listed as follows:

1. **145.3.8 PD power**
   The PD shall operate within the characteristics in Table 145-28. Which includes P_{Port_PD}, which has a maximum of P_{Class_PD}.
2. **145.3.8.4 Peak operating power**
   At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for single-signature PDs shall not exceed P_{Class_PD} for more than $T_{CUT\text{-}2P}$ min, as defined in Table 145-16 and 5% duty cycle. Peak operating power shall not exceed P_{Peak_PD}.

PD Input power/current requirements

3. **145.3.8.4 Peak operating power**
   The maximum I_{Port_RMS} value for all PDs except those described in 145.3.8.2.1 and 145.3.8.4.1, over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation (145-27):

$$I_{Port\_RMS\_max} = \left\{ \frac{P_{Class\_PD}}{V_{Port\_PD\text{-}2P}} \right\}_A \qquad (145\text{–}27)$$

$V_{Port\_PD\text{-}2P}$ is defined as the minimum of the allowed $V_{Port\_PD\text{-}2P}$ range. This makes the $I_{Port\_RMS\_max}$ value more permissive than the average and peak input power requirements. The $I_{Port\_RMS\_max}$ requirement also does not specify a measurement period or window length.

Average power

145.3.8.2 on Input average power says the following:

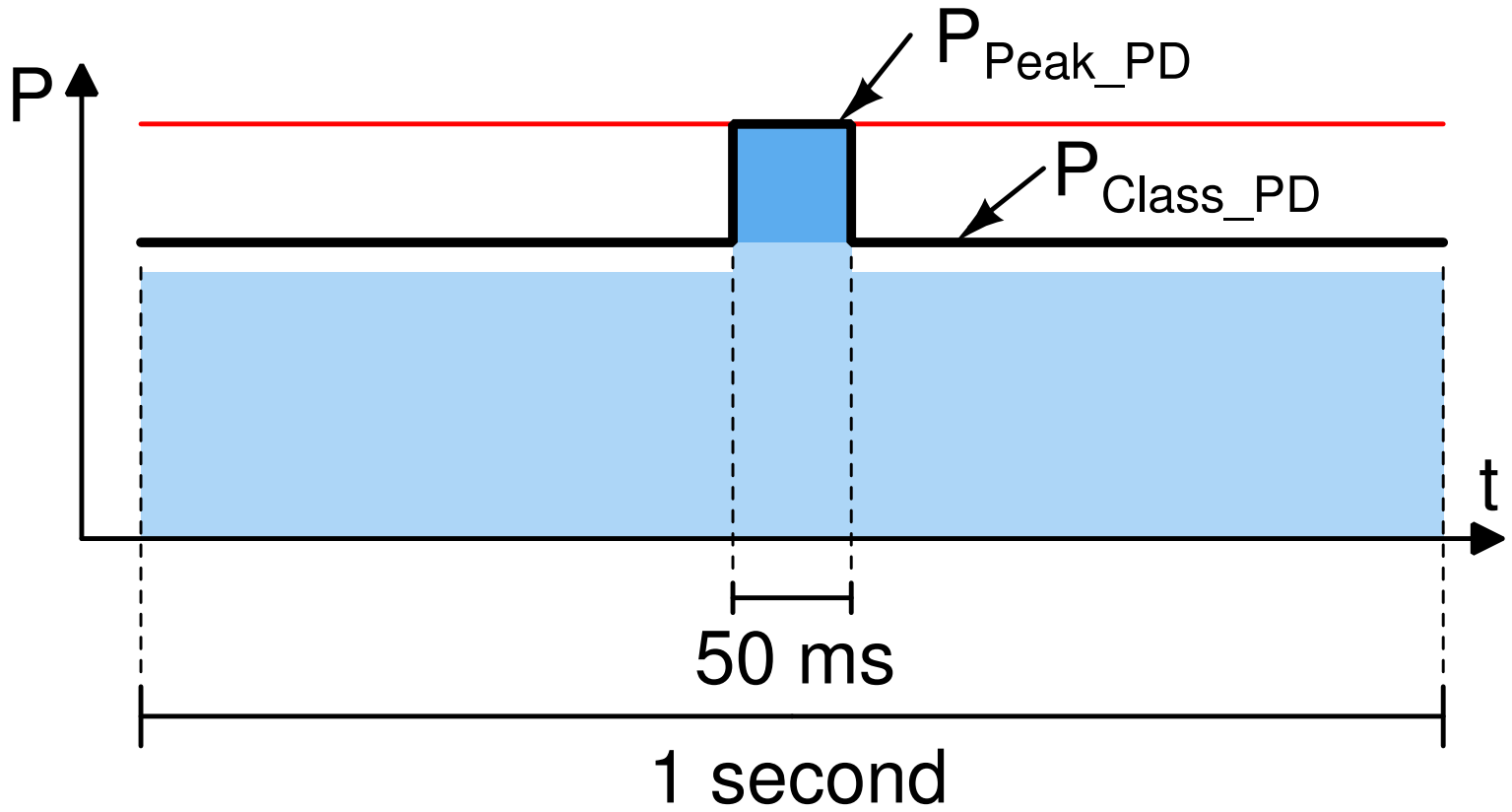
P_{Class_PD} is the maximum average PI power and applies to single-signature PDs. The maximum average power, P_{Class_PD} or $P_{Class\_PD\text{-}2P}$ in Table 145-24, Table 145-25 and Table 145-28 or PDMaxPowerValue in 145.5.3.3, is calculated over a 1 second interval.

NOTE - Average power is calculated using any sliding window with a width of 1 s.

Average power is defined as the product of the RMS current and voltage.

$$\text{Average power} = V_{RMS} \times I_{RMS}$$

Specification overview of (1) and (2)



1: Absolute max power consumption is P_{Peak_PD}.

2: Total blue area of a sliding window of 1 second must be $< P_{Class\_PD}$

3: The $I_{Port\_RMS\_max}$ requirement is a repeat of (2) expressed in current.

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Back to 802.3af

802.3af specified peak **current** rather than peak **power**:

4	Peak operating current, Class 0, 3	I_{Port}	mA		400	See 33.3.5.4
	Peak operating current, Class 1	I_{Port}	mA		120	
	Peak operating current, Class 2	I_{Port}	mA		210	
5	Input current (DC or RMS), V_{Port}=37Vdc	I_{Port}	mA		350	See 33.3.5.3
	Input current (DC or RMS), V_{Port}=57Vdc	I_{Port}	mA		230	

This allowed a PD to take significant peak power, eg:

$56V \cdot 400mA = 22.4W$, far more than the 14.4 W allowed in 802.3at.

802.3af and I_{Port_RMS}

802.3af solved this in the following way:

33.3.5.4 Peak operating current

At any operating condition the peak current shall not exceed P_{Port} max/V_{Port} for more than 50ms max and 5% duty cycle max. Peak current shall not exceed I_{Port} max.

Ripple current content (I_{ac}) superimposed on the DC current level (I_{dc}) is allowed if the total input power is less than or equal to P_{Port} max.

The RMS, DC and ripple current shall be bounded by the following equation: $Irms = \sqrt{(Idc)^2 + (Iac)^2}$.

The maximum I_{Port_dc} and I_{Port_rms} values for all operating V_{Port} range shall be defined by the following equation: I_{Port_max} [mA] =12950/V_{Port}.

With most of the spec written in current, this was the 802.3af way to express the combined power limit of normal and peak power not to exceed 12.95W.

Back to the future

Our specification however is written around **power** limits. Both combined power, as well as absolute peak power is well defined. The average power requirement incorporates RMS current requirements.

Which makes the requirement and text around I_{Port_RMS} and $I_{Port\_RMS\_max}$ redundant to the power requirements, and as such it can be removed.

See appended pages of D2.3 with editing instructions.


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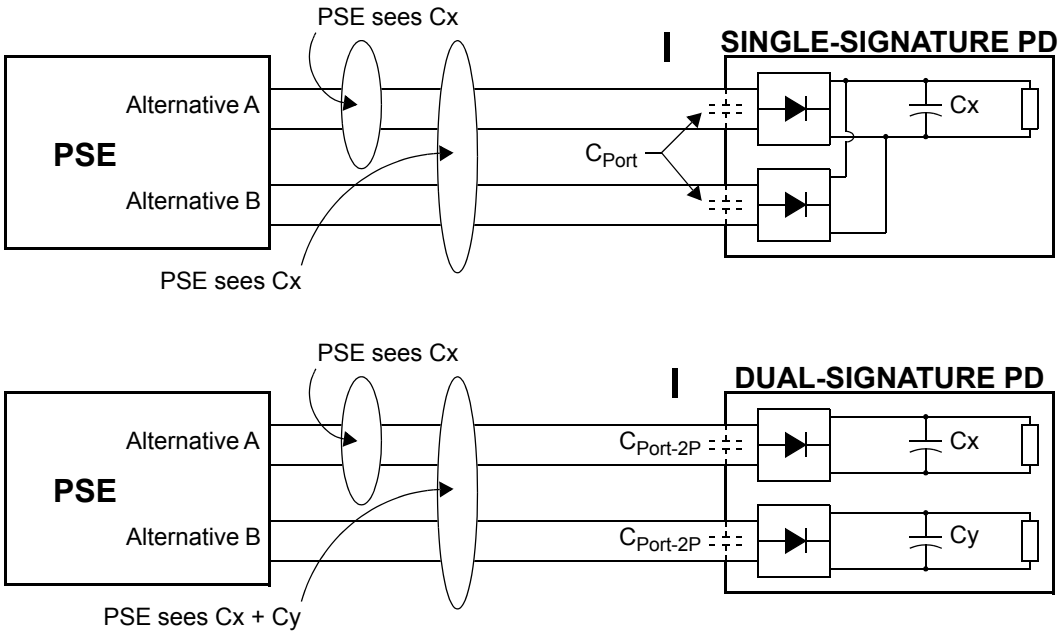

Figure 145–32—C_{Port} interpretation model

NOTE—The "dual-signature PD" in Figure 145–32 represents a PD with two completely isolated circuits connected to Mode A and Mode B. The PSE will see a capacitance of Cx + Cy. A dual-signature PD can also be implemented with a single load, resulting in a lower than Cx + Cy capacitance value as seen by the PSE.

For single-signature PDs, ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if P_{Peak_PD} requirements are met and the total input power is less than or equal to P_{Class_PD}.

For dual-signature PDs, ripple current content ($I_{Port\_ac\text{-}2P}$) superimposed on the DC current level ($I_{Port\_dc\text{-}2P}$) is allowed if $P_{Peak\_PD\text{-}2P}$ requirements are met and the total input power is less than or equal to $P_{Class\_PD\text{-}2P}$.

The RMS, DC and ripple current shall be bounded by Equation (145–26):

$$I_{Port\_RMS} = \left\{ \begin{array}{ll} \sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2} & \text{single-signature PD} \\ \sqrt{(I_{Port\_dc\text{-}2P})^2 + (I_{Port\_ac\text{-}2P})^2} & \text{dual-signature PD} \end{array} \right\}_A \quad (145\text{–}26)$$

where

I_{Port_dc} is the DC component of the input current for a single-signature PD

I_{Port_ac} is the RMS value of the AC component of the input current for a single-signature PD

$I_{Port\_dc\text{-}2P}$ is the DC component of the input current for a dual-signature PD

$I_{Port\_ac\text{-}2P}$ is the RMS value of the AC component of the input current for a dual-signature PD

The maximum I_{Port_RMS} value for all PDs except those described in 145.3.8.2.1 and 145.3.8.4.1, over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation (145–27):

$$I_{Port\_RMS\_max} = \left\{ \begin{array}{ll} \frac{P_{Class\_PD}}{V_{Port\_PD\text{-}2P}} & \text{single-signature PD} \\ \frac{P_{Class\_PD\text{-}2P}}{V_{Port\_PD\text{-}2P}} & \text{dual-signature PD} \end{array} \right\}_A \quad (145\text{–}27)$$

where

$V_{Port\_PD\text{-}2P}$ is the minimum specified input voltage at a PD pairset

P_{Class_PD} is the maximum power at the PD PI per the PDs assigned Class, as defined in Table 145–24

$P_{Class\_PD\text{-}2P}$ is the maximum power at the PD PI for a pairset per the PDs assigned Class as defined in Table 145–25

Peak power is defined in Table 145–28 and depends on the Class assigned by the PSE. The equations in Table 145–28 are used to approximate the ratiometric peak powers of Class 1 through Class 8. These equations may be used to calculate P_{Peak_PD} or $P_{Peak\_PD\text{-}2P}$ for Data Link Layer classification by substituting P_{Class_PD} or $P_{Class\_PD\text{-}2P}$ with PDMaxPowerValue and for Autoclass by substituting P_{Class_PD} with $P_{Autoclass\_PD}$.

The values in Table 145-28 approximate the ratiometric...

145.3.8.4.1 Peak operating power exceptions

For Class 6 and Class 8 single-signature PDs and for Class 5 dual-signature PDs, when additional information is available to the PD regarding actual channel DC resistance between the PSE PI and the PD PI, in any operating condition with any static voltage at the PI, the peak power shall not exceed P_{Class_PD} for single-signature PDs and $P_{Class\_PD\text{-}2P}$ for dual-signature PDs at the PSE PI for more than $T_{CUT\text{-}2P}$ min, as defined in Table 145–16 and with 5% duty cycle. Peak operating power shall not exceed 1.05 × P_{Class_PD} for single-signature PDs and shall not exceed 1.05 × $P_{Class\_PD\text{-}2P}$ for dual-signature PDs on each pairset.

For single-signature PDs ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if P_{Peak_PD} requirements are met and the total input power is less than or equal to P_{Class} at the PSE PI.

For single-signature PDs, the maximum I_{Port_RMS} value over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation (145–28):

$$I_{Port\_RMS\_max} = \left\{ \frac{P_{Class}}{V_{PSE}} \right\}_A \quad (145\text{–}28)$$

where

P_{Class} is the allocated Class power as defined in 145.2.7 and Equation (145–2)

V_{PSE} is the voltage at the PSE PI as defined in 145.1.3

For dual-signature PDs ripple current content ($I_{Port\_ac\text{-}2P}$) superimposed on the DC current level ($I_{Port\_dc\text{-}2P}$) is allowed if $P_{Peak\_PD\text{-}2P}$ requirements are met and the total input power is less than or equal to $P_{Class\text{-}2P}$ at the PSE PI.

For dual-signature PDs, the maximum $I_{Port\_RMS\text{-}2P}$ value over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation (145–29).

$$I_{\text{Port\_RMS-2P\_max}} = \left\{ \frac{P_{\text{Class-2P}}}{V_{\text{PSE}}} \right\}_{\text{A}} \quad (145\text{–}29)$$

where

$P_{\text{Class-2P}}$ is the allocated Class power on a pairset as defined in 145.2.7 and Equation (145–3)

V_{PSE} is the voltage at the PSE PI as defined in 145.1.3

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

145.3.8.5 Peak transient current

When the input voltage at the PI is static and in the range of $V_{\text{Port\_PD-2P}}$ defined by Table 145–28, the input current drawn by a single-signature PD shall not change faster than I_{Slewrate} defined in Table 145–28, in either polarity. Each pairset current drawn by a dual-signature PD shall not change faster than I_{Slewrate} defined in Table 145–28, in either polarity. This limitation applies after inrush has completed (see 145.3.8.3) and before the PD has disconnected.

145.3.8.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 145.2.8.3. A single-signature PD includes C_{Port} as defined in Table 145–28. A dual-signature PD includes $C_{\text{Port-2P}}$ as defined in Table 145–28 on each pairset.

The following PD configurations intrinsically meet the requirements in this subclause:

- Single-signature Type 3 PDs with peak power not exceeding $P_{\text{Class\_PD}}$, and with an input capacitance of 180 µF or less
- Single-signature Type 4 PDs with peak power not exceeding $P_{\text{Class\_PD}}$, and with an input capacitance of 360 µF or less
- Dual-signature Type 3 PDs with peak power draw not exceeding $P_{\text{Class\_PD-2P}}$, and with an input capacitance of 110 µF or less per pairset
- Dual-signature Type 4 PDs with peak power draw that does not exceed $P_{\text{Class\_PD-2P}}$ and with an input capacitance of 180 µF or less per pairset

Table 145–29—Transient conditions

PD Type	Transient condition	Initial voltage	Final voltage	Source dv / dt	Source resistance	Source current
3, 4	TR1	$V_{\text{Port\_PSE-2P}}$ min	56 V	2250 V/s	R_{Ch} ± 2.5%	Limited by Equation (145–30)
3, 4	TR2	$V_{\text{Port\_PSE-2P}}$ min	$V_{\text{Port\_PSE-2P}}$ min + 2.5 V	3.5 V/µs	1.5 Ω ± 2.5%	> 5 A capability

Table 145–29 defines two PSE transient conditions and PD Types to which these apply. Figure 145–33 shows operating bounds for the transients in Table 145–29. The shaded regions begin with the application of the transient and end at the times indicated in the Figure. These shaded regions can exceed normal operating limits and are not included in the average and peak operating power requirements set forth in Table 145–28.