TDL #275 and #276 D2.1

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

1. Make the following changes:

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (~~Zo_port~~Zo_pse), the cable impedance (Zc), the PD input port circuitry impedance (~~Zpd_cir~~Zcir_pd) and the PD EMI output filter impedance (Z_emi) should be lower than the PD power supply input impedance (Zin_ps_pd). All the above impedances are converted to the equivalent series impedance form as described by Figure 33A-1. ~~This sub-clause focuses on the PSE part.~~ [Redundant: It is in the title]

PSE ~~Port~~PI output impedance consists of two parts:

— PSE power supply output impedance (Zo_ps), which is a function of the load at the PSE PI~~(PPort)~~, and
— the ~~Series~~series elements (Z_ser) that connect the PSE power supply output to the PSE PI~~port~~.

Therefore, the total PSE PI ~~Port~~ output impedance during normal powering mode is ~~Zo_port~~Zo_pse=Zo_ps+Z_ser.

In order to maintain PSE-PD stability, the following guidelines apply:

— Zo_ps max = 0.3 Ω~~.~~ at frequencies up to 100 kHz at the highest PClass ~~-~~that the PSE supports, as defined in Table 33–13. If the PSE is loaded with less than the required Pclass max defined by the PD required class and the channel power loss as defined by PClass max, then Zout_ps_max =0.3Ω x PClass max / Pclass.

Zo_ps can be extracted from ~~Zport~~Zo_port by measuring ~~VPort_2P~~ VPort_PSE-2P / IPort (with an external power dynamic analyzer system) as a function of frequency and subtracting from ~~Zport~~ Zo_port the value of Zser ~~(f = DC)~~ which is limited by the value of ~~Zser~~ Zo_ser at DC (low frequency).

— The value of Zo_ps is not limited if the following conditions are met simultaneously:
a) ~~If~~ Zo_ps < Zo_ser
b) ~~and~~ VPort_PSE-2P ~~VPort_2P~~ is kept ~~to~~ in the range of ~~VPort_2P~~ VPort_PSE-2P min and ~~VPort_2P~~ VPort_PSE-2P max as defined in Table 33–18 during dynamic load changes from 10 Hz to 100 kHz.~~, then the value of Zo_ps is not limited~~.

Verification of these guidelines can be made by measuring the PSE PI ~~port~~ output impedance from 10 Hz to 100 kHz with the maximum load per the PSEs assigned Class, as defined in Table 33–13 at short cable length, or by performing simulations.

See Figure 33A–1 for the PSE-PD system impedance allocation.

2. Update Figure 33A-1 as follows:

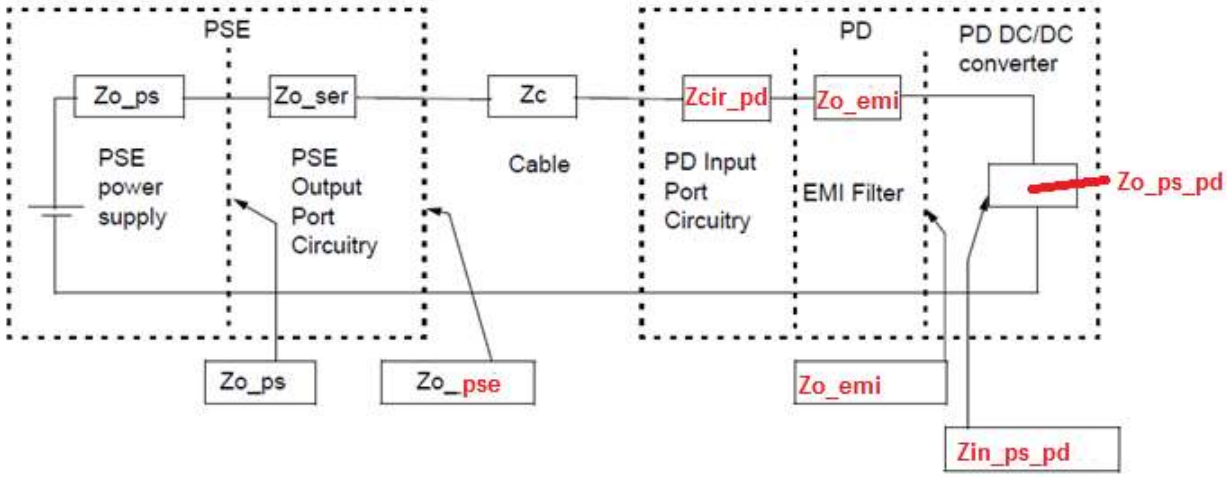

Figure 33A–1—PSE-PD system impedance allocation

~~See Figure 33A–2 for the test setup and Figure 33A–3 for the test requirements.~~

3. Delete Figure 33A-2 (no need to teach how to measure impedance of a port)
4. Delete Figure 33A-3 (the test requirements are in the text)
5. Make the following changes:

33A.2 Recommended PD design guidelines

PD ~~port~~ PI input impedance consists of the following two parts:

— PD PI ~~port~~ input circuits Zcir_pd and ~~including~~ the EMI filter ~~(Zin_ser)~~Z_emi, and

— PD power supply input impedance ~~(Zin_ps_pd)~~Zin_ps_pd.~~, which is fed by the output of the EMI filter (Zo_emi).~~

In order to maintain stability with the PSE, the PD power supply input impedance Zin_ps_pd ~~(Zin_ps_pd)~~ should be higher than the output impedance of the total network precede it (Zo_emi+Zcir_pd+Zc+Zo_pse). ~~including the PD EMI output filter impedance fed by the channel output impedance, which is fed by the PSE port output impedance.~~

The worst-case scenario is when the channel length is zero (in terms of lower damping factor).

The access to the PD input power supply is not possible through the PD port for evaluating the various impedances in the PD and derivation of the above individual impedances~~parameters~~. The following guidelines are recommended when measuring the PD input impedance:

— The PD power supply input impedance (Zin_ps_pd) at Pclass_PD~~max load of PPort_PD = PPort_PD max~~ as defined in Table 33–30 should be higher than 30 Ω at any frequency up to the PD power supply crossover closed loop frequency. If the PD power supply is consuming less than its maximum power capability defined by its required class PClass_PD max, ~~PPort_PD = PPort_PD max~~ as defined in Table 33–30, then Zin_ps_pd min = 30 x PClass_PD max ~~PPort_PD~~ max / ~~PPort_PD~~Pclass_PD.

— The PD power supply EMI filter output impedance should be Zo_emi = 2.7 Ω max. If the PD power supply is consuming less than PClass_PD max~~PPort_PD = PPort_PD max~~, then Zo_emi = 2.7 x PClass_PD max ~~PPort_PD max~~ / Pclass_PD~~PPort_PD~~.

See Figure 33A–1 for the PSE-PD system impedance allocation.

End of Baseline

The following is a clean version with out markups.

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (Zo_pse), the cable impedance (Zc), the PD input port circuitry impedance (Zcir_pd) and the PD EMI output filter impedance (Z_emi) should be lower than the PD power supply input impedance (Zin_ps_pd). All the above impedances are converted to the equivalent series impedance form as described by Figure 33A-1. [Redundant: It is in the title]

PSE PI output impedance consists of two parts:

— PSE power supply output impedance (Zo_ps), which is a function of the load at the PSE PI, and
— the series elements (Z_ser) that connect the PSE power supply output to the PSE PI.

Therefore, the total PSE PI output impedance during normal powering mode is Zo_pse=Zo_ps+Z_ser.

In order to maintain PSE-PD stability, the following guidelines apply:

— Zo_ps max = 0.3 Ω at frequencies up to 100 kHz at the highest PClass that the PSE supports, as defined in Table 33–13. If the PSE is loaded with less than the required Pclass max defined by the PD required class and the channel power loss as defined by PClass max, then Zout_ps_max =0.3Ω x PClass max / Pclass.

Zo_ps can be extracted from Zo_port by measuring VPort_PSE-2P / IPort (with an external power dynamic analyzer system) as a function of frequency and subtracting from Zo_port the value of Zser which is limited by the value of Zo_ser at DC (low frequency).

— The value of Zo_ps is not limited if the following conditions are met simultaneously:
  a) Zo_ps < Zo_ser
  b) VPort_PSE-2P is kept in the range of VPort_PSE-2P min and VPort_PSE-2P max as defined in Table 33–18 during dynamic load changes from 10 Hz to 100 kHz..

Verification of these guidelines can be made by measuring the PSE PI output impedance from 10 Hz to 100 kHz with the maximum load per the PSEs assigned Class, as defined in Table 33–13 at short cable length, or by performing simulations.

See Figure 33A–1 for the PSE-PD system impedance allocation.

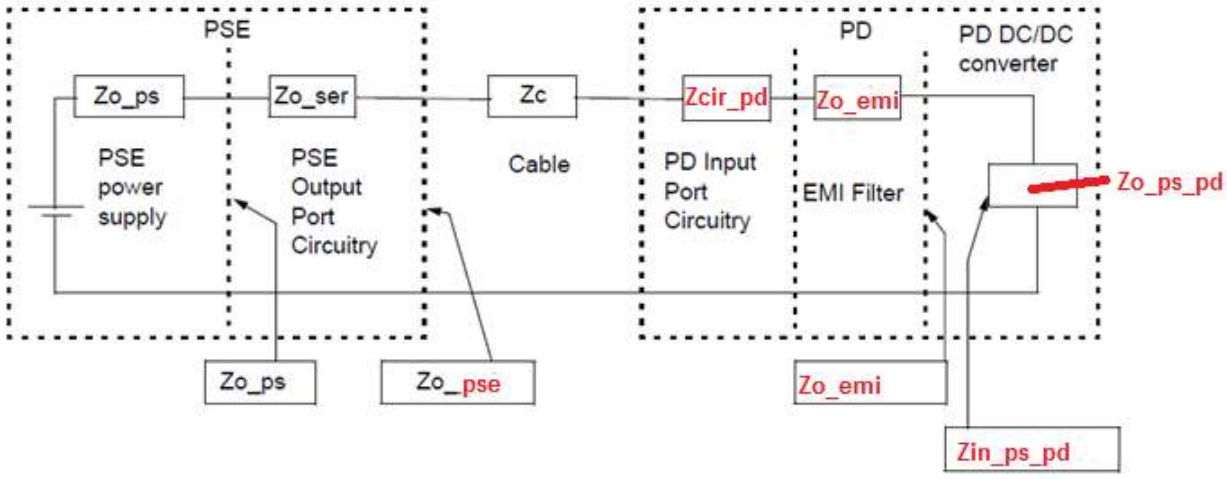

Figure 33A–1—PSE-PD system impedance allocation

33A.2 Recommended PD design guidelines

PD PI input impedance consists of the following two parts:

— PD PI input circuits Zcir_pd and the EMI filterZ_emi, and

— PD power supply input impedanceZin_ps_pd.

In order to maintain stability with the PSE, the PD power supply input impedance Zin_ps_pd should be higher than the output impedance of the total network precede it (Zo_emi+Zcir_pd+Zc+Zo_pse).

The worst-case scenario is when the channel length is zero (in terms of lower damping factor).

The access to the PD input power supply is not possible through the PD port for evaluating the various impedances in the PD and derivation of the above individual impedances. The following guidelines are recommended when measuring the PD input impedance:

— The PD power supply input impedance (Zin_ps_pd) at Pclass_PDas defined in Table 33–30 should be higher than 30 Ω at any frequency up to the PD power supply crossover closed loop frequency. If the PD power supply is consuming less than its maximum power capability defined by its required class PClass_PD max, as defined in Table 33–30, then Zin_ps_pd min = 30 x PClass_PD max max / Pclass_PD.

— The PD power supply EMI filter output impedance should be Zo_emi = 2.7 Ω max. If the PD power supply is consuming less than PClass_PD max, then Zo_emi = 2.7 x PClass_PD max / Pclass_PD.

See Figure 33A–1 for the PSE-PD system impedance allocation.