PD Behavior during PSE Transient D1.2 comment # 232, v3

Fred Schindler, Seen Simply

33.3.7.6 PD behavior …

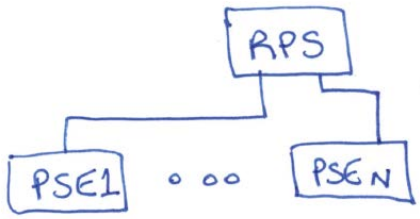
- This section exists to ensure that the PSE does not remove power from the PD during a PSE transient.
- This section was added when Type 2 devices were defined.
- This section may be used provide PD requirements during PSE increasing (original case) and decreasing voltages (text added during D1.1, which ensures PD has adequate stored energy).

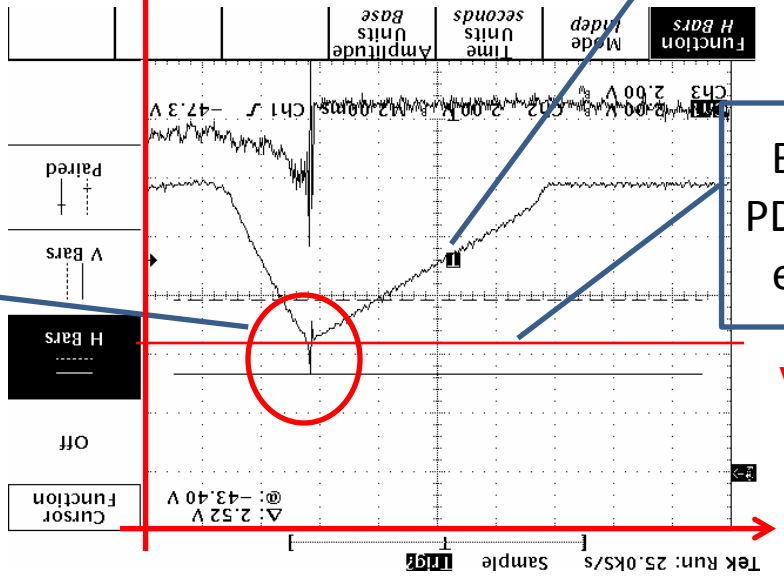
33.3.7.6 System View

This section results in a quantifiable load transient for a multiport PSE system so that the system power supply can be specified.

PSE Transient

- One failed PSE supply is backed up by a remote power supply (RPS).





1

Transient affects Ethernet data integrity.

2

Rise in voltage causes PD to draw current to charge Cpd.

3

Below VPSE_MIN the PD capacitance supplies energy to PD circuits.

Waveform from schindler_1_0107, IEEE 802.3at development effort.

System behavior

- The PSE provides current limit ILIM for up to TLIM. 2
- The PD is not required to provide a current limit unless it exceeds a specific bulk capacitance value.
- A higher channel resistance increases the time for the PD bulk capacitance to reach its voltage. 2
- A lower channel resistance increases the peak current that charges the PD bulk capacitance. The PD is tested for a possible PSE transient response. 1

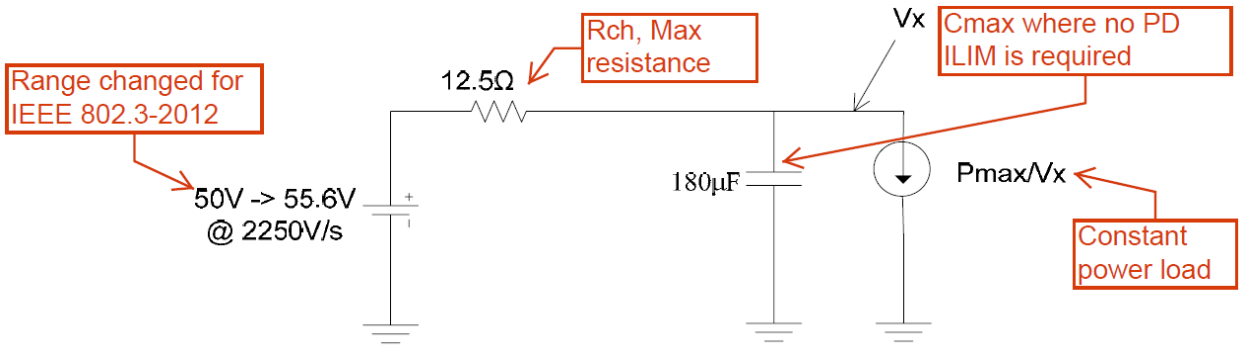
33.3.7.6 PD behavior … 2

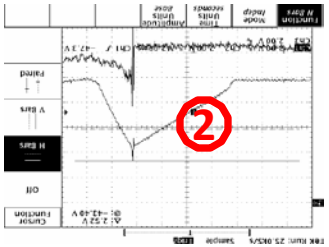
33.3.7.6 PD behavior during transients at the PSE PI

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

2

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after T_{LIM} min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.





Drawing from vetteth_1_0911, IEEE 802.3at development effort.

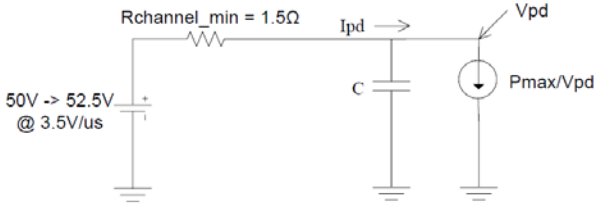
33.3.7.6 PD behavior … 1

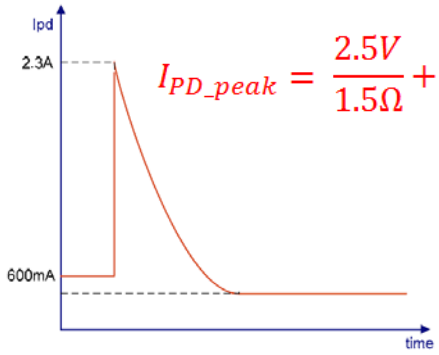
33.3.7.6 PD behavior during transients at the PSE PI

A Type 2 PD shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 Ω, and a source that supports a current greater than 2.5 A. 1

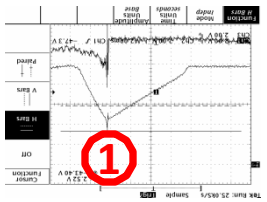
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance is R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI I_{LIM} per Equation (33–14). 2





$$I_{PD\_peak} = \frac{2.5V}{1.5\Omega} + \frac{P_{Class\_PD}}{V_{PD\_min}} = 1.67 + \frac{25.5W}{42.5V} = 2.3A$$

- **The PD input capacitor can be any value.**



Drawing from vetteth_1_0911, IEEE 802.3at development effort.

Review

- Transients above 3.5V/us may affect Ethernet data integrity. A PSE will limit dv/dt below this level. PD requirement (1) prevents the PSE from exceeding ILIM after TLIM.

- Equipment tests established dv/dt rates for (2) are less than 2,250 V/s and requirement (2) prevents the PSE from exceeding ILIM after TLIM.

New PD Types

- 4-pair powering , increases current limits and halves Rch for the PI. Current P2P unbalance may exist. The requirement should be written for a powered PD Mode demand.

- Type-3 PDs
  - Class-6 is 51.0 W, Extended power is 60.0 W
  - 180 uF, TLIM = 10 ms

- Type-4 PDs
  - Class-8 is 71.0 W, Extended power is 90.0 W
  - 360 uF, TLIM = 6 ms, Start at 52 V.

33.3.7.6 PD behavior …

- The existing PD static operating mask is for the total PD power.
- DS PD are should have the same class value on each Mode. DS PDs were tested the same as SS PDs.

Replace Figure 33-18 with the following figure:

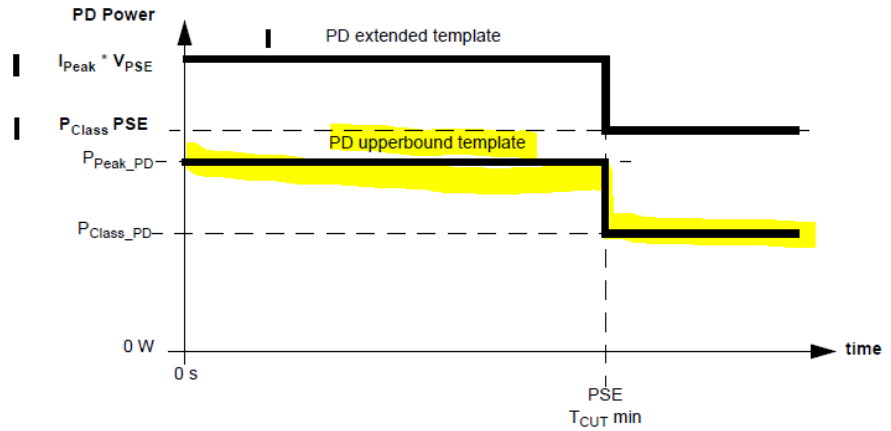


Figure 33–18—PD static operating mask

New PD Types Test Setup

- Both PD Modes are driven for PD Types that provide 4-pair power.
- Each PD Mode sees the same resistance as the two pair test because half the test current flows through each pair set.
- Current unbalance is not considered and tests resistances on each pairset should be equal.
- The source current limit is doubled when a single source is used.

Problems Encountered

- D1.2 does not provide a scale factor to get PpeakPD for class 6, and classes 7 and 8 when they are not Extended.
- Recommend that these be added to Table 33-18 and use a scale factor of 1.05.
- Note that an Autoclass extension being proposed by Lennart of Philips, should enable PDs to be placed in their maximum power consuming state.

New PD Types Simulations

- Test 1 results passes for all Types including for extended classes.
  - The peak current seen for higher-power PDs was lower than estimated.
- Test 2 results show significant margin for all Types including for extended classes.

Proposed baseline text
33.3.7.6 D1.2 page 275

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 or Type 3 PD with peak power draw that does not exceed PClass_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 4 PD with peak power draw that does not exceed PClass_PD max and has an input capacitance of 360 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after TLIM min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from VPort_PSE min to VPort_PSE max at limit 2250 V/s.

Proposed baseline text, continued 33.3.7.6 D1.2 page 275

A Type 2, Type 3, and Type 4 PD that demand less than class 5 power levels shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from VPort_PSE_min~~50 V~~ to VPort_PSE_min +~~5~~2.5 V at greater than 3.5 V/µs, a source impedance ~~of~~ within 2.5% of 1.5 Ω, and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance within 2.5% of ~~is~~ RCh (see Table 33–1), and the voltage source limits the current

to MDI ILIM-2P per Equation (33–14).

Proposed baseline text, continued 33.3.7.6 D1.2 page 275

A Type 3 or Type 4 PD that demands class 5 power levels shall meet both of the following:

a) The PD Mode input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template value (see Figure 33–18) within 4 ms. During this test, both PD Modes voltage are driven from VPort_PSE min to VPort_PSE min +2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE min to 56 V at 2250 V/s, the source impedance within 2.5% of RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM-2P per Equation (33–14).

Note that this is all new text. Red highlights how legacy Type-2 text was changed to accommodate new PD Types.

Proposed baseline text, continued 33.3.7.6 D1.2 page 275

A Type 3 or Type 4 PD that demand more than class 5 power levels shall meet both of the following:

a) The PD Mode input current spike shall not exceed 3.0 A and shall settle below the PD extended template value (see Figure 33–18) within 4 ms. During this test, both PD Modes voltage are driven from VPort_PSE min to VPort_PSE min +2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE min to 56 V at 2250 V/s, the source impedance within 2.5% of RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM-2P per Equation (33–14).

Note that this is all new text. Yellow highlights how the text on the previous page was changed to accommodate new PD Types.

Proposed baseline text, continued D1.2 page 275 lines 16 to 21

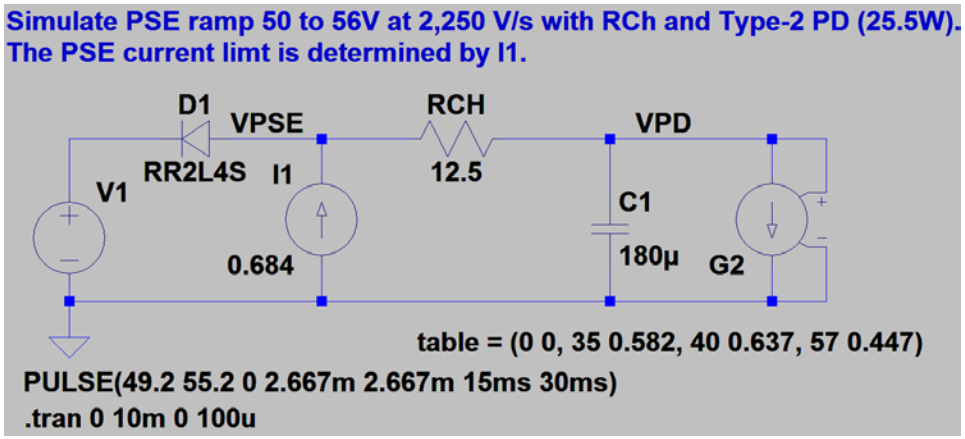
Type 1, Type 2, and single-signature Type 3 PDs with classes 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9. Type 3 dual-signature PDs with class 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9 for each pairset. For class 5 and 6 single-signature PDs, ~~if~~ CPort_min shall be ≥ 10µF~~,~~ to support transient behavior ~~has no further requirements~~. For dual-signature class 5 PDs, this recommendation applies to each pairset. For class 7 and 8 single signature PDs, ~~if~~ CPort min shall be ≥ 20µF~~,~~ to support transient behavior ~~has no further requirements~~. See 33.2.7.2 (TBD) or the transient conditions.

Strike Editor's Note,
"2. A drop out specification needs to be added to this section that requires PDs to ride out PSE transients. This is in place of increasing Cport.

Seen Simply

Turning complexity into understanding.

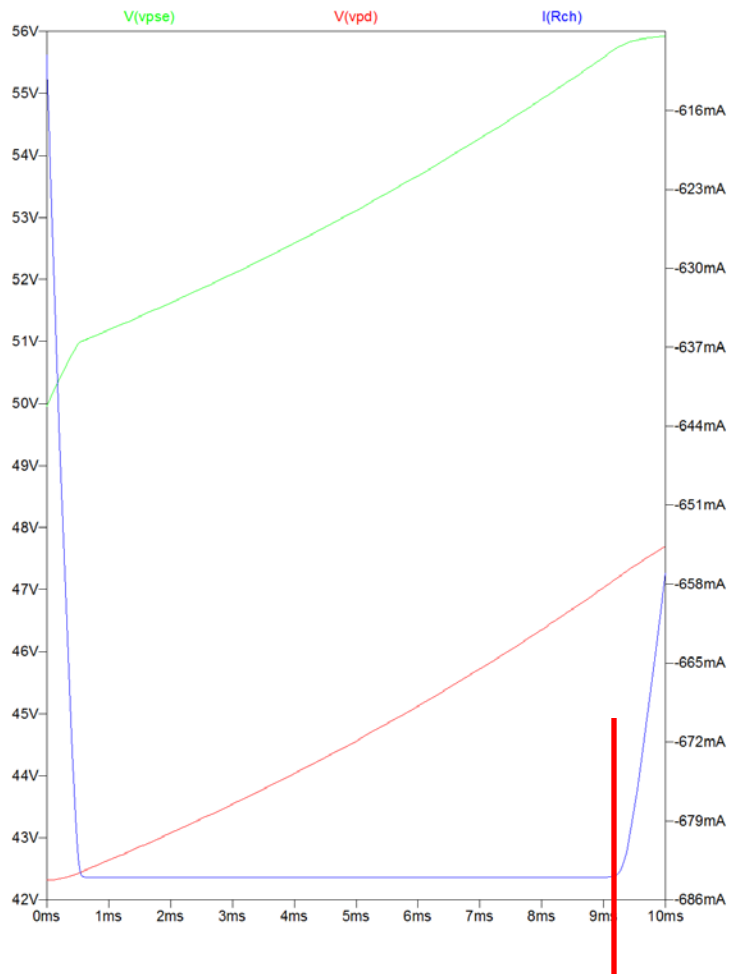
Type-2 PD, 2,250V Ramp



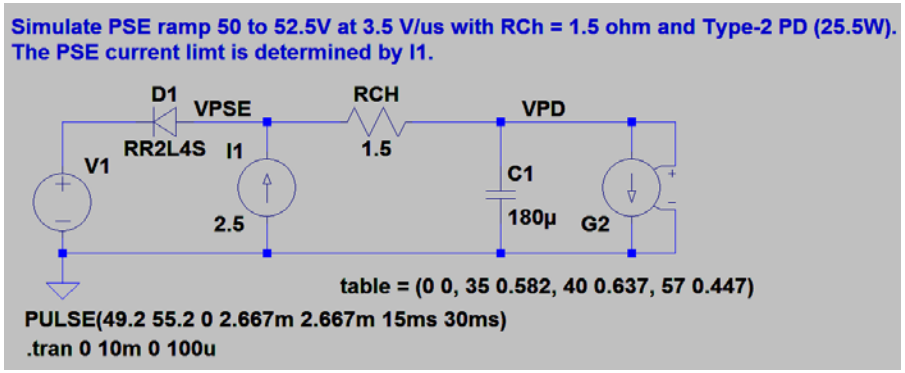
TLIM_MIN = 10 ms
ILIM_MIN = 0.684 A

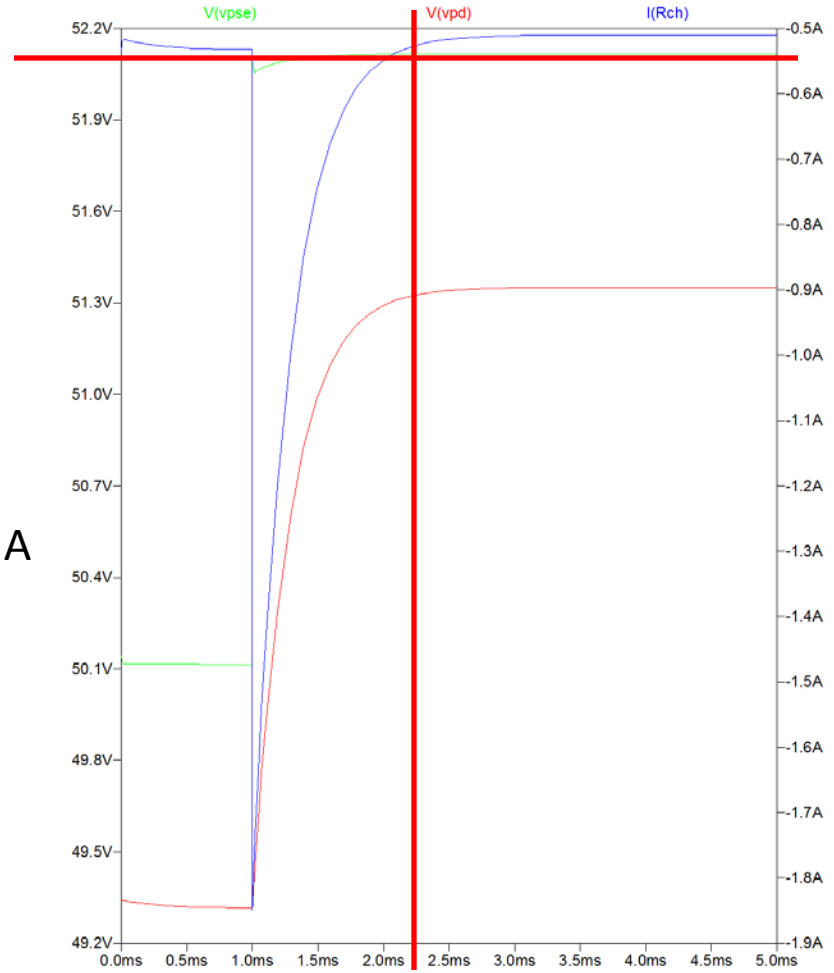
Note that current is higher at the bottom of the graph.

Special thanks to Jean Picard and Dave Dwelley For their input on SPICE simulations.



Type-2 PD, 3.5V/us Ramp





Ppeak_PD = 28.3 W, I = 28.3W/52.5V = 0.539 A

Subtract 1 ms from a scale value
to get the actual value.

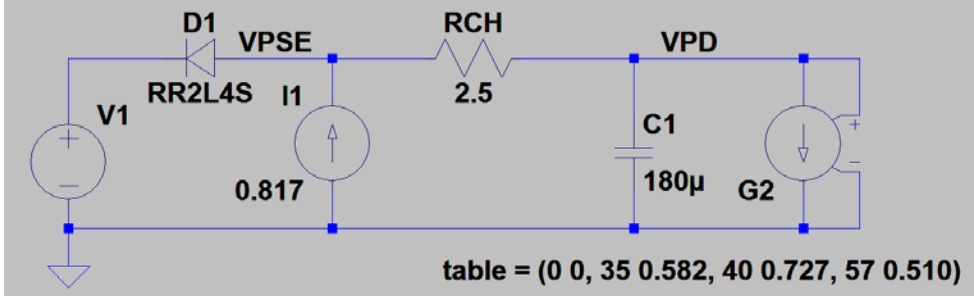
Type-3 PD

Type 3 systems provide 2x Type 2 system but the power limits match on PD Modes.

Type	Class	Power	Rs	PPD	VPD_MIN	Estimated Ipeak	Simulated Ipeak
		W	Ω	W	VPD_MIN	A	A
2	4	2P	1.5	25.5	42.5	2.3	1.9
3	5	4P	1.5	35.5	44.3	2.1	
3	6	4P	1.5	51.0	42.5	2.3	1.9
3E	6E	4P	1.5	< 60			2.2
4	7	4P	1.5	62.0	42.9	2.4	
4	8	4P	1.5	71.0	41.2	2.5	2.3
4E	8E	4P	1.5	< 90			2.4

Type-3 Extended PD, 2,250V Ramp

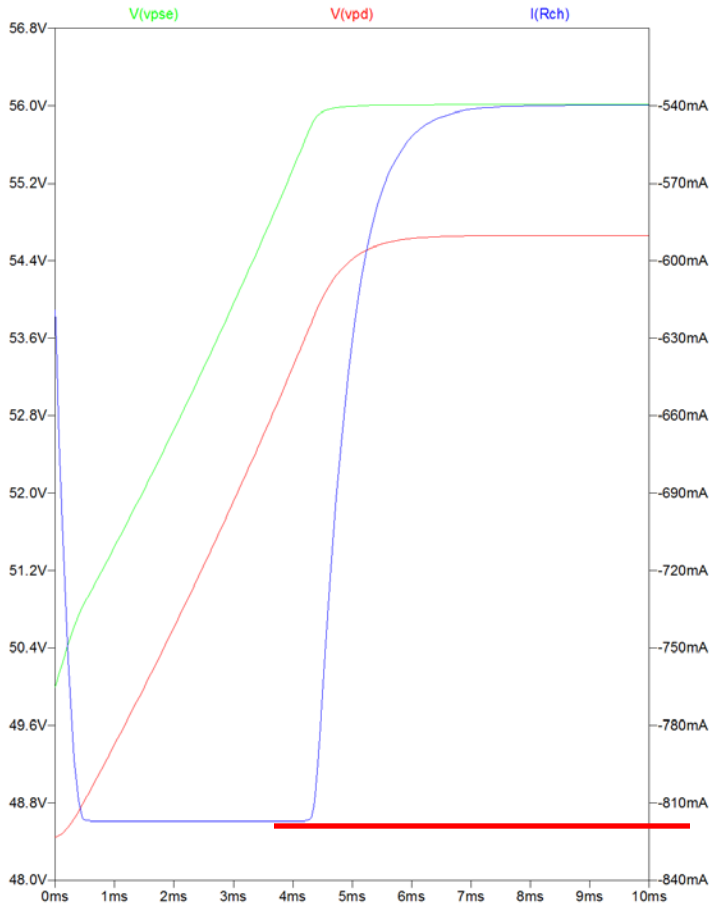
Simulate PSE ramp 50 to 56V at 2,250 V/s with RCh and Type-3E PD (58.2W).
~20 m of cable.
The PSE current limt is determined by I1.



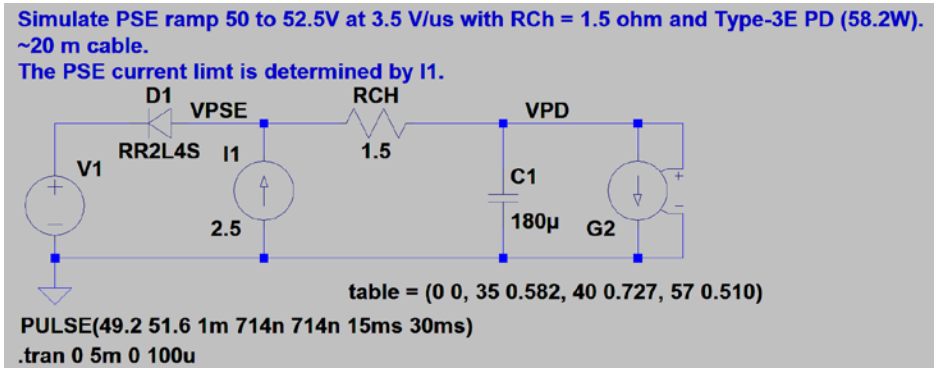
PULSE(49.2 55.2 0 2.667m 2.667m 15ms 30ms)
.tran 0 10m 0 100u

TLIM = 10 ms
2x ILIM-2P_MIN = 2x 0.817 = 1.63 A

This passes with more margin because Rch is less than worst-case.



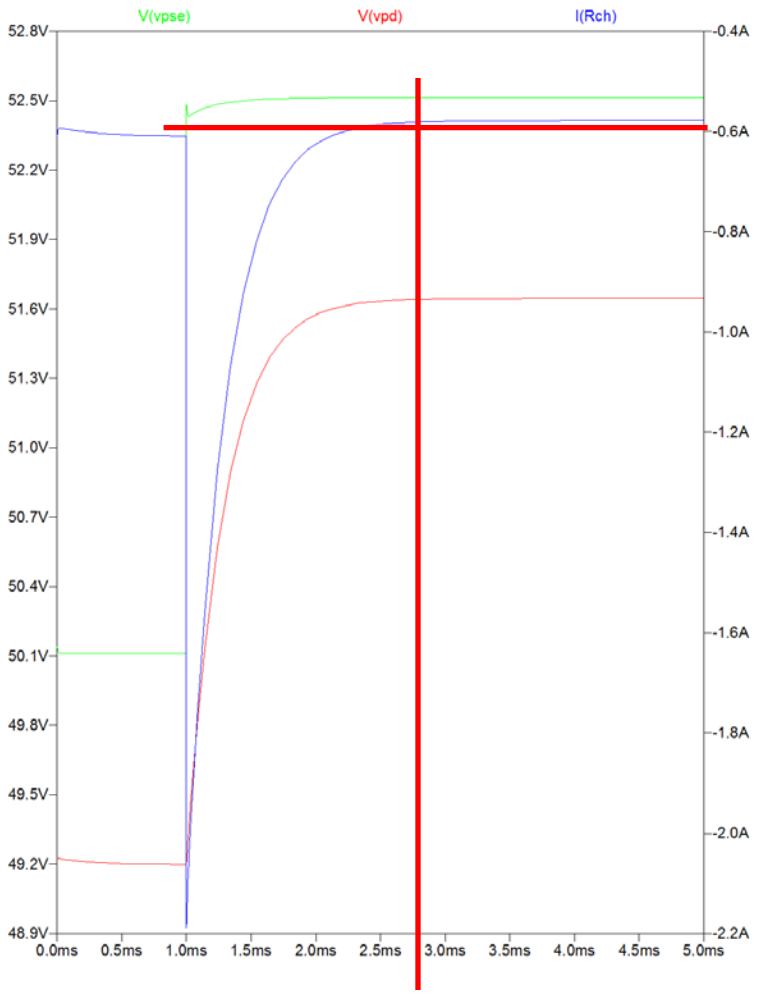
Type-3 Extended PD, 3.5 V/us Ramp



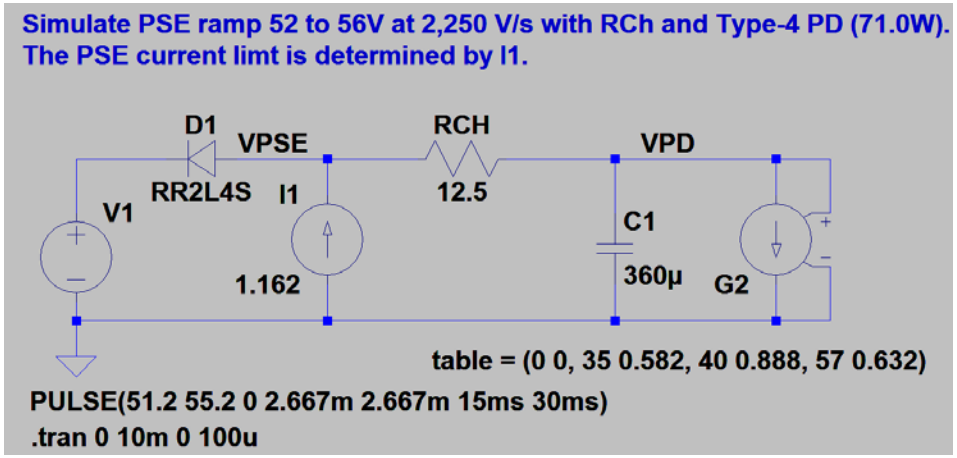
Ppeak_PD = 1.05 x PCLASS_PD
= 61.1 W, I = 61.1W/51.6V = 1.18 A = 0.59 A

Note PD is drawing less than Ppeak_PD.

Subtract 1 ms from a scale value
to get the actual value.

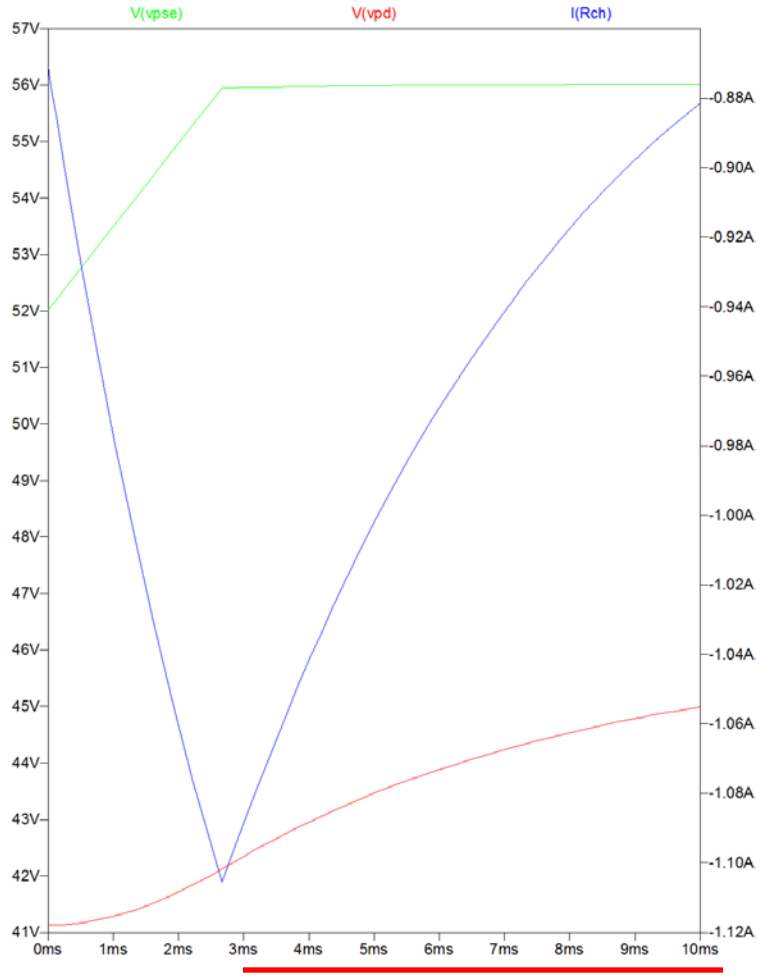


Type-4 PD, 2,250V Ramp

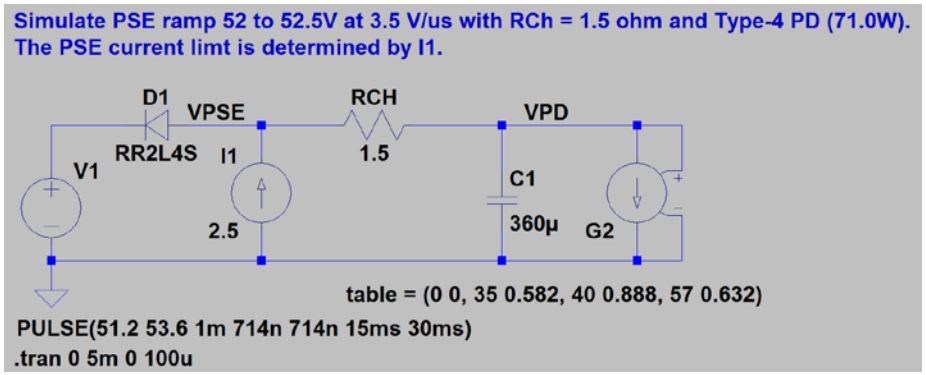


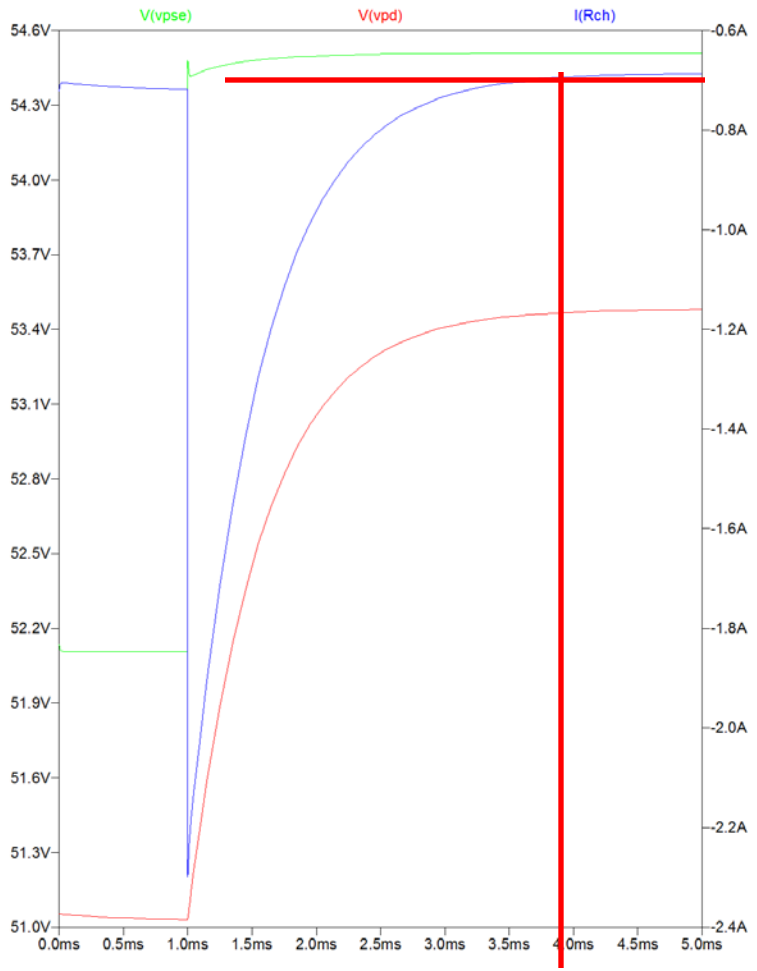
TLIM_MIN = 6 ms

2x ILIM-2P_MIN = 2x 1.162 = 2.32 A



Type-4 PD, 3.5 V/us Ramp





Ppeak_PD = 1.05 x PCLASS_PD
= 74.6 W, I = 74.6W/53.5V = 1.39 A = 2x 0.695 A
This is nonExtended class 8.

The PD draw ~73.7 W at 4 ms

Subtract 1 ms from graph value
to get actual time from the ramp start.

Type-4 Extended PD, 2,250V Ramp

Simulate PSE ramp 52 to 56V at 2,250 V/s with RCh and Type-4 PD (86.3 W).
~20 m cable.
The PSE current limt is determined by I1.

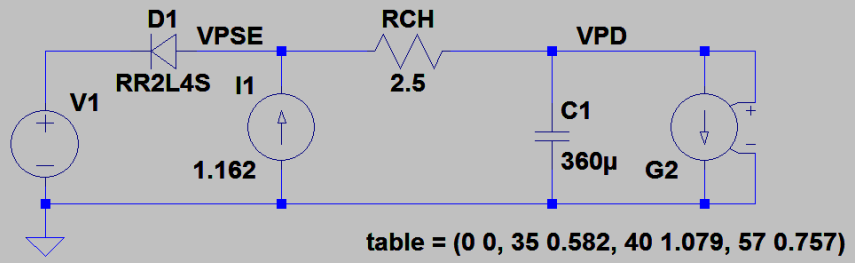
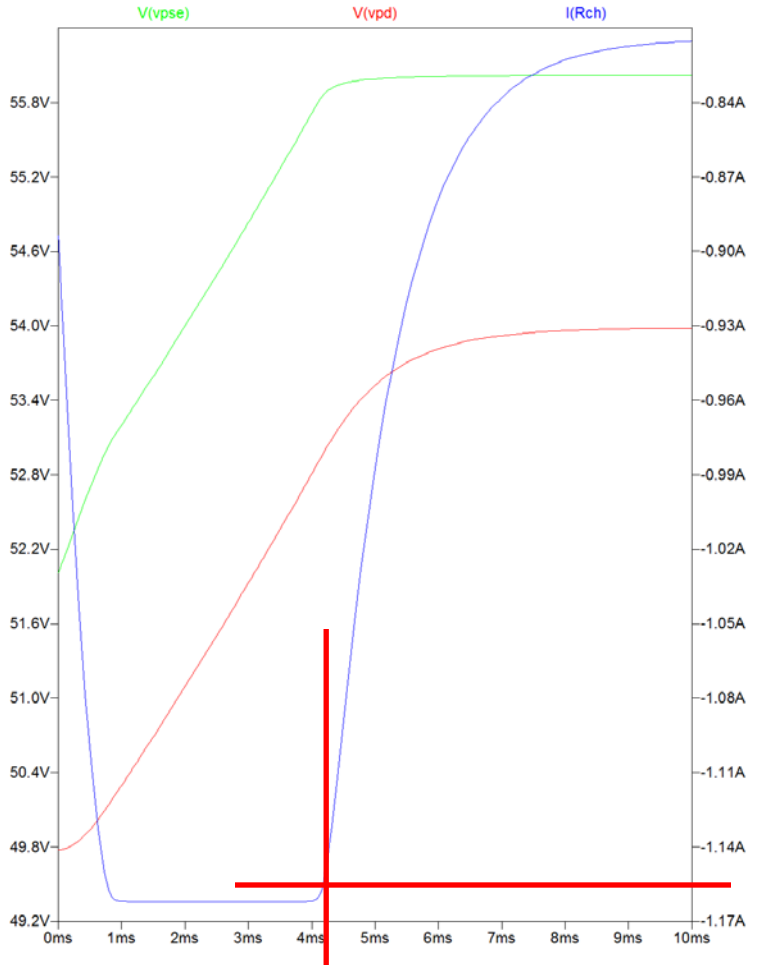


table = (0 0, 35 0.582, 40 1.079, 57 0.757)

PULSE(51.2 55.2 0 2.667m 2.667m 15ms 30ms)
.tran 0 10m 0 100u

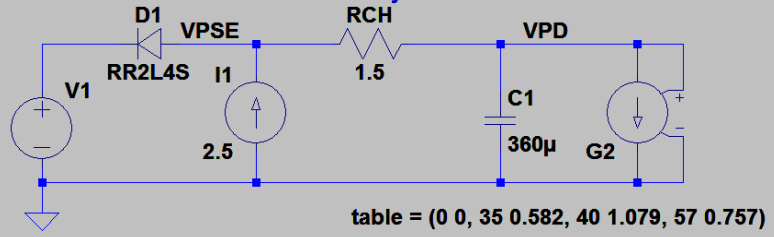


TLIM_MIN = 6 ms

2x ILIM-2P_MIN = 2x 1.162 = 2.32 A

Type-4 Extended PD, 3.5 V/us Ramp

Simulate PSE ramp 52 to 52.5V at 3.5 V/us with RCh = 1.5 ohm and Type-4 PD (86.3 W).
~20 m cable.
The PSE current limt is determined by I1.



PULSE(51.2 53.6 1m 714n 714n 15ms 30ms)
.tran 0 5m 0 100u

Ppeak_PD = 1.05 x PCLASS_PD
= 1.05 x 86.3 W, I = 90.6 W/53.3V
= 1.7 A = 2x 0.85 A

The PD draw ~87.8 W at 4 ms

Subtract 1 ms from graph value
to get actual time from the ramp start.