DC MPS

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Presentation Objectives

- Create an implementable set of rules
  - Clean up inconsistencies
  - Improve clarity
- Clearly sort requirements into
  - Type 1 and 2
  - Type 3 and 4, connected to single-signature PD
  - Type 3 and 4, connected to dual-signature PD

New DC MPS Requirements Have Become Polluted by Insertion

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is in the range of I_{Hold}.

The values of $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity and the corresponding values of I_{Hold} shall meet the conditions specified in Table 33–11.

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall monitor either the sum of $I_{port-2P}$ of both pairs of the same polarity or the pairset with the highest $I_{Port-2P}$ current value and use the appropriate I_{Hold} level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD shall monitor each pairset and use the appropriate I_{Hold} level shown in Table 33–11. The PSE shall remove power from any pairset on which the DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when *$I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max* continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Statements have been introduced in a manner that does not clearly differentiate Type 1 and 2 PSEs from Type 3 and 4 PSEs, when connected to single- and dual-signature PDs. Requirements are overlapping in ways that become difficult to meet.

Original 802.3at DC MPS Text

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if I_{Port} is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if I_{Port} is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of I_{Hold}.

Definition of DC MPS Present and DC MPS Absent

Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

Rule for Removing Power

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when I_{Port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Rule for Maintaining Power

Original Text followed a straight-forward template

Suggested New Text – Outline

33.2.9.1.2 PSE DC MPS component requirements

Header

Type 1 and 2
DC MPS Present/Absent Definitions
Power Removal Rule
Power Maintenance Rule

Type 3 and 4, connected to single-signature PD
DC MPS Present/Absent Definitions
Power Removal Rule
Power Maintenance Rule

Type 3 and 4, connected to dual-signature PD
DC MPS Present/Absent Definitions
Power Removal Rule
Power Maintenance Rule

Footer

The following slides attempt to capture the intent of the Task Force in the Present/Absent definitions and Power Removal/Maintenance rules.

Suggested New Text – Header

33.2.9.1.2 PSE DC MPS component requirements

All types of PSE, depending on the connected type of PD, will use the applicable I_{Hold} min, I_{Hold} max, T_{MPS} and T_{MPDO} values as defined in Table 33–11. The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component.

Reference Table 33-11 once

Improved 802.3at DC MPS Text

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if I_{Port} is greater than or equal to I_{Hold} max continuously for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if I_{Port} is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of I_{Hold}.

Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the PI ~~port~~ when ~~I_{Port} is greater than or equal to I_{Hold} max~~ DC MPS has been present ~~continuously for at least T_{MPS}~~ every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Definition of DC MPS Present and DC MPS Absent

Rule for Removing Power

Rule for Maintaining Power

The 802.3 starting point text can be improved

1) **Referencing the DC MPS Present definition**
   a) **Otherwise the DC MPS Present definition is unused**
2) **Change port to PI for clarity and consistency**
3) **Remove redundant “for at least/a minimum of T_{MPS}”**

Suggested New Text – Type 1 and 2 Section

A Type 1 and 2 PSE shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}. A Type 1 and 2 PSE shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ is less than or equal to the applicable I_{Hold} min. A Type 1 and 2 PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of the applicable I_{Hold}.

Definition of DC MPS Present and DC MPS Absent

Type 1 and 2 PSEs shall remove power ~~shall be removed~~ from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

Rule for Removing Power

A Type 1 and 2 PSE shall not remove power from the ~~port~~ PI when ~~I_{port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS}~~ DC MPS has been present every T_{MPS} + T_{MPDO}~~, as defined in Table 33–11~~.

Rule for Maintaining Power

Selected Old Text – Type 3 and 4, Single-sig PD Section

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is in the range of I_{Hold}.

The values of $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity and the corresponding values of I_{Hold} shall meet the conditions specified in Table 33–11.

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall monitor either the sum of $I_{port-2P}$ of both pairs of the same polarity or the pairset with the highest $I_{Port-2P}$ current value and use the appropriate I_{Hold} level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD shall monitor each pairset and use the appropriate I_{Hold} level shown in Table 33–11. The PSE shall remove power from any pairset on which the DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when *$I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max* continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Definition of DC MPS Present

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be present if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{port-2P}$ of both pairsets of the same polarity is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}.

Definition of DC MPS Absent

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be absent if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity are less than or equal to the applicable I_{Hold} min.

Rule for Removing Power

Type 3 and 4 PSEs, when connected to a single-signature PD, shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

Rule for Maintaining Power

Type 3 or Type 4 PSEs, when connected to a single-signature PD, shall not remove power from the PI when DC MPS has been present every T_{MPS} + T_{MPDO}.

Rebuilt New Text – Type 3 and 4, Single-sig PD Section

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be present if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}. A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be absent if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity are less than or equal to the applicable I_{Hold} min. A Type 3 or Type 4 PSE, when connected to a single-signature PD, may consider the DC MPS component to be either present or absent if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity is within the range of the applicable I_{Hold}.

Type 3 and 4 PSEs, when connected to a single-signature PD, shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

Type 3 or Type 4 PSEs, when connected to a single-signature PD, shall not remove power from the PI when DC MPS has been present every T_{MPS} + T_{MPDO}.

Definition of DC MPS Present

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be present if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{port-2P}$ of both pairsets of the same polarity is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}.

Definition of DC MPS Absent

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be absent if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity are less than or equal to the applicable I_{Hold} min.

Rule for Removing Power

Type 3 and 4 PSEs, when connected to a single-signature PD, shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

Rule for Maintaining Power

Type 3 or Type 4 PSEs, when connected to a single-signature PD, shall not remove power from the PI when DC MPS has been present every T_{MPS} + T_{MPDO}.

Selected Old Text – Type 3 and 4, Dual-sig PD Section

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is in the range of I_{Hold}.

The values of $I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity and the corresponding values of I_{Hold} shall meet the conditions specified in Table 33–11.

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall monitor either the sum of $I_{port-2P}$ of both pairs of the same polarity or the pairset with the highest $I_{Port-2P}$ current value and use the appropriate I_{Hold} level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD shall monitor each pairset and use the appropriate I_{Hold} level shown in Table 33–11. The PSE shall remove power from any pairset on which the DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when *$I_{Port-2P}$ or the sum of $I_{port-2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max* continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Definition of DC MPS Present

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present on a pairset if $I_{Port-2P}$ is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}.

Definition of DC MPS Absent

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be absent on a pairset if $I_{Port-2P}$ is less than or equal to the applicable I_{Hold} min.

Rule for Removing Power

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}.

Rule for Maintaining Power

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall not remove power from a pairset when DC MPS has been present on both pairsets every T_{MPS} + T_{MPDO}. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may maintain power on a pairset if DC MPS has been present on that pairset every T_{MPS} + T_{MPDO}.

Rebuilt New Text – Type 3 and 4, Dual-sig PD Section

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present or absent on a pairset independently from the other pairset. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present on a pairset if $I_{Port-2P}$ is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be absent on a pairset if $I_{Port-2P}$ is less than or equal to the applicable I_{Hold} min. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may consider the DC MPS component on a pairset to be either present or absent if $I_{Port-2P}$ is within the range of the applicable I_{Hold}.

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}.

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall not remove power from a pairset when DC MPS has been present on both pairsets every $T_{MPS} + T_{MPDO}$. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may maintain power on a pairset if DC MPS has been present on that pairset every $T_{MPS} + T_{MPDO}$.

Definition of DC MPS Present

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present on a pairset if $I_{Port-2P}$ is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}.

Definition of DC MPS Absent

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be absent on a pairset if $I_{Port-2P}$ is less than or equal to the applicable I_{Hold} min.

Rule for Removing Power

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}.

Rule for Maintaining Power

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall not remove power from a pairset when DC MPS has been present on both pairsets every $T_{MPS} + T_{MPDO}$. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may maintain power on a pairset if DC MPS has been present on that pairset every $T_{MPS} + T_{MPDO}$.

Suggested New Text – Footer

The DC MPS rules allow a PD to minimize its power consumption.

Conclusion

- DC MPS suggested text eliminates conflicting requirements
- DC MPS suggested text improves clarity
- Any unintentional modifications to DC MPS rules can be easily implemented on this textual baseline