Cl **33** *SC* *P* *L* # 19

Darshan, Yair — Microsemi

Comment Type **ER** *Comment Status* **D** *Editorial*

For the next draft, it is preferred to show the new editorial marks (insertions and deletions) in addition to the changing bars. It helps to see the changes without the need to compare two documents.

SuggestedRemedy

For next Drafts: show the new editorial marks (insertions and deletions) in addition to the changing bars.

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

We are replacing the whole clause, so the editing marks do not get shown.

I believe what you are asking for would create a bunch of work for our editor.

TFTD

Cl **1** *SC* **1** *P* **1** *L* **1** # 201

Yseboodt, Lennart — Philips

Comment Type **ER** *Comment Status* **X** *Editorial*

Do you want me to reset the change bars in Clause 33 for D1.8 ?

SuggestedRemedy

Indicate YES/NO.

Proposed Response *Response Status* **W**

TFTD

Cl **1** *SC* **1** *P* **1** *L* **1** # 202

Yseboodt, Lennart — Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

As we are preparing for D2.0 in July, we need to be getting rid of all Editor's Notes.

SuggestedRemedy

Remove all Editor's Notes that do not specifically say "remove prior to publication".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

If anyone has an editor's note they would like to see remain in the document (other than those sited in the suggested remedy), please make a note of it and be ready to let me know when we get to this comment.

TFTD

Cl **30** *SC* **30.12.2.1.18a** *P* **37** *L* **22** # 3

Anslow, Pete — Ciena

Comment Type **E** *Comment Status* **X** *Management*

Adding 30.12.2.1.18a, 30.12.2.1.18b, 30.12.2.1.18c, 30.12.2.1.18d means that Table 30-7 should be modified with new rows.
Similarly for 30.12.3.1.18a, 30.12.3.1.18b, 30.12.3.1.18c, 30.12.3.1.18d

SuggestedRemedy

Show additions to Table 30-7 for new subclauses.

Proposed Response *Response Status* **W**

Where is Table 30-7. I don't see it in our draft.

TFTD

Lennart to follow up

Cl **33** *SC* **33.2.5** *P* **56** *L* **7** # 218

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt11*

Updates to the PSE State Diagram

SuggestedRemedy

Adopt yseboodt_11_0516_psestatedia.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.5** *P* **56** *L* **13** # 83

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **A** *Pres: Schindler1*

Variable parameter_type is used in legacy text to indicate the PSE type powering the system so that the electrical parameters (ILIM) may be set based on the PSE Type. The value of parameter_type is not a constant (p61, L53) and is determined by mutual identification of the PSE and PD. The function set_parameter_type is used to set the electrical values based on table values. New Types have these same parameters (ILIM) set based on class rather than Type. The Type 3 and 4 state diagrams (SDs) do not facilitate setting parameters based on class or Type. Comment D1.6 #278 turn the Type 3 and 4 parameter_type variable into a constant. The Type 3 and 4 SD do not use this name to perform a purpose.

New PSE Types are required to do physical classification so the facility to change electrical parameters is not required or included in the Type 3 and 4 SD. Remove the unnecessary use of parameter_type in new text. This comment may be covered in schindler_3bt_01_05_16.

SuggestedRemedy

Strike lines 40 to 45 on page 65.

Response *Response Status* **C**

ACCEPT.

WFP

TFTD

Lennart to follow up.

Cl **33** *SC* **33.2.5.8** *P* **65** *L* **39** # 64

Lukacs, Miklos — Silicon Labs

Comment Type **E** *Comment Status* **X** *Pres: Lukacs*

A timing diagram showing the cconnection check sequences would help in understanding the text and would make the intent more clear.

SuggestedRemedy

See timing diagrams presentation (Lukacs)

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.5.8** *P* **65** *L* **40** # 219

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **A** *PSE SD*

original text: "parameter_type: Values:
3: Type 3 PSE parameter values
4: Type 4 PSE parameter values"

The legacy SD, uses PSE_TYPE for the purpose we
are now using parameter_type in the new SD.
We did this, because parameter_type is used in the DLL state machine. The link however between the DLL SM and the PSE SM needs to be properly looked at anyway and revised.

SuggestedRemedy

- Rename parameter_type to PSE_TYPE.
"PSE_TYPE
A constant indicating the Type of the PSE.
Values:
3: Type 3 PSE
4: Type 4 PSE"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 83

TFTD, YD, DS

Cl **33** *SC* **33.2.5.9** *P* **66** *L* **46** # 69

Picard, Jean — Texas Instruments

Comment Type **TR** *Comment Status* **A** *PSE SD*

The class_4PID_mult_events_sec variable is missing from the list of variables although it is used in the SM

SuggestedRemedy

Add the following variable from "Picard_03_0316.pdf" page 1:

"class_4PID_mult_events_sec:
A variable indicating if the PSE generates 3 class events on the secondary alternative to determine if the dual signature PD is a candidate for 4-pair power.
TRUE: the PSE generates at least 3 class events to determine if the PD is a candidate for 4-pair power.
FALSE: the PSE does not need to generate 3 class events to determine if the PD is a candidate for 4-pair power."

Response *Response Status* **C**

ACCEPT.

TFTD, YD, DS

Cl **33** *SC* **33.2.5.9** *P* **67** *L* **44** # 103

Stover, David — Linear Technology

Comment Type **T** *Comment Status* **D** *PSE SD*

The variable dll_4PID is redundant with pd_dll_power_type.

SuggestedRemedy

Remove dll_4PID. Replace logic in POWER_ON state as follows:
From: (dll_4PID + ((pd_req_pwr > 4) * (pse_avail_pwr > 4)) + (mr_pse_ss_mode = 1))
To: ((pd_dll_power_type > 2) + ((pd_req_pwr > 4) * (pse_avail_pwr > 4)) + (mr_pse_ss_mode = 1))

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD, FS, YD

Cl **33** *SC* **33.2.5.9** *P* **68** *L* **10** # 43

Johnson, Peter — Sifos Technologies

Comment Type **E** *Comment Status* **A** *PSE SD*

The definitions for Iport-2P-pri and Iport-2P-sec each finish with (see 33.2.8.6), but there is no mention of these variables in 33.2.8.6.

SuggestedRemedy

Remove the references to 33.2.8.6

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change 33.2.8.6 to 33.2.8.4

TFTD, YD

Cl **33** *SC* **33.2.5.9** *P* **70** *L* **18** # 144

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **A** *PSE SD*

pd_cls_4PID_pri:
This variable indicates that 4PID has been established by confirming that both pairsets have a valid detection signature and that a device classified as a Type 3 or Type 4 PD.

Does not mention on which Alternative.

SuggestedRemedy

pd_cls_4PID_pri:
This variable indicates that 4PID has been established on the Primary Alternative by confirming that both pairsets have a valid detection signature and that a device classified as a Type 3 or Type 4 PD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 104

TFTD, DS

Cl **33** *SC* **33.2.5.9** *P* **70** *L* **19** # 104

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **A** *PSE SD*

Definition of pd_cls_4PID_pri is inconsistent with assignment in PSE SD: "This variable indicates that 4PID has been established by confirming that both pairsets have a valid detection signature and that a device classified as a Type 3 or Type 4 PD."

SuggestedRemedy

Replace variable definition as follows: "This variable indicates that a device on the primary pairset classified as a Type 3 or Type 4 PD."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD.

See 144

Replace variable definition as follows: "This variable indicates that a device on the primary alternative classified as a Type 3 or Type 4 PD."

Rename variable as pd_cls_4Ptype_pri.

Cl **33** *SC* **33.2.5.9** *P* **70** *L* **25** # 105

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **A** *PSE SD*

Definition of pd_cls_4PID_sec is inconsistent with assignment in PSE SD: "This variable indicates that 4PID has been established by confirming that both pairsets have a valid detection signature and that a device classified as a Type 3 or Type 4 PD."

SuggestedRemedy

Replace variable definition as follows: "This variable indicates that a device on the secondary pairset classified as a Type 3 or Type 4 PD."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

See 173

Replace variable definition as follows: "This variable indicates that a device on the secondary alternative classified as a Type 3 or Type 4 PD."

rename variable pd_cls_4Ptype_sec.

Cl **33** *SC* **33.2.5.9** *P* **70** *L* **25** # 173

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *PSE SD*

pd_cls_4PID_sec:
This variable indicates that 4PID has been established by confirming that both pairsets have a valid detection signature and that a device classified as a Type 3 or Type 4 PD.

Does not mention on which Alternative.

SuggestedRemedy

pd_cls_4PID_sec:
This variable indicates that 4PID has been established on the Secondary Alternative by confirming that both pairsets have a valid detection signature and that a device classified as a Type 3 or Type 4 PD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 105

TFTD, DS

Cl **33** *SC* **33.2.5.9** *P* **70** *L* **39** # 221

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Schindler1*

original text: "Editors Note: Mutual identification will require a variable pd_power_type similar to pd_dll_power_ type."

SuggestedRemedy

Remove Editors note and replace it by:
pd_power_type
A control variable output by the PSE power control state diagram (Figure 33-49) that indicates the Type of PD as advertised through Physical Link Layer classification.
Values:
1: PD is a Type 1 PD or a Type 3 PD (default)
2: PD is a Type 2 PD, a Type 3 PD, or a Type 4 PD
3: PD is a Type 3 PD
4: PD is a Type 4 PD

Proposed Response *Response Status* **W**

I don't understand this remedy. How does it fit in with Figure 33-49? Why have you made the choices you did with the meaning of each value?

TFTD

WFP

Cl **33** *SC* **33.2.5.10** *P* **73** *L* **44** # 15

Darshan, Yair — Microsemi

Comment Type **ER** *Comment Status* **A** *Pres: Darshan11*

Missing link to Table 33-7 in the following text:
"tcc_timer
A timer used to monitor the duration of Connection Check."

SuggestedRemedy

Change from:
"tcc_timer
A timer used to monitor the duration of Connection Check."

To:
"tcc_timer
A timer used to monitor the duration of Connection Check. See Table 33–7."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 107.

TFTD

Cl **33** *SC* **33.2.5.11.** *P* **76** *L* **2** # 62

Lukacs, Miklos — Silicon Labs

Comment Type **E** *Comment Status* **D** *Pres: Yseboodt8*

mr pd autoclass refers to the signature seen during the first (long) class event, before the TACS window.

SuggestedRemedy

The PD classification signature seen before TACS min during the long first class event.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD, DS

Change variable name to "mr_pd_autoclass_detected".

Do not implement suggest rememdy.

The variable is referring to the signature during the window, not before it.

Cl **33** *SC* **33.2.5.11** *P* **76** *L* **10** # 63

Lukacs, Miklos — Silicon Labs

Comment Type **E** *Comment Status* **X** *Pres: Lukacs*

A timing diagram showing the classification part of Autoclass would help in understanding the text and would make the intent more clear.

SuggestedRemedy

See timing diagrams presentation (Lukacs)

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.5.11** *P* **76** *L* **17** # 108

Stover, David — Linear Technology

Comment Type **T** *Comment Status* **A** *PSE SD*

Propose we add an additional connection check result to express, for example, that the status of the link segment has changed during do_cxn_chk.

SuggestedRemedy

Add a result to sig_type: "Invalid: Neither open circuit, nor single-signature PD, nor dual-signature PD connection check signature has been found."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD.

Change "open_circ" to "invalid" and definition to "Neither a single-singature PD nor a dual-signature PD connection check signature has been found. This includes an open circuit condition."

Cl **33** *SC* **33.2.5.12** *P* **79** *L* **1** # 223

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **A** *Pres: Yseboodt6*

Entry arc into IDLE:
pse_reset + error_condition * (mr_pse ...) can be ambiguous
I have not found any mention of a defined order of operation. Convention is for AND to take precedence over OR, but this is not a universal truth.

SuggestedRemedy

Use brackets whenever ambiguity is possible.
pse_reset + (error_condition * (mr_pse ...)).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change to: (pse_reset + error_condition) * (mr_pse_enable = enable).

I don't believe your interpretation is correct.

To get to idle, mr_pse_enable has to be true, so it should be ANDed with everything.

Why do we have mr_pse_enable have enumerated choices (why isn't it True/False)?

TFTD

Cl **33** *SC* **33.2.5.12** *P* **79** *L* **35** # 71

Picard, Jean Texas Instruments

Comment Type **TR** *Comment Status* **D** *PSE SD*

The IF(CC_DET_SEQ ≠ 2) statement is missing, seems to have been deleted from previous Draft.

SuggestedRemedy

Re-instate the IF(CC_DET_SEQ ≠ 2) statement. Refer to "Picard_02_0316.pdf" page 1

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

The text shown to be inserted in Picard_02_... Replaced the text that was there rather than be inserted before it.

TFTD, YD, LY

Jean and Chris to discuss and follow up.

Cl **33** *SC* **33.2.5.12** *P* **80** *L* **9** # 175

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *PSE SD*

Figure 33-15, arc from DETECT_EVAL to A1
(mr_pse_alternative [?] both) * (sig_pri = valid) + (det_temp = both_neither) * (sig_sec = valid)

Missing brackets.

SuggestedRemedy

((mr_pse_alternative [?] both) * (sig_pri = valid)) + ((det_temp = both_neither) * (sig_sec = valid))

Response *Response Status* **C**

ACCEPT.

TFTD, see 109.

Cl **33** *SC* **33.2.5.12** *P* **80** *L* **9** # 109

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **D** *PSE SD*

Transition logic in conflict: Out of DETECT_EVAL, PSE can be required to follow arcs "A" and "A1" simultaneously.

SuggestedRemedy

Replace: "(mr_pse_alternative != both) * (sig_pri = valid) + (det_temp = both_neither) * (sig_sec = valid)"
With: "(mr_pse_alternative != both) * (det_temp = only_one) * (sig_pri = valid) + (det_temp = both_neither) * (sig_sec = valid)"

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD, see 175.

Cl **33** *SC* **33.2.5.12** *P* **80** *L* **24** # 176

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Pres: Yseboodt6*

Figure 33-15, arc from CXN_CHK_DETECT_EVAL to A:
Brackets are not consistently used => what was the intent here ?

SuggestedRemedy

TFTD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Transition is correct, no changes.

TFTD as requested.

Also see 109, 175

Cl **33** *SC* **33.2.5.12** *P* **81** *L* **8** # 110

Stover, David Linear Technology

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt11*

Conditional logic in SS state diagram (POWER_UP) may be simplified with no change to function.

SuggestedRemedy

Replace: "IF (mr_pse_alternative = both) * (mr_pse_ss_mode = 1) + ((pd_req_pwr > 4) * (pse_avail_pwr > 4)) THEN"
With: "If (mr_pse_alternative = both) * (mr_pse_ss_mode = 1) + (pd_req_pwr > 4) THEN"

Proposed Response *Response Status* **W**

TFTD.

Is this true? This seems to imply that a PD assigned class 4 or less (due to demotion) must be powered up in 4-pair mode.

I think this breaks stuff…

See 73

Cl **33** *SC* **33.2.5.12** *P* **81** *L* **9** # 73

Picard, Jean Texas Instruments

Comment Type **ER** *Comment Status* **D** *Pres: Yseboodt11*

A parenthesis is missing and another is at the wrong location.

SuggestedRemedy

Replace with this
IF (mr_pse_alternative = both) * ((mr_pse_ss_mode = 1) + ((pd_req_pwr > 4) * (pse_avail_pwr > 4))) THEN

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD, LY

Cl **33** *SC* **33.2.5.12** *P* **81** *L* **18** # 74

Picard, Jean Texas Instruments

Comment Type **ER** *Comment Status* **A** *PSE SD*

A parenthesis is missing

SuggestedRemedy

Insert a parenthesis between IF and "dll_4PID"

Response *Response Status* **C**

ACCEPT.

There is an unequal number of open and close parenthesis currently.

TFTD, LY

Cl **33** *SC* **33.2.5.12** *P* **81** *L* **20** # 111

Stover, David Linear Technology

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt11*

Conditional logic in SS state diagram (POWER_ON) may be simplified with no change to function.

SuggestedRemedy

Replace: "IF dll_4PID + ((pd_req_pwr > 4) * (pse_avail_pwr < 4)) + (mr_pse_ss_mode = 1)) THEN"
With: "IF dll_4PID + (pd_req_pwr > 4) + (mr_pse_ss_mode = 1) THEN"

Proposed Response *Response Status* **W**

TFTD.

See response to 110.

Cl **33** *SC* **33.2.5.12** *P* **81** *L* **39** # 112

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **X** *PSE SD*

Transition logic from POWER_ON into POWER_DENIED is (power_not_available * !tmpdo_timer_done * etc);

Transition logic from POWER_ON into IDLE is (!power_not_available * tmpdo_timer_done * etc).

When power_not_available and tmpdo_timer_done are simultaneously TRUE, PSE state machine cannot transition to either IDLE or POWER_DENIED states.

SuggestedRemedy

Remove "!tmpdo_timer_done" from transition logic between POWER_ON and POWER_DENIED.

Proposed Response *Response Status* **W**

TFTD.

Don't we want the SD to transition to IDLE if tmdpo expires?

I believe the Type 1/2 SD has this same issue…

See 113, 114

DS and LY to follow up.

Cl **33** *SC* **33.2.5.12** *P* **83** *L* **32** # 113

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **X**

Transition logic from POWER_ON_PRI into POWER_DENIED_PRI is (power_not_available_pri * !tmpdo_timer_done_pri * etc). Transition logic from POWER_ON_PRI into IDLE_PRI is (!power_not_available_pri * tmpdo_timer_pri_done * etc). When power_not_available_pri and tmpdo_timer_pri_done are simultaneously TRUE, primary alt state machine cannot transition into either IDLE_PRI or POWER_DENIED_PRI states.

SuggestedRemedy

Remove "!tmpdo_timer_pri_done" from transition logic between POWER_ON_PRI and POWER_DENIED_PRI.

Proposed Response *Response Status* **W**

TFTD

See 112, 114

DS and LY to follow up.

Cl **33** *SC* **33.2.5.12** *P* **85** *L* **30** # 114

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **X**

Transition logic from POWER_ON_SEC into POWER_DENIED_SEC is (power_not_available_sec * !tmpdo_timer_done_sec * etc). Transition logic from POWER_ON_SEC into IDLE_SEC is (!power_not_available_sec * tmpdo_timer_sec_done * etc). When power_not_available_sec and tmpdo_timer_sec_done are simultaneously TRUE, secondary alt state machine cannot transition into either IDLE_SEC or POWER_DENIED_SEC states.

SuggestedRemedy

Remove "!tmpdo_timer_sec_done" from transition logic between POWER_ON_SEC and POWER_DENIED_SEC.

Proposed Response *Response Status* **W**

TFTD

See 112, 113

DS and LY to follow up.

Cl **33** *SC* **33.2.5.9** *P* **85** *L* **35** # 240

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt7*

We adopted a new MPS state diagram last cycle.
It works great for single-signature, but does not address dual-signature, which need independent MPS.

SuggestedRemedy

Adopt yseboodt_07_0516_dsmps.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.5.12** *P* **86** *L* **1** # 115

Stover, David Linear Technology

Comment Type **T** *Comment Status* **X** *PSE SD*

Per 33.2.7.2, the PSE shall return to the IDLE state in the event any measured IClass is equal to or greater than IClass_LIM. This is not reflected in the PSE SD.

SuggestedRemedy

Add transition arcs to the appropriate idle state out of all CLASS_EV states as defined in 33.2.7.2, page 98, Line 25. Transition logic to read, "IClass >= IClass_LIM".

Proposed Response *Response Status* **W**

TFTD

Does every little thing need to be in the state diagram? This was not in the Type 1/2 SD either, but it was a requirement for Type 2 PSEs.

Cl **33** *SC* **33.2.5.12** *P* **87** *L* **17** # 116

Stover, David Linear Technology

Comment Type **T** *Comment Status* **A** *PSE SD*

Transition logic from CLASS_EV2_PRI to MARK_EV_LAST_PRI redundantly performs a check for !class_4PID_mult_events_pri (was already checked out of CLASS_EV1_LCE_PRI).

SuggestedRemedy

Strike the transition arc from CLASS_EV2_PRI to MARK_EV_LAST_PRI.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

On arc from CLASS_EV2_PRI to MARK_EV_LAST_PRI, replace "mr_pd_class_detected_pri != 4" with "class_num_events_pri = 2"

on arc from CLASS_EV2_PRI to MARK_EV2_PR, replace "mr_pd_class_detected_pri = 4" with "class_num_events_pri > 2"

I believe this is needed because we can get to class2 if the class sig is 4, right?

In addition, we can't strike the entire arc, it is checking for other things.

TFTD

Cl **33** *SC* **33.2.5.12** *P* **87** *L* **19** # 117

Stover, David Linear Technology

Comment Type **T** *Comment Status* **A** *PSE SD*

Transition logic from CLASS_EV2_PRI to MARK_EV2_PRI may be simplified.

SuggestedRemedy

Change transition logic from CLASS_EV2_PRI to MARK_EV2_PRI as follows: "tcle2_timer_pri_done * (mr_pd_class_detected = temp_var_pri)"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

OBE by 116.

Cl **33** *SC* **33.2.5.12** *P* **88** *L* **16** # 119

Stover, David Linear Technology

Comment Type **T** *Comment Status* **A** *PSE SD*

Transition logic from CLASS_EV2_SEC to MARK_EV_LAST_SEC redundantly performs a check for !class_4PID_mult_events_sec (was already checked out of CLASS_EV1_LCE_SEC).

SuggestedRemedy

Strike the transition arc from CLASS_EV2_SEC to MARK_EV_LAST_SEC.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement same response as 116 with "sec" replacing "pri"

TFTD

See 116.

Cl **33** *SC* **33.2.5.12** *P* **88** *L* **18** # 120

Stover, David — Linear Technology

Comment Type **T** *Comment Status* **A** *PSE SD*

Transition logic from CLASS_EV2_SEC to MARK_EV2_SEC may be simplified.

SuggestedRemedy

Change transition logic from CLASS_EV2_SEC to MARK_EV2_SEC as follows:
"tcle2_timer_pri_done * (mr_pd_class_detected = temp_var_sec)"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

Implement same response as 117 with "sec" replacing "pri"

Cl **33** *SC* **33.2.5.12** *P* **89** *L* **3** # 181

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **A** *PSE SD*

Figure 33-22, entry arcs into IDLE_MPS_*
"higest_2p" is misspelled.

SuggestedRemedy

Change to "highest_2P"

Response *Response Status* **C**

ACCEPT.

TFTD, DS

Cl **33** *SC* **33.2.5.12** *P* **89** *L* **14** # 78

Picard, Jean — Texas Instruments

Comment Type **ER** *Comment Status* **A** *PSE SD*

missing parentheses

SuggestedRemedy

Middle flowchart: (highest_2p = pri)
Right flowchart: (highest_2p = sec)

Response *Response Status* **C**

ACCEPT.

TFTD, DS

Cl **33** *SC* **33.2.5.12** *P* **89** *L* **21** # 77

Picard, Jean — Texas Instruments

Comment Type **ER** *Comment Status* **A** *PSE SD*

"!" should NOT be there in the left column of Figure 33-22

SuggestedRemedy

Remove the "!" symbol to read "mr_mps_valid_sum"

Response *Response Status* **C**

ACCEPT.

TFTD, DS

Cl **33** *SC* **33.2.5.12** *P* **89** *L* **23** # 76

Picard, Jean — Texas Instruments

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt7*

PSE MPS monitor State Diagram for DS PD is missing

SuggestedRemedy

See yseboodt_07_0516_dsmps.pdf presentation

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.5.12** *P* **89** *L* **33** # 122

Stover, David — Linear Technology

Comment Type **T** *Comment Status* **A** *PSE SD*

When PSE is in the POWER_ON state, both alt_xxx_pwrd and pwr_app_xxx are TRUE and the PSE inrush state diagram cycles through IDLE_INRUSH and MONITOR_INRUSH states, starting and stopping tinrush_xxx_timer indefinitely.

SuggestedRemedy

Replace transition logic from IDLE_INRUSH_PRI to MONITOR_INRUSH_PRI with "alt_pri_pwrd * !pwr_app_pri".
Replace transition logic from IDLE_INRUSH_SEC to MONITOR_INRUSH_SEC with "alt_sec_pwrd * !pwr_app_sec".

Response *Response Status* **C**

ACCEPT.

TFTD

Is this true. If so, the Type 1/2 SD has this same issue, right?

Cl **33** *SC* **33.2.6** *P* **90** *L* **5** # 33

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Detection*

In the following text:
"Also, a PSE may successfully detect a PD but then opt not to power the detected PD."

The following case is not covered:
PSE may successfully detect and classify a PD but then opt not to power the detected PD.

To add text that PSE may detect and not continue and go to IDLE or detect and classify and not go to POWER_UP or detect and classify and POWER_UP and not continue to POWER_ON.
To find the location with the existing text and update it.

SuggestedRemedy

Change to:
"Also, a PSE may successfully detect and classify a PD but then opt not to power the detected PD."

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

I believe that what you are asking for is already included (it detected a PD, but did not power it). Changing legacy text should be avoided it possible. I do not see any value to the new text and if anything it can used to say that you must classify after a detection (which is not true).

TFTD, YD

Cl **33** *SC* **33.2.6** *P* **90** *L* **6** # 123

Stover, David Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Detection*

Allowable detection behavior is inconsistent between CC_DET_SEQ variants. Particularly, CC_DET_SEQ 3 is unique in that an invalid detection signature on alt_pri prevents PSE from investigating alt_sec.

SuggestedRemedy

Add the following text: "A Type 3 or Type 4 PSE detecting an invalid PD signature on either alternative may perform detection on the other alternative."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD, YD

Cl **33** *SC* **33.2.6.1** *P* **90** *L* **39** # 124

Stover, David Linear Technology

Comment Type **T** *Comment Status* **A** *Pres: Darshan11*

tcc_timer has been intentionally removed from PSE SD, but Tcc remains in Table 33-7.

SuggestedRemedy

Remove reference to Tcc on line 27, Table 33-7, and accompanying NOTE on Tcc min.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

OBE by 107

Cl **33** *SC* **33.2.6.1** *P* **90** *L* **40** # 41

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **A** *Pres: Darshan11*

Table 33-7 item 3 and the note below.

From the note it appears that before we will start connection check we need to wait until full mated MDI exists Tcc minimum. And then item 3 requires Tcc_min=200msec min from start to completion which can be interpreted that total Tcc_min is higher than 200msec.
The requirement is not clear.
The note doesn't explain the Tcc_min.

SuggestedRemedy

"NOTE-When a link segment is connected to an MDI, not all contacts are made simultaneously. Therefore, a minimum total time (Tcc_min) is required to complete connection check that includes the time required for full mated MDI and the time required to perform the connection check function."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

OBE by 107.

Cl **33** *SC* **33.2.6.1** *P* **90** *L* **52** # 40

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *Connection Check*

In the text:
"If the voltage on either pairset rises above Vvalid max (defined in Table 33–8) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max (defined in Table 33–17) for at least
TReset (defined in Table 33–15) before performing classification."

We need to define the time in which we consider the voltage is above Vvalid to be imuuned for noise.

SuggestedRemedy

Change to:
"If the voltage on either pairset rises above Vvalid max (defined in Table 33–8) **for more than TBD msec** during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max (defined in Table 33–17) for at least TReset (defined in Table 33–15) before performing classification."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

PDs have no timing requirements that force them to filter out very small times of voltages crossing thresholds. Thus a PD can count a pulse above Vvalid max of 1ns as a class pulse (bad design, but allowed).

TFTD

Cl **33** *SC* **33.2.7** *P* **94** *L* **32** # 84

Schindler, Fred Seen Simply, Broadco

Comment Type **TR** *Comment Status* **A** *PSE Class*

Clause 33 is designed to permit understanding of the requirements of the network device after reading mainly the relevant PSE or PD subsections. To aid the reader in understanding of the PSE classification section add references to the PD section that provides details on classification event response interpretation.

SuggestedRemedy

Modify existing text,
“The assigned Class is the results of the PDs requested Class and the number of class events produced by the PSE as shown in Table 33–11 and Table 33–12.”

with,

“The assigned Class is the results of the PDs requested Class shown in Table 33-24 for single-signature PDs and Table 33-25 for dual-signature PDs, and the number of class events produced by the PSE as shown in Table 33–11 and Table 33–12.”

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

“The assigned Class is the result of the PD's requested Class and the number of class events produced by the PSE as shown in Table 33–11 and Table 33–12. See 33.3.5 for PD classification behavior.”

Change "PDs" to "PD's"

TFTD, FS, YD

Cl **33** *SC* **33.2.7** *P* **95** *L* **43** # 184

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Editorial*

Table 33-11, some ranges are very small, maybe better to make it explicit.

SuggestedRemedy

Change "2 to 3" into "2, 3".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change to "2 or 3"

Consider "2 or 3" as it is the most meaningful in this table. If you agree, pull it out as a TFTD so we can change it, otherwise "2, 3" it is.

TFTD, YD, LY

Cl **33** *SC* **33.2.7** *P* **96** *L* **1** # 125

Stover, David Linear Technology

Comment Type **T** *Comment Status* **A** *PSE Class*

There is no indication in Table 33–12 that the PSE may, for example, issue 3 class events to a dual-signature PD for Type discovery, perform class reset, then issue a number of events consistent with PSE available power.

SuggestedRemedy

Add a note below Table 33–12: "Note: PSEs may issue additional class events to determine additional information about the PD and negotiate power allocation. See 33.2.7.2 for details." Reference this note in column header "Number of PSE class events".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD, YD

Add a note below Table 33–12: "Note: This is the number of class events since the most recent PD reset." Reference this note in column header "Number of PSE class events". Reference this note in column header "Number of PSE class events".

Cl **33** *SC* **33.2.7** *P* **96** *L* **29** # 226

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **A** *PSE Class*

We removed the PD equivalent of Table 33-13 in the PD section, because the text already covered that information. The same is true in the PSE section.
We can get rid of the table.

SuggestedRemedy

Remove Table 33-13.

Change the text on page 97, line 4-12 as follows:
"Subsequent to successful detection, all Type 2 PSEs ***shall*** perform classification using at least one of the following: Multiple-Event Physical Layer classification; Multiple-Event Physical Layer classification and Data Link Layer classification; or Single-Event Physical Layer classification and Data Link Layer classification.
Subsequent to successful detection, all Type 3 and Type 4 PSEs ***shall*** perform classification using at least one of the following: Multiple-Event Physical Layer classification; or Multiple-Event Physical Layer classification and Data Link Layer classification. Both pairsets attached to a dual-signature PD shall be classified by Type 3 and Type 4 PSEs that will deliver 4-pair power."

Response *Response Status* **C**

ACCEPT.

TFTD, YD

Cl **33** *SC* **33.2.7** *P* **97** *L* **16** # 127

Stover, David Linear Technology

Comment Type **T** *Comment Status* **X** *PSE Class*

Unclear if PSE is allowed to investigate classification result on valid pairsets of a port outside behavior defined in PSE SD; behavior described in PSE SD addresses valid cases for powering a PD, does not address PSE simply investigating both pairsets of the link.

SuggestedRemedy

Add the following text: "A Type 3 or Type 4 PSE connected to a dual-signature PD may perform classification on any pairset presenting a valid detection signature prior to returning to the IDLE state."

Proposed Response *Response Status* **W**

TFTD

See 33.

Cl **33** *SC* **33.2.7.1** *P* **97** *L* **32** # 243

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **A** *PSE Class*

"All measurements of I Class shall be taken after the minimum relevant class event timing in Table 33-15."

We now have T_Class for this.

SuggestedRemedy

"All measurements of I Class shall be taken after T_Class, as defined in Table 33-15."

Response *Response Status* **C**

ACCEPT.

TFTD, DS

Cl **33** *SC* **33.2.7.1** *P* **97** *L* **38** # 39

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Class*

The requirement:
"If the measured IClass is within the range of IClass_LIM, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state."
Is not covered by the state machine.
There are probably other requirements that are not covered by the state machine and have shall's.
Do we have rule that that force us to describe shall in SM?
I believe we don't. We can decide according to the cost effectiveness of it in regards to SM simplicity and readability.

SuggestedRemedy

Add the following Editor Note:

"Editor Note: To address in the state machine the case of what should Type 1 do if the measured IClass is within the range of IClass_LIM or use text only (preffered)."

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

We are not changing the Type 1/2 State Diagram unless you submit a maintenance request. I don't believe we should do this anyway. We don't have these requirements shown in the Type 1/2 SD, we shouldn't have to include them for the Type 3/4 SD either.

TFTD, YD, DS

Cl **33** *SC* **33.2.7.1** *P* **97** *L* **40** # 59

Lukacs, Miklos — Silicon Labs

Comment Type **T** *Comment Status* **X** *Pres: Lukacs*

A timing diagram showing the single event classification would help in understanding the text and would make the intent more clear.

SuggestedRemedy

See timing diagrams presentation (Lukacs)

Proposed Response *Response Status* **W**

WPF

TFTD

Cl **33** *SC* **33.2.7.2** *P* **97** *L* **41** # 244

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt8*

The specification of Autoclass in the Multiple-event section can be improved.

SuggestedRemedy

Adopt yseboodt_08_0516_autoclass4.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.7.2** *P* **97** *L* **41** # 128

Stover, David — Linear Technology

Comment Type **TR** *Comment Status* **X** *Pres: Stover1*

There are inconsistencies between Tpdc, autoclass, and mutiple-event classification.

SuggestedRemedy

See stover_01_0516.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.5.12** *P* **98** *L* **4** # 27

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **A** *Pres: Darshan9*

We need to address the following use case (as an example):
When Type 3 PSE with available power of Type 1 or Type 2 connected to single signature PD class 5 or above and we need to report to the host what is the actual PD class and yet to supply the correct number of fingers (1 in case of 15.4W) to indicate the available PSE power.
For this purpose we need to allow class reset after 3 class event and issuing one class event.

SuggestedRemedy

1. To add the following text at page 98 line 4:
"Type 3 and Type 4 PSEs may issue up to 3 class events to determine PD Class.
Type 3 and Type 4 PSEs incapable of supporting PD Class may issue a class reset event to clear the class and mark event counts and may issue the lowest number of class events that is corresponding to the PSE available power."

2. No need to update PSE SM since it is optional feature similar to the text that "PSE can detect and not power" or PSE can use Type 4 class 7 current settings when operating Type 3 class 6 PDs or may other examples in the current spec including IEEE802.3-2012 version.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 106

TFTD.

Better Text:
To add the following text at page 98 line 4:
"Type 3 and Type 4 PSEs may issue up to 3 class events to determine the PD's requested Class. Type 3 and Type 4 PSEs incapable of supporting the assigned Class due to those class events may issue a class reset event to clear the class and mark event count and may issue the lowest number of class events that corresponds to the PSE available power."

Cl **33** *SC* **33.2.7.2** *P* **98** *L* **4** # 129

Stover, David Linear Technology

Comment Type **T** *Comment Status* **A** *Pres: Darshan9*

Requirements and allowances for 4PID, class, and mutual identification are unclear.

SuggestedRemedy

Replace sentence: "Type 3 and Type 4 PSEs may issue a class reset event to perform mutual identification."
With: "Type 3 and Type 4 PSEs may issue up to 3 class events to determine PD Class. Type 3 and Type 4 PSEs incapable of supporting negotiated PD Class may issue a class reset event to clear the class and mark event counts."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 106

I believe we also need to define "class reset" somewhere. We use the term a lot, but is it defined anywhere?

TFTD

Cl **33** *SC* **33.2.7.2** *P* **99** *L* **1** # 130

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **D** *PSE Class*

"If any measured IClass is equal to or greater than IClass_LIM min, a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state." Most importantly, this list is missing a serial comma. Failing that, SISM state machines experiencing class overcurrent should likely return to their resident IDLE_PRI/IDLE_SEC state, and not the global IDLE state.

SuggestedRemedy

"If any measured IClass is equal to or greater than IClass_LIM min, a Type 2 PSE shall return to the IDLE state. If any measured IClass is equal to or greater than IClass_LIM min, a Type 3 or Type 4 PSE shall return to the appropriate idle state."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD, FS

Dave Stover to draw some arcs.

Cl **33** *SC* **33.2.7.2** *P* **99** *L* **1** # 32

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **A** *PSE Class*

The following requirement is not described by the state machine.
"If any measured IClass is equal to or greater than IClass_LIM min, a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state. The PSE shall limit class event currents to IClass_LIM and shall limit mark event currents to IMark_LIM."

SuggestedRemedy

Add the following Editor Notes:
"Editor Note: To address existing "shall" requirements that are not covered in the state machine."

"Editor Note: To address in the state machine the case of what should Type 2, 3 and 4 do if the measured IClass is within the range of IClass_LIM or use text only (preffered)."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Obe by ….

Partial OBE by 130.

I don't think we need to add editor's notes. Type 1/2 SD is not changing. Type 3/4 can be covered in text just like Type 1/2.

TFTD

Cl **33** *SC* **33.2.7.2** *P* **99** *L* **9** # 34

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Class*

"The PSE shall complete Multiple-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI or pairset to go below VMark min, unless in the CLASS_RESET_PRI or CLASS_RESET_SEC states."

Missing POWER_UP state as well.

SuggestedRemedy

Change to:
"The PSE shall complete Multiple-Event Physical Layer classification and transition to the POWER_UP and POWER_ON state without allowing the voltage at the PI or pairset to go below VMark min, unless in the CLASS_RESET_PRI or CLASS_RESET_SEC states."

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

If we transition to POWER_ON, that means we went through POWER_UP. So the requirement is already there.

TFTD, DS

Cl **33** *SC* **33.2.7.2** *P* **99** *L* **11** # 245

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **A** *PSE Class*

"If the PSE returns to the IDLE state, it shall maintain the PI voltage at VClass for a period of at least TReset min before starting a new detection cycle."

- VClass should be VReset
- Also, that same requirement holds for PSEs that are in the CLASS_RESET states.

SuggestedRemedy

"If the PSE returns to the IDLE state, it shall maintain the PI voltage at VReset for a period of at least TReset min before starting a new detection cycle. If the PSE is in any of the CLASS_RESET states, it shall maintain the PI or pairset voltage at VReset for a period of at least TReset min."

- Remove the sentence on page 99, line 26 which says:
"When the PSE is in the state CLASS_RESET_PRI or CLASS_RESET_SEC the PSE shall provide to the PI V Reset , subject to the T Reset timing specification."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

List CLASS_RESET states explicitely as there are other states with RESET in the name and it may be confusing.

TFTD, YD

Cl **33** *SC* **33.2.7.2** *P* **99** *L* **20** # 217

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PSE Class*

original text: "Classification events may appear on one or both pairsets."

True for single-signature, not for dual.
Also problematic for Type 1 and Type 2 PSEs.

The original intent of that sentence was to allow:
- "4-pair" class events for single-sig PDs
- alternating class events between pairsets
- other creative classification games

The sentences that deal with applying Vclass already say "to the PI or pairset", granting leave to do all of this.

SuggestedRemedy

We no longer need the quoted sentence. Remove it.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD, YD

Yair to work on text for do_classification function description.

Cl **33** *SC* **33.2.7.2** *P* **99** *L* **28** # 60

Lukacs, Miklos Silicon Labs

Comment Type **T** *Comment Status* **X** *Pres: Lukacs*

A timing diagram showing the multiple event classification would help in understanding the text and would make the intent more clear.

SuggestedRemedy

See timing diagrams presentation (Lukacs)

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.8** *P* **101** *L* **51** # 131

Stover, David — Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Power*

Guidance on how to handle dual-signature PDs with mismatched Class/Type combinations is unclear for some defined PSE implementations.

SuggestedRemedy

Insert the sentence "PSEs powering dual-signature PDs may enforce on both pairsets the values in Table 33-17 corresponding to the pairset of that PD identified as the highest PD Class."

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Insert the sentence "PSEs powering dual-signature PDs may enforce the values in Table 33-17 corresponding to the pairset with the highest assinged class on both pairsets."

TFTD, LY

Cl **33** *SC* **33.2.8** *P* **103** *L* **30** # 35

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **A** *PSE Power*

Table 33-17 item 12 class 4 row, min value 0.684.
The foot note 2 that was attached to the 0.684A for Type 3 and 4 was lost after updating this item.

SuggestedRemedy

Change "0.684A" to "0.684^2".
Add the following text after Table 33-17:
"^2 Unbalance at class 4 is not restricted. The ILIM-2P value is higher than the value for class 5 for Type 3 and 4 PSEs operating with 4-pairs."

Response *Response Status* **C**

ACCEPT.

TFTD

Cl **33** *SC* **33.2.8** *P* **105** *L* **36** # 36

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan4*

Editor Note #2. This item is important for the integrity and protection reliability of the PSE under unbalance condition.
Due to lake of time, this subject was not resolved yet.
To be discussed with the group how to continue with this item and yet meet our time table.

SuggestedRemedy

See darshan_04_0516.pdf for discussion details and possible remedy

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.8.4** *P* **106** *L* **25** # 247

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt2*

There are several inconsistencies/errors identified in the PSE power section.

SuggestedRemedy

Adopt yseboodt_02_0516_power.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.8.4** *P* **106** *L* **27** # 50

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment may be OBE by presentation.

One area where 33.2.8.4 is written for 4-Pair (Type 3/4) PSE's only:

The terms Iport-2P and Iport-2P-other are defined using terms from the Type 3/4 state diagram. These terms have no meaning for 2-Pair powering cases. Iport-2P is then later used as vertical axis to current templates including those applicable to Type 1/2 PSEs.

Iport is defined earlier with the Type 1 and Type 2 state machine in 33.2.5.4. that in turn references 33.2.8.6.

SuggestedRemedy

One remedy is to add a specificity to Iport-2P definition:

Iport-2P
= Iport for Type 1 and Type 2 PSE's
= Iport-2P-pri for the Primary Alternative of Type 3 and Type 4 PSEs
= Iport-2P-sec for the Secondary Alternative of Type 3 and Type 4 PSEs

Iport-2P-other
= Iport-2P-sec for the Primary Alternative of Type 3 and Type 4 PSEs
= Iport-2P-pri for the Secondary Alternative of Type 3 and Type 4 PSEs

Proposed Response *Response Status* **W**

WFP?

TFTD

Cl **33** *SC* **33.2.8.4** *P* **106** *L* **46** # 51

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment may be OBE by presentation.

This comment may be OBE by presentation.

Equation 33-7 defines Icon-2P = Pclass / Vpse when in 2-pair mode. Table 33-17 (item 5) defines Icon = Pclass / Vport-PSE-2P. If we assume Vpse (defined in 1.4) is the really the same thing as Vport-PSE-2P (defined in Table 3-17), then Icon-2P is really the same as Icon.

Also, Pclass and Pclass-2P are really defined in EQ 33-2 and EQ 33-3 respectively, not Tables 33-11 and 33-12.

SuggestedRemedy

Change Equation 33-7 to:

Icon-2P
= Icon when in 2-pair mode
= min(.....) when 4-pair powering a single signature PD
= Pclass-2P / Vpse when 4-pair powering a dual signature PD

where
Pclass is defined in Equation 33-2
Pclass-2P is defined in Equation 33-3

Proposed Response *Response Status* **W**

WFP?

TFTD

Cl **33** *SC* **33.2.8.4** *P* **107** *L* **7** # 52

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment may be OBE by presentation.

Another area where 33.2.8.4 is written for 4-Pair (Type 3/4) PSE's only:

"A PSE is not required to support Icon-2P values greater than Icon-2P-unb. Icon is the total current of both pairs with the same polarity that a PSE supports. Icon-2P_unb is the maximum current the PSE supports over one of the pairs of the same polarity..."

SuggestedRemedy

Replace this text.

(New Paragraph)
"When a Type 3 or Type 4 PSE is powering 4 pairs, that PSE is not required to support Icon-2P values greater than Icon-2P-unb. Icon is the total current of both pairs with the same polarity that a PSE supports. Icon-2P_unb is the maximum current the PSE supports over one of the pairs of the same polarity..."

Proposed Response *Response Status* **W**

WFP?

TFTD

Cl **33** *SC* **33.2.8.4** *P* **107** *L* **12** # 53

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment may be OBE by presentation.

Another area where 33.2.8.4 is written for 4-Pair (Type 3/4) PSE's only:

"In addition to ICon, ICon-2P and ICon-2P-unb as specified in Table 33–17 and Equation (33–7), the PSE shall support the following AC current waveform parameters, while within the operating voltage range of VPort_PSE-2P:

IPeak, IPeak-2P-unb, and IPeak-2P minimum for TCUT-2P minimum and 5 % duty cycle minimum, where"

SuggestedRemedy

This section needs some work. It probably should be re-written to individually address the three fundamental cases:

1) 2-Pair Powering:
Only need to define Ipeak-2P using (Rchan) in quadratic

2) 4-Pair Powering Single Signature PD(where Ipeak-2P-unb applies):
Define Ipeak, Ipeak-2P, Ipeak-2P_unb using (Rchan/2) in the quadratic

3) 4-Pair Powering Dual Signature PD
Define Ipeak-2P using (Rchan) and (PPeak_PD-2P) in the quadratic

Proposed Response *Response Status* **W**

WFP?

TFTD

Cl **33** *SC* **33.2.8.4** *P* **107** *L* **33** # 54

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment may be OBE by presentation.

There are 2 different equations for Ipeak-2P_unb: EQ 33-9 and EQ 33-11.

EQ 33-9 describes IPeak-2P_unb as a function of Ipeak that is in turn a function of PSE port voltage and PD load.

EQ 33-11 describes IPeak-2P_unb as a function of ILIM-2P, but ILIM-2P is not a function of PSE port voltage or PD load - it is a fixed value greater than ILIM-2P_min. Also, my sample calculation of Ipeak-2P_unb for Class 6 (828mA) produces a figure well higher than ILIM-2P_min (702 mA) for Class 6.

Is EQ 33-11 indicating that ILIM-2P_min must be higher than what is in Table 33-17 ??????

SuggestedRemedy

Not sure what to do here.

One option is to just eliminate EQ 33-11. However, if it is adding information relevant to PSE behavior, we need to better capture that.

Proposed Response *Response Status* **W**

WFP?

TFTD

Cl **33** *SC* **33.2.8.4.1** *P* **109** *L* **1** # 44

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Unbalance*

Rpse_max is defined as "the maximum PSE common mode effective resistance..." and Rpse_min is defined as "the minimum PSE common mode effective resistance".

This is slightly confusing and may infer that there are some maximum and minimum absolute values in some table somewhere.

SuggestedRemedy

Change to:

Rpse_min is the lowest possible effective resistance in the powered pairs of the same polarity.

For a given Rpse_min,

Rpse_max is the highest possible effecive resistance in the powered pairs of the same polarity.

Proposed Response *Response Status* **W**

TFTD.

Yair and Pete to discuss.

I don't think you can format it like that as the two parameters are inside a "where" that descirbes equation 33-13.

I also don't understand what we are really trying to say here.

Are we really trying to say that RPSE_min is the lower of the common mode effective resistance of the powered pairs of the same polarity? And RPSE_max is the maximum allowed common mode effective resistance in the powered pairs of the same polarity for a given RPSE_min?

Cl **33** *SC* **33.2.8.5** *P* **109** *L* **16** # 81

Picard, Jean — Texas Instruments

Comment Type **TR** *Comment Status* **D** *PSE Inrush*

The following statement is incorrect in case where the PD is class 0-4, in which case a type 3 PSE is allowed to do inrush with only one 2P channel.

"Type 3 and Type 4 PSEs that apply power to both pairsets when connected to a single-signature PD shall reach the POWER_ON state on both pairsets within TInrush-2P max, starting with the first pairset
transitioning into the POWER_UP state. The second pairset may transition to POWER_UP anytime within this time period."

SuggestedRemedy

Replace with this:

"Type 3 and Type 4 PSEs that have assigned Class 5 to 8 to a single-signature PD shall reach the POWER_ON state on both pairsets within TInrush-2P max, starting with the first pairset transitioning into the POWER_UP state, whereas the second pairset transitions to POWER_UP anytime within this time period."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Jean to check SD for same behavior.

TFTD

"Type 3 and Type 4 PSEs that have assigned Class 5 to 8 to a single-signature PD shall reach the POWER_ON state on both pairsets within Tinrush-2P max, starting with the first pairset transitioning into the POWER_UP state, and where the second pairset transitions to POWER_UP anytime within this time period."

Cl **33** *SC* **33.2.8.5** *P* **109** *L* **20** # 28

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *PSE Inrush*

In the following text, it is not clear when the PSE is following the template:
"The PSE shall limit IInrush-2P and IInrush during POWER_UP per the requirements of Table 33-17. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset inrush template in Figure 33-26 and Equation (33-13)."
in Figure 33-26 and Equation (33-13) some PD implementations start to show Iinrush only after significant time (10-30msec) after the application of Vpd but still within Tinrus_min time duration but the template in figure 33-26 looks that it is relevant to iinrush appearance at t=0 only.

SuggestedRemedy

Change from:
"The PSE shall limit IInrush-2P and IInrush during POWER_UP per the requirements of Table 33-17. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset inrush template in Figure 33-26 and Equation (33-13)."

to:
"The PSE shall limit IInrush-2P and IInrush during POWER_UP **state** per the requirements of Table 33-17. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset inrush template in Figure 33-26 and Equation (33-13) **for the duration of POWER_UP state**."

Proposed Response *Response Status* **W**

TFTD

Yair, Lennart, and Pete to work on text.

I am not sure how the suggested text makes your concern any clearer in the text.

Change to:
"The PSE shall limit Iinrush-2P and Iinrush during POWER_UP per the requirements of Table 33-17. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset inrush template in Figure 33-26 and Equation (33-13) for the duration of POWER_UP."

Cl **33** *SC* **33.2.8.5** *P* **110** *L* **9** # 195

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Editorial*

Equation 33-14 uses variable y1.
Since there is neither a y0 or a y2, we can also rename it to 'i'.

SuggestedRemedy

Rename 'y1' to 'i' in Equation and variable list.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Rename it "Imax". "i" seems like an index to something.

"Imax" stands for Imax since this is what the variable represents.

TFTD, LY

Cl **33** *SC* **33.2.8.6** *P* **110** *L* **48** # 45

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

Iport-2P is defined in two places, 33.2.8.4 and then again in 33.2.8.6. It should have only one definition, and given the present structure of the standard, that definition needs to be universal to all PSE types and powering modes. Both 33.2.8.4 and 33.2.8.6 infer a relationship between Iport-2P and Type 3/4 PSEs.

Suggestion is to broaden the Iport-2P definition in 33.2.8.4 - that is covered in a separate comment. Then move the Iport definition to 33.2.8.4 along side of the Iport-2P definition.

SuggestedRemedy

Modify 33.2.8.4:
Add first sentence:
"IPort is the total current supplied by the PSE to the PI."

Modify 33.2.8.6:

Revise:
"If IPort, the current supplied by the PSE to the PI, exceeds ICUT-2P for..."
to
"If IPort exceeds ICUT-2P for...."

Revise:
"If IPort-2P, the current supplied on a pairset by the PSE to the PI, exceeds ICUT-2P for longer..."
to
"If IPort-2P exceeds ICUT-2P for longer..."

Modify Iport definition in 33.2.5.4:

Revise:
"IPort Output current (see 33.2.8.6)."
to
"IPort Output current (see 33.2.8.4)."

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.8.7** *P* **111** *L* **9** # 82

Picard, Jean — Texas Instruments

Comment Type **TR** *Comment Status* **D** *PSE Power*

There is an issue with allowing a Type 4 PSE to apply a 1.3A Upperbound template for as long as 4 seconds over 2P when powering a SS PD with Class 6 or lower or DS PD with class 4 or lower. That level of stress for so long can damage components that are not selected for this amount of energy, for example the data transformers of Mag Jacks.

SuggestedRemedy

Require Type 4 PSEs to apply the "Type 3 operating current template" when powering a Type 1-3 PD .

This means the following sentence:
"For Type 4 PSEs, Figure 33–29, Equation (33–17) and Equation (33–20) apply when connected to Type 4 PD, otherwise Figure 33–28, Equation (33–16) and Equation (33–19) apply. "

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

However, as we have dicussed before, the PD determines how much current is drawn. The PSE can't force 1.3A down the channel.

TFTD

Cl **33** *SC* **33.2.8.7** *P* **111** *L* **14** # 25

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan5*

Referring to the text (see darshan_05_0516.pdf for details):
"[**Part-1**] Power shall be removed from a pairset PI of a PSE before the pairset PI current exceeds the "PSE upperbound template" in Figure 33-14, Figure 33-14a, and Figure 33-14b.
[**Part-2**] When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Due to the fact that for single-signature PD:
a)Each pairset is already protected by [**part-1**].
b)Shutting off both pairset doesn't add extra protection to the PD.
c)Forcing the PSE to shut off both pairset in case of fault, kills PD applications that was designed to work at lower power in case of fault when 4-pairs is required for full power.

We don't need [**Part-2**] due to the fact that in single-signature PD if current over a pairset approaches the upper bound template, this pairset will be powered off, if the PD was not designed to handle lower power mode, the whole current will flow through the remaining pairset and it will be disconnected as well, so there is no need for the redundant text in [**Part-2**].

SuggestedRemedy

Option 1:
Delete:
"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template"

Option 2: To address solution proposed by Chritian to be discussed by the group.
The solution may be described in darshan_05_0516.pdf if we get a consensus on the wording of it prior the meeting.

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.8.7** *P* **111** *L* **14** # 6

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt4*

The following sentence,

When connected to a single-signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

has severel weak points:

- the (TBD) to be removed
- the "should" makes nobody happy: those who want the PSE to be able to go past a failure working on single pairset would ignore a reccomendation, and those who want the power to be removed from both pairsets don't have the assurance it will be implemented.
- the timing requirements for power removal can increase PSE complexity.

The main goal here should be avoiding that a PD that failed to work over 4-pairs, when powered on 2-pairs would exceed the current originally intended to flow on one pairset, potentially overstressing the magnetics.

So, the requirement should allow the PSE to disconnect only one pairset only if the current of thesecond pairset is below one-half of the assigned power (i.e. the current that was originally supposed to flow in that pairset). It ensures that the PD is still keeping control of its own current, and no damage occurred.

See also Darshan_05

SuggestedRemedy

Replace:
When connected to a single-signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

With:
When connected to a single-signature PD, a Type 3 or Type 4 PSE may remove power from one pairset and maintain power on the other pairset only if the PD power consumption is below one half of the assigned Pclass (0.5*Pclass).

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.8.7** *P* **111** *L* **14** # 228

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt4*

"When connected to a single-signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

SuggestedRemedy

See/adopt yseboodt_04_0516_pse4p.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.2.8.7** *P* **112** *L* **12** # 46

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **D** *PSE Power*

Figures 33-28 and 33-29 include an ILIM parameter on the right vertical axis. But there is no ILIM definition any more.

Presumably, these should be removed.

SuggestedRemedy

Remove ILIM from Figures 33-28 and 33-29.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Lennart to work with Yair, Jean, and Pete on these figures.

TFTD

Cl **33** *SC* **33.2.8.7** *P* **114** *L* **16** # 49

Johnson, Peter Sifos Technologies

Comment Type **TR** *Comment Status* **A** *PSE Power*

The list of variables beneath Equations 33-18, 33-19, 33-20 includes the term Icon-2P but it is 'Icon-2P min' that is used in the equations.

The definition for Icon-2P is okay.

SuggestedRemedy

Replace Icon-2P with 'Icon-2P min'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Replace Icon-2P min in equations with Icon-2P

TFTD, LY

Cl **33** *SC* **33.2.10.1.2** *P* **118** *L* **26** # 248

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **A** *PSE MPS*

"A PSE, depending on the connected Type of PD, shall use the applicable I Hold min, I Hold max, T MPS and T MPDO values as defined in Table 33-17."

Needs to mention I_Hold-2P.

SuggestedRemedy

"A PSE, depending on the connected Type of PD and whether it is a single-, or dual-signature PD, shall use the applicable I Hold, I Hold-2P , T MPS and T MPDO values as defined in Table 33-17."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD, DS

"A PSE, depending on the connected Type of PD and whether it is connected to a single-signature or dual-signature PD, shall use the applicable I Hold, I Hold-2P, T MPS, and T MPDO values as defined in Table 33-17."

Cl **33** *SC* **33.2.10.1.2** *P* **118** *L* **30** # 55

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **A** *PSE MPS*

It seems that this section is not accounting for a Type 3 PSE that powers 2-pair (Class 1-3). The rules for Type 3 and Type 4 PSEs are written for 4-Pair powering of single signature and dual signature PDs.

SuggestedRemedy

Revise:
"A Type 1 and Type 2 PSE:" to
"A PSE powering with 2 pairs:"

Revise:
"A Type 3 or Type 4 PSE, when connected to a single-signature PD:" to
"A PSE powering a single signature PD with 4 pairs:"

Revise:
"A Type 3 or Type 4 PSE, when connected to a dual-signature PD:" to
"A PSE powering a dual signature PD with 4 pairs:"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD, DS

DS PD rules should not change based on number of powered pairsets (DS PDs have their own unique rules per pairset). Also, I suggest keeping the Types listed to make it easier to a reader to understand

Revise:
"A Type 1 and Type 2 PSE:" to
"A PSE powering a PD over a single pairset:"

Revise:
"A Type 3 or Type 4 PSE, when connected to a single-signature PD:" to
"A Type 3 or Type 4 PSE powering a single-signature PD over both pairsets:"

Revise:
"A Type 3 or Type 4 PSE, when connected to a dual-signature PD:" to
"A Type 3 or Type 4 PSE powering a dual-signature PD:"

Cl **33** *SC* **33.2.10.1.2** *P* **118** *L* **40** # 230

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PSE MPS*

"A Type 1 and Type 2 PSE: - shall not remove power from the PI when I Port is greater than or equal to I Hold-2P max continuously for at least T MPS every T MPS + T MPDO , as defined in Table 33-17."

"A Type 3 or Type 4 PSE, when connected to a single-signature PD: -shall not remove power from the PI when DC MPS has been present within the T MPS + T MPDO window. This allows a PD to minimize its power consumption."

"A Type 3 or Type 4 PSE, when connected to a dual-signature PD: -- shall not remove power from a pairset when DC MPS has been present on both pairsets every T MPS + T MPDO ."

These shalls are essentially meaningless. PSEs may remove power for any reason. The PSE shall remove power in the case of overcurrent, or Vport-2P being out of spec.

This is to protect against bad MPS implementations that remove power when they shouln`t.

SuggestedRemedy

Add a condition 'unless there is a non-MPS related reason to do so':

"A Type 1 and Type 2 PSE: - shall not remove power from the PI, unless there is a non-MPS related reason to do so, when I Port is greater than or equal to I Hold-2P max continuously for at least T MPS every T MPS + T MPDO , as defined in Table 33-17."
(Note: merge the above with the other comment that touches this if adopted).

"A Type 3 or Type 4 PSE, when connected to a single-signature PD: -shall not remove power from the PI, unless there is a non-MPS related reason to do so, when DC MPS has been present within the T MPS + T MPDO window. This allows a PD to minimize its power consumption."

"A Type 3 or Type 4 PSE, when connected to a dual-signature PD: -- shall not remove power from a pairset, unless there is a non-MPS related reason to do so, when DC MPS has been present on both pairsets every T MPS + T MPDO ."

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

I understand the idea, but the wording is terrible. Also, .3at did not include this language, do we need to?

How about, "…shall not remove power due to MPS absence when…"

TFTD

Cl **33** *SC* **33.2.10.1.2** *P* **118** *L* **40** # 229

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PSE MPS*

"A Type 1 and Type 2 PSE: - shall not remove power from the PI when I Port is greater than or equal to I Hold-2P max continuously for at least T MPS every T MPS + T MPDO , as defined in Table 33-17."

This final shall is inconsistenly worded compared to the "do not remove power" shalls for Type 3 and Type 4.
See: hstewart_01_0116_DC_MPS_Template_v8.pdf for what the intent was.

SuggestedRemedy

Replace by:
"- shall not remove power from the PI when DC MPS has been present within the T_MPS + TMPDO window."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Yair to review.

TFTD, YD

Cl **33** *SC* **33.2.10.1.2** *P* **118** *L* **52** # 249

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE MPS*

For Type 3 and 4 PSEs, connected to a single-signature PD, there are 2 'shalls' and a 'may' that determine if DC MPS component is either PRESENT, ABSENT or PRESENT OR ABSENT. These requirements should not overlap, ie, only one of those 3 conditions can be true at the same time.

The 'may' statement overlaps with the two shalls for certain combinations of current.
For example, if the Iport-2P currents are 1mA and 6mA respectively, the first 'shall' says MPS is PRESENT.
The may statement however is also True, indicating that MPS may be PRESENT OR ABSENT.

To avoid overlap, the two shall statements need to be made more narrow.

SuggestedRemedy

The 'or' in the first two shall statements for "A Type 3 or Type 4 PSE, when connected to a single-signature PD" needs to become and 'and':
- change "or" to "and" on page 118, line 46
- change "or" to "and" on page 118, line 49

Proposed Response *Response Status* **W**

TFTD

Jean and Lennart to discuss.

I don't like this remedy as it implies that the PSE must check both the sum and individual pairset currents.

Cl **33** *SC* **33.2.10.1.2** *P* **119** *L* **19** # 231

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **A** *PSE MPS*

"A Type 3 or Type 4 PSE, when connected to a dual-signature PD: -may maintain power on a pairset if DC MPS has been present on that pairset every T MPS + T MPDO."

Is inconsistent in describing the timing requirements.

SuggestedRemedy

"-may maintain power on a pairset _when_ DC MPS has been present on that pairset _within_ the T MPS + T MPDO _window_."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make similar change to line 17.

TFTD, YD

Cl **33** *SC* **33.2.10.1.2** *P* **119** *L* **22** # 26

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan10*

False disconnect or false maintain power as a result of Short MPS under PSE transient need to be adrressed.
We need to allow PSE system to decide what to do in this case when a PSE dv of up to 2V for a dt of 0.8ms to 20ms which result with distored of the short MPS pulse for at least one cycle of MPS+TMPDO for a specific time window.

SuggestedRemedy

Add the following text to the end of section 33.2.10.1.2:
Option 1:
Type 3 and Type 4 PSE when supporting short MPS may fail to detect presence or absence of a short MPS pulse as a result of PSE dv/dt that may cancel or distorted or add MPS pulse. Type 3 and Type 4 PSE when supporting short MPS during PSE dv/dt for PSE voltage change dv of up to 2V and time duration dt of 0.8msec to 10msec for a sliding time window of 3 sec (TBD) may maintain the power or disconnect the power when presence or absence of short MPS pulse is not possible under the above conditions.

Option 2:
A PSE may ignore the current MPS status of a short MPS pulse once every 3 seconds, which permits PSEs to deal with seldom occurring transients that may distort the MPS signal.

Proposed Response *Response Status* **W**

TFTD

I do not like either option. Option 1 says "up to 2V" which means that a PSE can always ignore the MPS status and say that there was a 1nV transient. Option 2 seems way to often. To let the PSE ignore a missed MPS pulse every 3 seconds seems to make it just a matter of time before something is unplugged and something new is plugged in and the PSE toasts some poor NIC.

Cl **33** *SC* **33.3.3** *P* **121** *L* **13** # 232

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt12*

Updates to the PD State Diagram

SuggestedRemedy

Adopt yseboodt_12_0516_pdstatedia.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.3.5** *P* **124** *L* **1** # 147

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **X** *Pres: Yseboodt05*

The PD legacy state machine has the issue that it is incapable of leaving the IDLE state.

SuggestedRemedy

See yseboodt_05_0516_pdsmlegacy.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.3.5** *P* **124** *L* **3** # 86

Schindler, Fred Seen Simply, Broadco

Comment Type **TR** *Comment Status* **A** *Editorial*

The remedy to D1.6, comment 248 may not be completely implemented. I believe the request should apply to legacy state diagrams.

SuggestedRemedy

Implement the accepted solution,
“Replace all square brackets with parenthesis in state diagrams.”

Response *Response Status* **C**

ACCEPT.

TFTD

We have decided to leave the existing Type 1/2 state machine alone (except for maintenance requests). Does this include formatting?

Cl **33** *SC* **33.2.3.8** *P* **127** *L* **38** # 87

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **A** *PD SD*

Existing sentence, "tpowerdly_timer
A timer used to prevent Type 2 and Type 3 PDs from drawing more than Type 1 power and Type 4
PDs from drawing more than Class 2 power during the PSE's inrush period; see Tdelay-2P in Table
33–28." Incorrectly covers Type 2 PDs in the Type 3 and 4 section. Type 2 PDs are covered by legacy text on p123.

SuggestedRemedy

Replace the sentence with,"tpowerdly_timer
A timer used to prevent Type 3 PDs from drawing more than Type 1 power and Type 4
PDs from drawing more than Class 2 power during the PSE's inrush period; see Tdelay-2P in Table
33–28."

Response *Response Status* **C**

ACCEPT.

TFTD, DS

Cl **33** *SC* **33.3.3.10** *P* **129** *L* **8** # 42

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan7*

It is not clear that the state machine permits Tdelay also for Type 1.
Technically there is no need for it since Type 1 current always < PSE Inrush_min however to simplify future PD chip designs we need to allow same behavior for all PD types regarding delaying the load current consumption by Tdelay.

SuggestedRemedy

See darshan_07_0516.pdf for proposed remedy.

Proposed Response *Response Status* **W**

WFP

TFTD

However, I see no need for this because the Tpowerdly timer is meant to make all PDs act like Type 1, which Type 1 PDs already do…

Cl **33** *SC* **33.3.3.10** *P* **129** *L* **41** # 18

Darshan, Yair — Microsemi

Comment Type **ER** *Comment Status* **A** *PD SD*

Title of figure 33-33 need to be 33-2

SuggestedRemedy

Change fig number to 33-2

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD, YD

Change figure number to "33-32" as its "continued"

Replace "The PD shall provide the behavior of the state diagram shown in Figure 33-32."

With: "Type 1 and Type 2 PDs shall provide the behavior of the state diagram shown in Figure 33-31. Single-signature Type 3 and Type 4 PDs shall provide the behavior of the state diagram shown in Figure 33-32. Dual-signature Type 3 and Type 4 PDs shall provide the behavior of the state diagram shown in Figure 33-33.

Change all figure numbering after 33-32 to match.

Cl **33** *SC* **33.3.3.11** *P* **130** *L* **3** # 38

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan6*

To add dual sig PD state machine.

SuggestedRemedy

See proposal for dual-signature state machine in darshan_06_0516.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.4** *P* **131** *L* **1** # 250

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt3*

A PD is either a single-, or a dual-signature device. The determination of single/dual impacts nearly every requirement.

Yet the PD section offers zero guidance or requirements on what a PD needs to meet to be guaranteed to be correctly identified by connection check.

SuggestedRemedy

Adopt yseboodt_03_0516_pdsig.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.4** *P* **132** *L* **3** # 89

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **D** *Editorial*

Tables 33-21 and 33-22 do not use the same style as other tables.

SuggestedRemedy

Recommend Table 33-26 be used as a guide to add missing columns, Item, and Symbol. Column Unit should also be relocated to match style. Provide editor with license to fill in other columns. Thank the Editor for exception this. This is related to comment marked COMMENT-1.

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Why is this a technical comment?

If none of the parameters from these tables are referenced by name in the draft, why do they need Item numbers and symbols?

TFTD

Cl **33** *SC* **33.3.7.2.1** *P* **140** *L* **36** # 11

Bennett, Ken — Sifos Technologies, In

Comment Type **TR** *Comment Status* **A** *Pres: Darshan14*

Until recently, Pport_PD only existed in 33.3.7.2.1. Pport_PD and Pport_PD_2P are now symbols for the input average power in Table 33-28 and in 33.3.7.2.

The definitions of the Pport_PD and Pport_PD_2P variables in Section 33.3.7.2.1 are in conflict with the average power variables in the PClass_PD specification. They use a static (fixed) Vport_PD_2P value which is incorrect; The PD input Voltage changes dynamically with power variations in the PD (due to channel resistance).

Section 33.3.7.2.1 also doesn't seem to make sense. It is a subsection of 33.3.7.2-Input Average Power, and is entitled:

"System Stability Test Conditions During Start-up and Steady State."

The content states Pport_PD and Pport_PD_2P "shall be defined by" ..., and that's it. There IS no test condition mentioned. Pport_PD isn't even used anywhere else in the existing (.at) standard.

Section 33.3.7.2.1 should be deleted. Alternatively, different symbols should be used for average power in table 33-28.

SuggestedRemedy

Delete section 33.3.7.2.1.
OR
Change Pport_PD and Pport_PD_2P in table 33-28 to Pavg_PD and Pavg_PD_2P.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

adopt darshan_14_0516.pdf

Does this affect anything I am not seeing?

Cl **33** *SC* **33.3.7.3** *P* **141** *L* **7** # 215

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Pres: Yseboodt10*

The PD inrush section is particularly troublesome. How many times have we tweaked this text. It doesn`t seem to improve.

SuggestedRemedy

Completely new text, adopt yseboodt_10_0516_pdinrush.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.7.3** *P* **141** *L* **7** # 133

Stover, David Linear Technology

Comment Type **TR** *Comment Status* **X** *Pres: Stover2*

PD input inrush current requirements are inconsistent with other sections of the text.

SuggestedRemedy

See stover_02_0516.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.7.3** *P* **141** *L* **16** # 30

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan2*

Addressing comments # 179 and others related to this clause as elaborated below from D1.6:
The following proposed modifications are addressing the following questions:
1.Does PDs that are internally limiting their inrush current are required to end Inrush period within TInrush-2P min per Table 33-17?
2.How we prevent that PD internal load during Iinrush period is less than Inrush current setting value to ensure successful POWER_UP?
3.Adding a note that explains why the PD PI current is not equal to the DC load current during POWER UP.
4.Adding text that addresses the new 110uF value for dual-signature class 1-4.

SuggestedRemedy

See darshan_02_0516.pdf for proposed remedy.

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.7.3** *P* **141** *L* **35** # 92

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **D** *Editorial*

Text previously corrected was changed back to the same undesirable form. It is incorrect to state that a thing has human properties, liking seeing.

SuggestedRemedy

Existing text:
CPort in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. CPort-2P in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD.

Corrected:
A PSE is connected to CPort in Table 33–28 during POWER_UP and POWER_ON states, when connected to a single-signature PD. A PSE is connected to CPort-2P in Table 33–28, on each pairset, during POWER_UP and POWER_ON states, when connected to a dual-signature PD.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

While factually correct, the new text doesn't actually provide any clarity on what Cport and Cport-2P are…

TFTD, new text is welcome.

Fred to follow up.

Cl **33** *SC* **33.3.7.4** *P* **141** *L* **49** # 56

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Johnson1*

This commment is a recommendation to separate concepts of extended power to class 6 and class 8 PDs and associated requirements to meet *PSE* output power rather than *PD* input power requirements from other more general and more widely applicable PD requirements. We also need to better qualify the cases where Class 6 and Class 8 PDs are not subject to Pclass_PD and Ppeak_PD limits.

Rationale is that extended power will be applicable only in specialized systems that are engineered to allow certain PD's to operate above Pclass_PD and interoperate with standard compliant PSE's.

SuggestedRemedy

Create new sub-sections 33.7.2.1 and 33.3.7.4.1.

Re-locate Class 6 / Class 8 extended power text, formulas, and current templates into those respective sections.

I will separately provide a document (baseline text) showing what this would look like in johnson_01_0516_Extended_Pwr_baseline_v1.docx.

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.7.3** *P* **142** *L* **2** # 93

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **D** *PSE Inrush*

It is incorrect to state that a thing has human properties, liking seeing.

SuggestedRemedy

Figure 33-27 text uses “PSE sees”. Replace with, “PSE load capacitance is”.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Again, while factually correct the new text doesn't distinguish between what is seen on a pairset vs seen at the PI, which is the entire point of the figure.

Better text is welcome.

TFTD.

Fred to follow up

Cl **33** *SC* **33.3.7.4** *P* **142** *L* **35** # 57

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *Pres: Johnson1*

This comment may be OBE by another comment I'm submitting for 33.3.7.4.

Certain phrases are written as if all Class 6 and Class 8 PDs will benefit from extended power. This is contradictory with 33.3.7.2 and needs to be corrected.

Examples:
Line 35
"The maximum IPort value for all PDs except those in Class 6 or Class 8..."

Line 47
"The maximum IPort value for all PDs in Class 6 or Class 8, over the operating VPort_..."

SuggestedRemedy

Revise these phrases.
Line 35
"The maximum IPort value for PDs that operate across all possible channels, over the operating VPort_PD-2P range..."

Line 47
"The maximum IPort value for Class 6 or Class 8 PDs that are aware of actual channel DC resistance, over the operating VPort_PD-2P range..."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

I don't see a remedy, just a comment telling me which text is wrong.

TFTD (remedy is present).

Cl **33** *SC* **33.3.7.6** *P* **145** *L* **11** # 235

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt9*

The PD transients section contains many duplicate requirement text blocks which can be merged and the differences captured in a Table.
We love Tables.

SuggestedRemedy

Adopt yseboodt_09_0516_pdtransient.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

If only Tables felt the same way about you…

Cl **33** *SC* **33.3.7.6** *P* **145** *L* **25** # 31

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Darshan3*

We need to address the fact that we change dual-signature class 1-4 PD capacitance value from 180uF to 110uF

SuggestedRemedy

See proposed remedy in darshan_03_0516.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.3.7.6** *P* **145** *L* **30** # 24

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *Pres: Yseboodt9*

Per comment #193 in D1.6 according to approved remedy DARSHAN_06_0316.PDF the "a)" should be deleted in the following text:

"a) A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33-38) after TLIM min (see Table 33-17 for a Type 1 PSE) when the following...."

SuggestedRemedy

Change to:
1. "A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–38) after TLIM min (see Table 33–17 for a Type 1 PSE) when the following...."
2. Align the paragraph to the next paragraph starting with "A Type 2 or single-signature Type 3 PD...."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Editor to follow IEEE style guide (are a's allowed if no b is present?).

TFTD, LY

Cl **33** *SC* **33.3.7.10** *P* **147** *L* **26** # 13

Bennett, Ken Sifos Technologies, In

Comment Type **TR** *Comment Status* **X** *Pres: Bennet1*

The first two paragraphs are ambiguous. It's not clear whether the ICon_2P_unb, ICon_2P requirements must be met for a single set of RSource and Vport_PSE values that fall within the ranges mentioned, or if ICon_2P_unb, ICon_2P must be met over the full Rsource and Vport_PSE_2P ranges.

The requirements for ICon apply to the full Rsource and Vport ranges, which correspond to compliant ranges of PSE and Channel characteristics. (PDs can fail Icon_unb at short or long channels, and at any length for extended power.)

SuggestedRemedy

See bennett_1_0516.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.4.1.1.2** *P* **151** *L* **11** # 5

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **A** *AES*

In order to successfully detect DS PDs with a common ground, PSEs that support 4-pair operation have to switch the more negative conductor at least. This is already specificed for Environment A PSEs, but not for Environment B.

SuggestedRemedy

Add after the second paragraph of 33.4.1.1.2 the following sentence:

An Environment B PSE that supports 4-pair power shall switch the more negative conductor. It is allowable to switch both conductors.

Response *Response Status* **C**

ACCEPT.

TFTD, FS

Cl **33** *SC* **33.4.2** *P* **151** *L* **26** # 253

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **A** *AES*

"The PSE PI shall withstand without damage the application of short circuits of any wire to any other wire within the cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I LIM max as defined in Table 33-17."

No longer correct for the new Types.

SuggestedRemedy

Replace second sentence by:
"The magnitude of the current through such a short circuit:
- shall not exceed I LIM-2P max, as defined in Table 33-17, for Type 1 and Type 2 PSEs
- shall not exceed 0.85A for Type 3 PSEs
- shall not exceed I_LPS for Type 4 PSEs"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD

You are taking a statement that referenced I LIM max (which is the upperbound template) and replacing it with fixed numbers for Type 3 and Type 4. How does that work? Shouldn't all types just reference the upperbound template?

Replace second sentence by:
"The magnitude of the current through such a short circuit:
- shall not exceed IPSEUT-2P, as defined in Equation 33-15, for Type 1 and Type 2 PSEs
- shall not exceed IPSEUT-TYPE3-2P, as defined in Equation 33-16, for Type 3 PSEs
- shall not exceed IPSEUT-TYPE4-2P, as defined in Equation 33-17, for Type 4 PSEs"

Cl **33** *SC* **33.4.2** *P* **151** *L* **28** # 96

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **X** *AES*

The concerns of D1.6 comments 272 remain unaddressed.

The Fault tolerance section covers cases where a PSE is subjected to faults like link section conductor shorts. This section should contain similar requirements for new PDs so that they continue operating after a link segment conductor open fault has been removed.

SuggestedRemedy

Add the following text before the third paragraph of the called out section.

"Type-3 and Type-4 PDs shall withstand one or more conductor open failures within the link section without damage when powered by any PSE."

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.4.9.2** *P* **162** *L* **30** # 20

Darshan, Yair — Microsemi

Comment Type **ER** *Comment Status* **D** *Pres: Darshan15*

The Editor Note is not required anymore. All the necessary parameters were defined.

SuggestedRemedy

Delete Editor Note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD, YD

Cl **33** *SC* **33.6.3.2** *P* **169** *L* **44** # 166

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **X** *Pres: Yseboodt1*

LLDP can support extended power in a better way.

SuggestedRemedy

Adopt yseboodt_01_0516_lldpext.pdf

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.6.3.5** *P* **175** *L* **9** # 98

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **X** *Pres: Schindler1*

The San Antonio 2014 meeting presentation, Mutual_ID_PD_updated, change variable pse_dll_power_type to pse_dll_power_level and added variable pse_power_level for Type 3 and 4 state diagrams. This was probably done because Type no longer indicates the power being provided.

Unfortunately, this change:
1. Broke legacy DLL power control.
2. Broke DLL classification for new Types.

LLDP and the SD on p175 work together to provide LLDP field values. To reported PSE Type and not class, we need access to variable that reports Type.

SuggestedRemedy

This comment may be covered in schindler_3bt_01_05_16.

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **33** *SC* **33.6.4.1** *P* **176** *L* **31** # 99

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **A** *DLL*

It is incorrect to state that a thing has human properties, liking seeing.

SuggestedRemedy

Existing text:
If the PSE sees a change to the previously stored MirroredPDRequestedPowerValue, it recognizes a request by the PD to change its power allocation.

Corrected:
If the PSE previously stored MirroredPDRequestedPowerValue changes, a request by the PD to change its power allocation is recognizes.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

If the PSE previously stored MirroredPDRequestedPowerValue changes, a request by the PD to change its power allocation is recognized.

TFTD, DS

Cl **33** *SC* **33.6.4.1** *P* **176** *L* **44** # 100

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **A** *DLL*

It is incorrect to state that a thing has human properties, liking seeing.

SuggestedRemedy

Existing text:
If the PD sees a change to the previously stored MirroredPSEAllocatedPowerValue or local_system_change is asserted by the PD so as to change its power allocation, it enters the PD POWER REVIEW state.

Corrected:
If the PD previously stored MirroredPSEAllocatedPowerValue is changed or local_system_change is asserted by the PD so as to change its power allocation, it enters the PD POWER REVIEW state.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

TFTD, DS

If the PD previously stored MirroredPSEAllocatedPowerValue is changed or local_system_change is asserted by the PD so as to change its power allocation, the PD enters the PD POWER REVIEW state.

Cl **79** *SC* **79.3.2** *P* **203** *L* **27** # 101

Schindler, Fred — Seen Simply, Broadco

Comment Type **TR** *Comment Status* **X** *Pres: Schindler2*

Accepted draft 1.4 comments broke extended power operation using LLDP and DLL. An ad hoc meeting reviewed these concerns during D1.5 review cycle and a very busy person was not able to complete a solution for the D1.6 review cycle.

SuggestedRemedy

A solution should appear in schindler_3bt_02_05_16 or other related presentation for this review cycle.

Proposed Response *Response Status* **W**

WFP

TFTD

Cl **79** *SC* **79.3.2.6b.3** *P* **208** *L* **31** # 238

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *LLDP*

In Table 79-6b and section 79.3.2.6b.3 the "PD PI" bit is described. Given the recent evolutions we made in defining single and dual signature PDs, this bit no longer serves any purpose. It can however be repurposed to make LLDP support dual-signature PDs in a proper way.

SuggestedRemedy

- Rename "PD PI" to "PD Mode selection"
- Change value of item 2 in Table 79-6b to read:
"1 = PD requested power applies to Mode A pairset
0 = PD requested power applies to Mode B pairset"
- Change text in 79.3.2.6b.3 to read:
"This field shall be set according to Table 79-6b to select the Mode for which the PD is requesting power when the power type is PD. This field shall be set to 0 when the power type is PSE."

Proposed Response *Response Status* **W**

TFTD

I would like those group members interested in LLDP to review this change as it seems substantial.

Fred and Lennart to work on.

Cl **33** *SC* **33.3.7** *P* **231** *L* **52** # 216

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Pres: Darshan12*

"Selected resistance values for RPSE_max and RPSE_min which provide adequate verification to Equation (33-13) or control ICon-2P-unb value are dependent upon PSE circuit implementation and as such are left to the designer."

PARSE_ERROR.

SuggestedRemedy

I don`t know where to begin. What does this mean ?

Proposed Response *Response Status* **W**

Yair?

TFTD

Yair to send to reflector, Darshan 12.