

Info (not part of baseline)

Figure 145–22 is a test fixture that is used in the PSE unbalance requirement. Because it was originally drawn for an Annex, it is too elaborate and shows parameters beyond the PI. It also contains a PD model, which is non-relevant for the PSE unbalance specification.

The equivalent Figure on the PD side is much better (Figure 145–31). Figure 145–22 is redrawn in the style of 145–31 and the PD specific details are abstracted away. The PD specification uses R_{source_min} and R_{source_max} as the test fixture parameters, for the PSE side we introduce R_{load1} and R_{load2} .

145.2.8.5.1 PSE ~~PI~~ pair-to-pair ~~effective resistance and~~ current unbalance

PSEs that operate over 4 pairs are subject to unbalance requirements. The contribution of PSE PI pair-to-pair effective resistance unbalance to the system end to end effective resistance unbalance is specified by PSE maximum (R_{PSE_max}) and minimum (R_{PSE_min}) common mode effective resistance in the powered pairs of same polarity, see ~~Figure 145–22~~ Figure 145A–0a.

...

A PSE shall not source more than $I_{Con-2P-usb_min}$ on any pair when connected to a load as shown in Figure 145–22, using values of R_{load_min} and R_{load_max} as defined in Equation (145–16) and Equation (145–17).

...

~~R_{PD_min} and R_{PD_max} are respectively the minimum and maximum common mode effective PD PI resistances. They account for the effective resistance of the resistive elements, combined with the PD pair-to-pair voltage difference and the effect of system end-to-end pair-to-pair unbalance. See Annex 145A.~~

~~$R_{Ch_unb_min}$ and $R_{Ch_unb_max}$ are respectively the minimum and maximum common mode link section resistances in the powered pairs of the same polarity from the PSE PI to the PD PI per the model described in Figure 145A–1.~~

~~The sum of $R_{Ch_unb_min}$ from the positive pairs and $R_{Ch_unb_max}$ from the negative pairs is $R_{Chan-2P}$ as described in Figure 145–22 and as defined by the link section pair-to-pair resistance unbalance requirement for 4-pair operation in 145A.3.~~

Table 145–17 specifies the values of resistance used to compute R_{load_min} and R_{load_max} according to Equation (145–16) and Equation (145–17) and Figure 145–22. ~~The values of R_{PD_min} and R_{PD_max} are given to allow calculations and measurement of P_{Class_PD} at the PD PI. The load resistances R_{load_min} and R_{load_max} are split into two series resistances R_{load1_min} and R_{load2_min} , and R_{load1_max} and R_{load2_max} respectively, as shown in Figure 145–22, to correctly be able to set the power sink.~~

Rename as follows in Table 145–17:

$R_{Ch_unb_min}$	→	R_{load1_min}
$R_{Ch_unb_max}$	→	R_{load1_max}
R_{PD_min}	→	R_{load2_min}
R_{PD_max}	→	R_{load2_max}

Change Equation 145–16 and 145–17 to the following:

$$R_{load_min} = R_{load1_min} + R_{load2_min} \quad (145-16)$$

$$R_{load_max} = R_{load1_max} + R_{load2_max} \quad (145-17)$$

where

R_{load1_max}	is, given R_{load1_min} , the higher resistance value representing the link section resistance
R_{load1_min}	is the lower resistance representing the link section resistance
R_{load2_max}	is, given R_{load2_min} , the higher resistance value representing the PD unbalance
R_{load2_min}	is the lower resistance representing the PD unbalance

$I_{Con-2P-usb}$ and Equation (145–15) are specified for total channel common mode pair resistance $R_{Chan-2P}$ from 0.2 Ω to 12.5 Ω and worst case unbalance contribution by a PD. ~~See 145A.3 for guidelines on how to support low resistance link sections. PSEs that support channel common mode resistance less than 0.2 Ω , or if R_{Chan} is less than 0.1 Ω , the PSE should meet $I_{Con-2P-usb}$ requirements when connected to $(R_{load_min} - 0.5 \times R_{Chan-2P})$ and $(R_{load_max} - 0.5 \times R_{Chan-2P})$. This can be achieved by using a lower R_{PSE_max} or higher R_{PSE_min} than required by Equation (145–15). Lower~~

~~R_{PSE_max} values may be obtained by using smaller constant α or higher R_{PSE_min} in Equation (145–15) in the form of $R_{PSE_max} = \alpha \times R_{PSE_min} + \beta$.~~

Replace Figure 145–22 as follows:

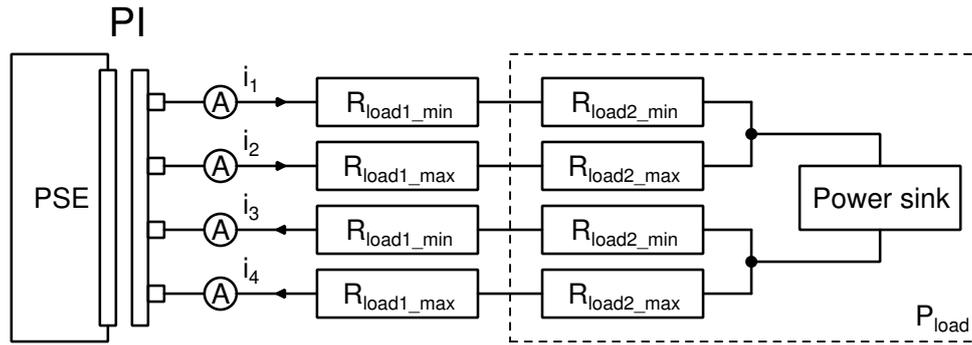


Figure 145–22 — PSE current unbalance verification circuit

Replace the evaluation method on page 161 lines 22 to 32 by the following:

The evaluation method is as follows:

- Use R_{load_min} and R_{load_max} from Equation (145–16) and Equation (145–17) for low channel resistance conditions.
- Adjust the power sink such that P_{load} (the power consumed by the R_{load2} resistances and the power sink) equals P_{Class_PD} for the given Class
- Verify that i_1 , i_2 , i_3 , and i_4 are lower than $I_{Con-2P-usb}$, as defined in Table 145–16.
- Exchange R_{load_max} and R_{load_min} . Repeat steps b) and c).
- Repeat steps b) through d) for R_{load_min} and R_{load_max} from Equation (145–16) and Equation (145–17) for high channel resistance conditions.

145.3.8.10 PD pair-to-pair current unbalance

On page 196, line 32, change as follows:

where

...
 R_{source_min} is, ~~given R_{source_max}~~ , the ~~highest lowest~~ allowable common mode effective source resistance in the powered pairs of the same polarity
 ...

Replace Figure 145–31 as follows:

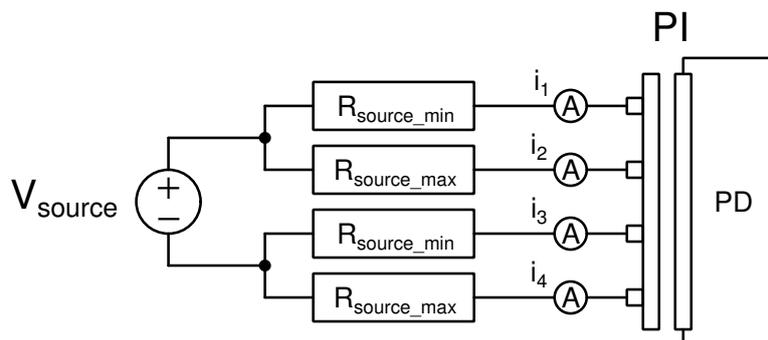


Figure 145–31 — PD current unbalance verification circuit

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We still need a Figure that shows R_{PSE_min} and R_{PSE_max} as these parameters are referred to in the text. We can replace Figure 145A–1 with something that shows all.

Annex 145A

Insert new subclause before 145A.2 as follows:

145A.1a Unbalance overview

Pair-to-pair current unbalance is caused by unequal resistances in a parallel current path of the same polarity. The PSE, the PD, and the link section connecting those independently contribute to unbalance. A system model for the worst-case instance of this is shown in Figure 145A–0a.

R_{PSE_min} or R_{PSE_max} common mode effective resistance is the resistance of the two internal conductors (including the internal components on each conductor) in a powered pair of the same polarity connected in parallel.

$R_{Ch_unb_min}$ and $R_{Ch_unb_max}$ are respectively the minimum and maximum common mode link section resistances in the powered pairs of the same polarity from the PSE PI to the PD PI per the model described in Figure 145A–1.

R_{PD_min} and R_{PD_max} are respectively the minimum and maximum common mode effective PD PI resistances. They account for the effective resistance of the resistive elements, combined with the PD pair-to-pair voltage difference and the effect of system end-to-end pair-to-pair unbalance.

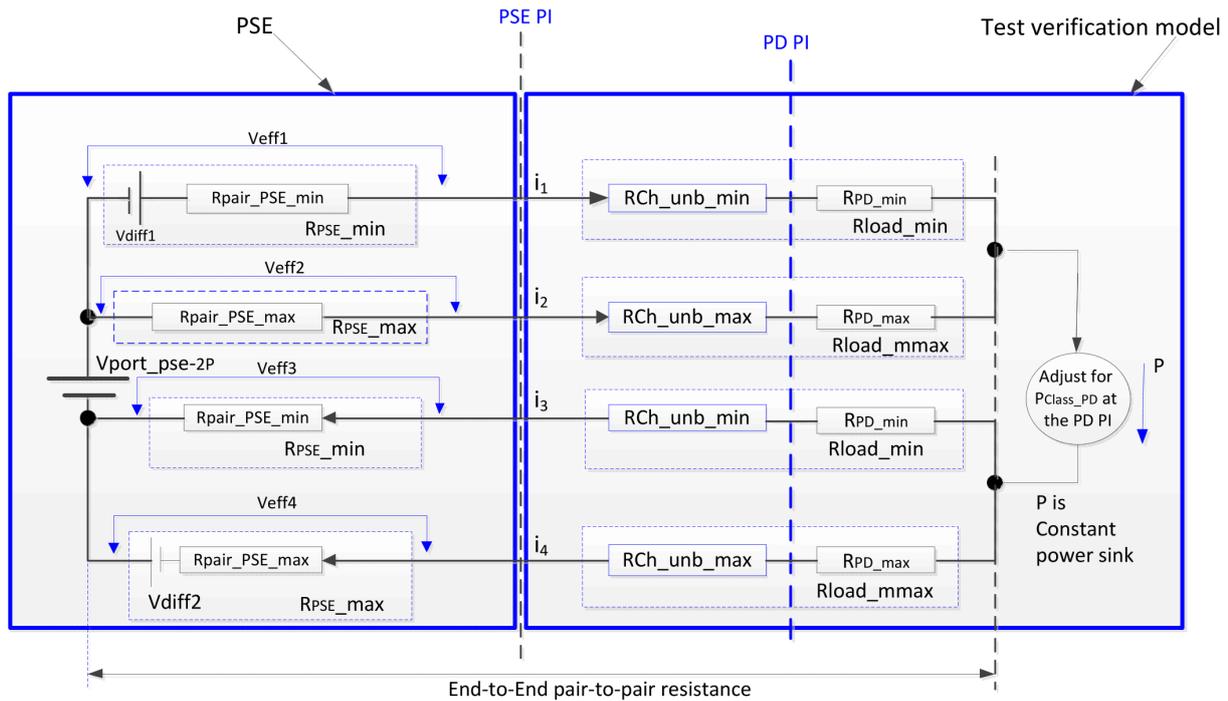


Figure 145A–0a — PD current unbalance verification circuit

145A.3 PSE resistance and current unbalance

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Comments that affect this paragraph must be implemented before moving. Specifically, comment i-422 changes this paragraph. Make sure to implement changes in Annex.

Append at the end of this subclause:

$I_{Con-2P-usb}$ and Equation (145–15) are specified for total channel common mode pair resistance $R_{Chan-2P}$ from 0.2 Ω to 12.5 Ω and worst case unbalance contribution by a PD. PSEs that support channel common mode resistance less than 0.2 Ω , or if R_{Chan} is less than 0.1 Ω , the PSE should meet $I_{Con-2P-usb}$ requirements when connected to $(R_{load_min} - 0.5 \times R_{Chan-2P})$ and $(R_{load_max} - 0.5 \times R_{Chan-2P})$. This can be achieved by using a lower R_{PSE_max} or higher R_{PSE_min} than required by Equation (145–15). Lower R_{PSE_max} values may be obtained by using smaller constant α or higher R_{PSE_min} in Equation (145–15) in the form of $R_{PSE_max} = \alpha \times R_{PSE_min} + \beta$.