Power Matters

Microsemi

Type 3/4 PSEs Inrush_max value with Type 1/2 PDs

IEEE802.3bt

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Rev 005

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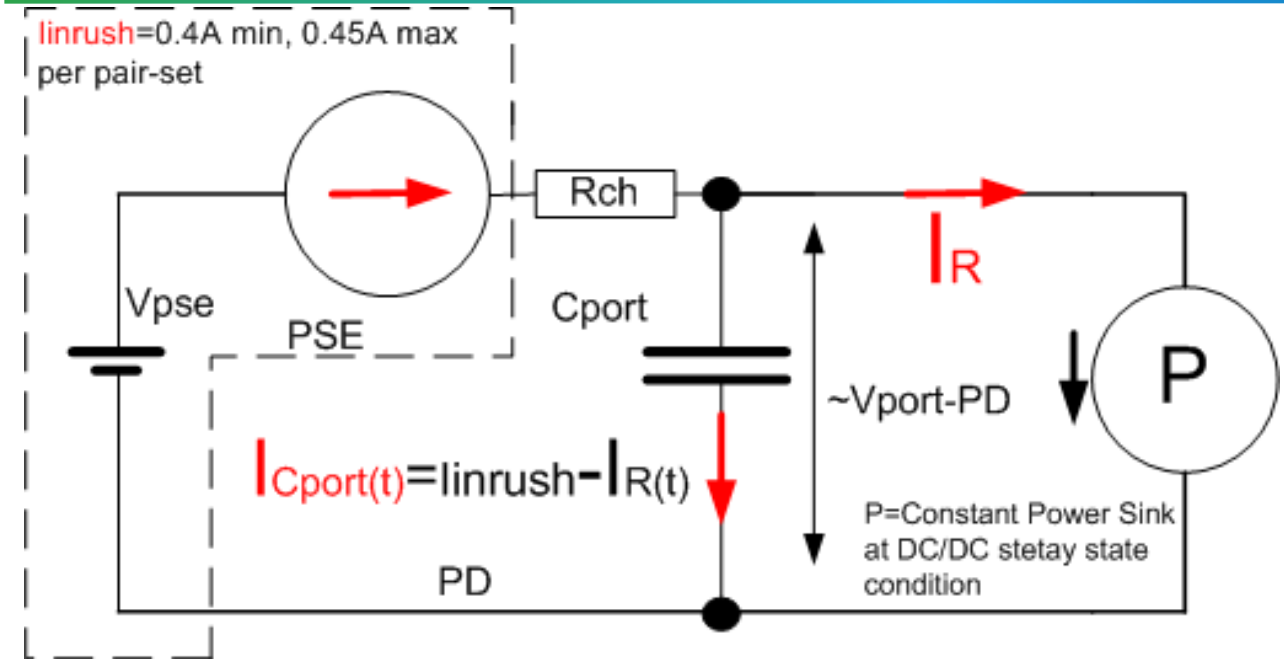
Objectives

- To show that Type 1 PD when connected to Type 3 or 4 PSE can handle and must handle Type 3 and 4 Iinrush max due to other systems requirements beyond Iinrush.
- Moreover: a PD that can't do the above, violates the following standards:
  - IEEE requirements
  - Practical considerations in system level.

POWER_UP Model



Iload is varied until
Tinrush=50msec is achived.

- For a given PD with:
- Vport=57V, Iinrush=0.425A, Iload=0.244A, Cpd=180uF and Tinrush=50msec. Then Energy =0.64Joul.
- E=0.45A*49msec*57V/2=~0.63Joul (Ignoring the first 1msec..)
- If Iinrush increased to 0.9A, Charging time is shorten to 15msec. Then total energy is reduced to 0.4Joul.
- For PD with Iload=0. It will be the same energy for Inrush=0.45A and 0.9A : 0.292joul
- **If we add the 50A part, Energy>>0.292Joul and > 0.63Joul.**

Iinrush limitis for Type 1 and 2

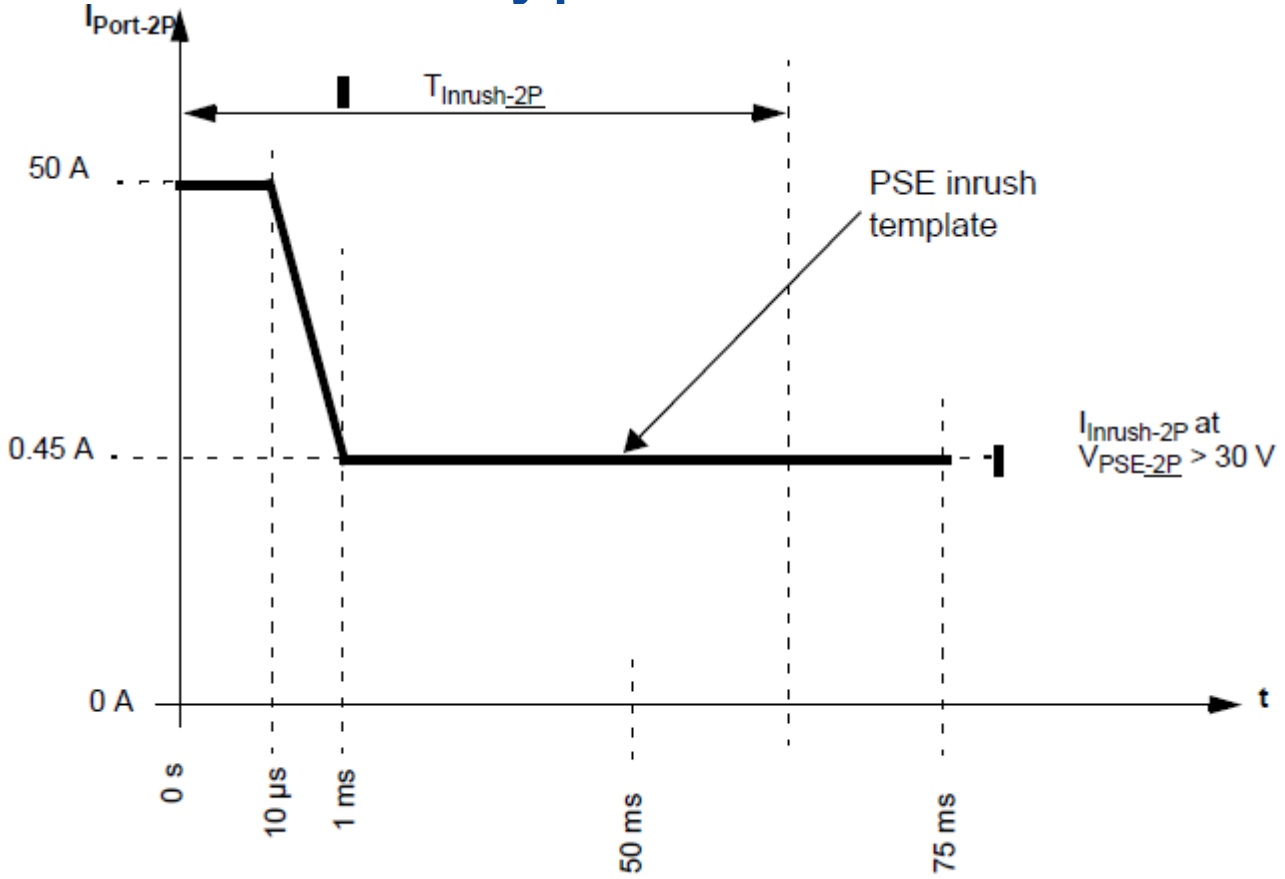


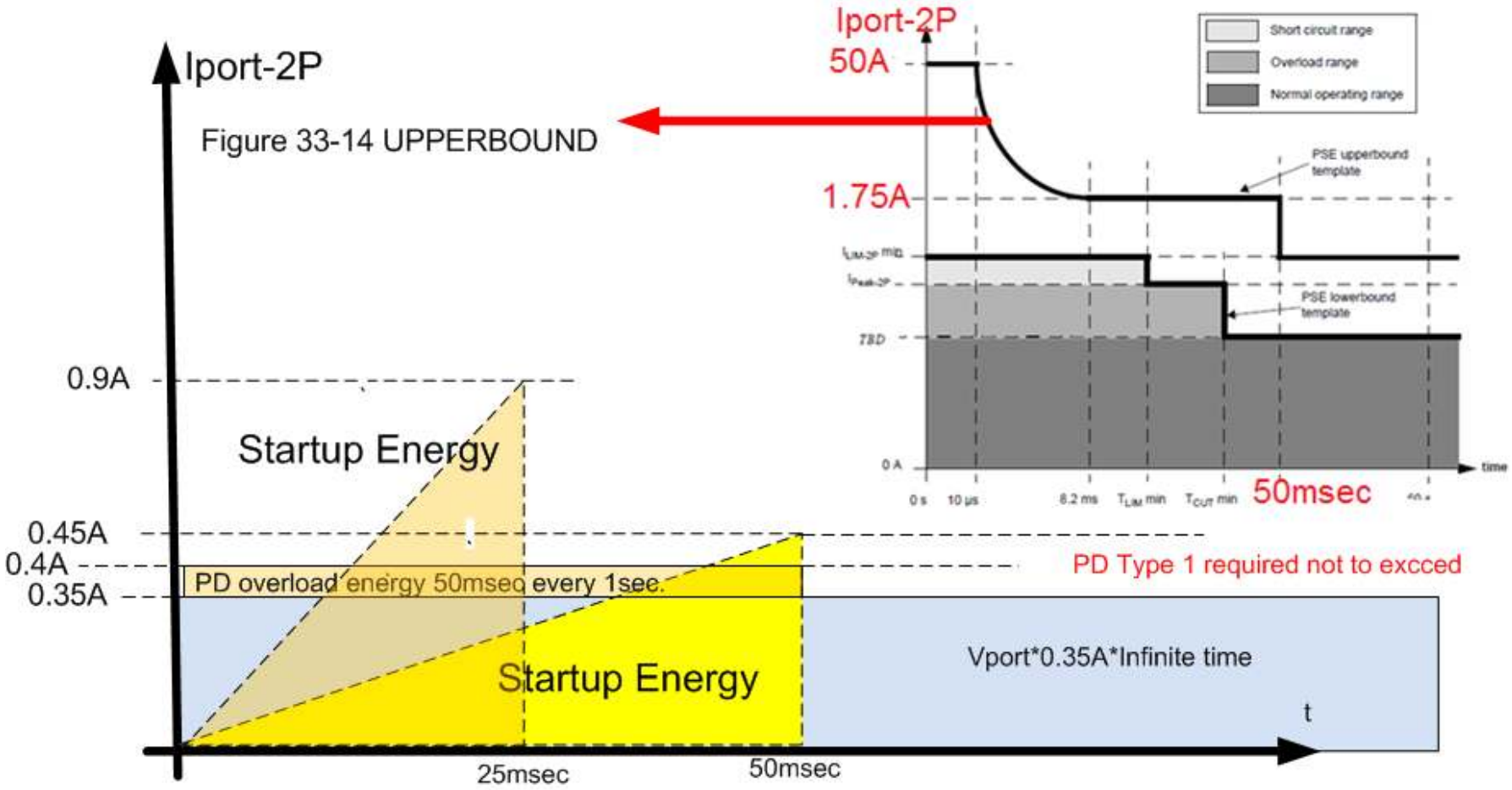
Figure 33–13—$I_{Inrush-2P}$ current and timing limits, per pairset in POWER_UP

(1) 50A.➔ I^2*t =2500A^2*t ! (The Fusing Energy). It is >>0.45A^2*t for the 50A area.
~5000 times higher !

(2) Inrush Energy=49msec*57V*0.45A + $\approx \int_0^{1msec} 57V \cdot t \cdot i(t)dt$ >0.63Joule

Type 3/4 PSE connected to Type 1/2 PD

- Same Energy **or lower** if Inrush increased from 0.45A to 0.9A ignoring the 50A part….:
- Needs to meet PSE upperbound >> 0.45A (1.75A/50msec, and 50A/10usec➔1msec.



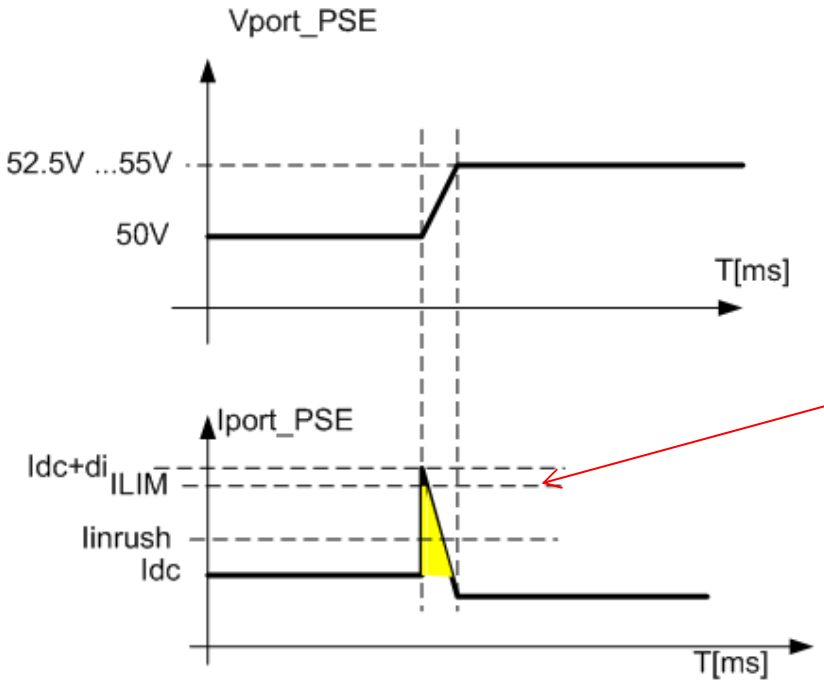
Typical use cases were Iport>Iinrush

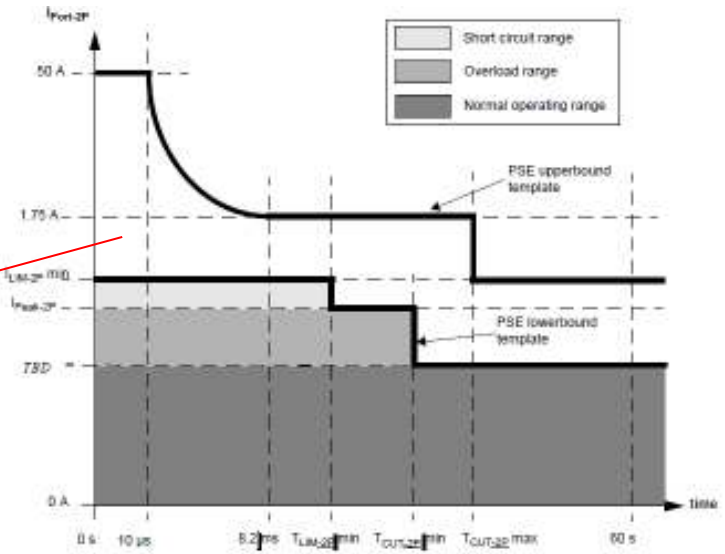
33.2.7.7:

The PSE shall limit the a pair set current to ILIM-2P for a duration of up to TLIM-2P in order to account for PSE dV/dt transients at the PI pair set

- PSE can limit up to UPPERBOUND template. PD sees Inrush like >>Iport

Ipeak=Idc+180uF*5V/0.5msec=(Idc+1.8A) **> Iinrush=0.45A max**
Actual Ipeak is limited by ILIM which can be anything up to upper bound template.





What if worst case happen?

- Vpse_1=50V
- Vpse_2=57V (backup)
- Rate of change: 0.1msec
- Cport=180uF.
- Iinrush_Peak=C*dv/dt=180uF*7V/0.1msec=12.6A

- What if dv/dt is faster? Then >12.6A.

- Conclusion: PD must have internal current protection.
- PD must survive Inrush like currents>>0.45A.

Conclusions

- PD Can and should handle Iinrush max=0.9A when Type 3 PSE connected to PD Type 1.
- PD needs to meet much higher currents anyway

Summary

- PD Ioverload≤0.4A at all times ➔ Needs internal limits. See table 33-18.
- Need to stand Iinrush up to **50A** per Figure 33-13
- Inrush of 0.45A for 50msec is the same energy of Iinrush=0.9A at 25msec.
  - **Energy with higher inrush may result with lower energy for a given Type 1 PD.**
- PDs needs to handle transient **current of 2.5A** (or higher) per 33.3.7.6 (PSE dv/dt).
  - It is the same mechanism as Iinrush (charging capacitor).
- PDs need to tolerate current levels below the upperbound of figure 33-14
  - <50A, 1.75A, Ppeak, Pclass as function of the different timings.
- PDs that are not protected when connected to any power source are violating UL requirements.
- Therefore PD Type 1 that exposed to Iinrush of 0.9A instead of 0.45A is not an issue when the above requirements are met.
- System vendors do not want to be liable for poorly designed PDs or non compliant PDs
- Therefore, Type 3 and 4 PSEs limited to 0.4A-0.45A to Type 1/2 PDs could be a feature but can not be mandatory. PD need to be designed to handle higher than 0.9A anyway.

Proposed Changes for D1.3

#	Parameter	Symbol	Units	Min	Max	PSE Type	Additional Information
5	Output current in POWER_UP state	Iinrush	A	0.4	See Info	1,2,~~3,~~ ~~4~~	~~For Type 1 and Type 2 PDs.~~ See 33.2.7.5. Max value defined by Figure 33-13.

Discussion

THANK YOU

Backup slides

- Originally presented in July 2015

Background

- PD Type 1 or 2 works with PSE Type 1/2 with Inrush=0.4A to 0.45A.
- When Type 3 or 4 PSE is connected to Type 1 and 2 PDs with Iinrush capability of 0.4 to 0.45A per pairset (Total 0.8A to 0.9A if both pair sets are ON together):
  - The stress on the components up to the diode bridges outputs stays the same.
  - The capacitor will see twice the charging current for half of the time which is the same energy.
  - Series resistance such EMI filters dumping elements and hot swap MOSFET needs to meet: t*R*Icont^2 >> 25ms*R*0.9^2)/3.
  - In addition all the components above need to meet much higher current transients etc. due to internal and external effects (UL, IEEE etc.).
- What if during operation a **pair set** is disconnected?
  - Nothing happen. It is similar to Type 1/2 system. Same currents.
- What if during operation only a pair is disconnected?
  - One diode bridge and one transformer will see 0.9A for maximum 25msec.
  - Same energy stress for shorter time. No issues.
    - Moreover : In POWER ON the currents are higher for longer time (until system shuts off) which is worsen than the previous case ➔ No issues.

What a PD need to do for its own protection?

- **IEEE (**Need to be guaranteed by PD at all times)**:**
- Type 1: Not to consume more than 0.4A for more than 50msec.
- Type 2: Not to consume more than ~0.6A*1.14 for more than 50msec
- All types: to meet PSE dv/dt that will generate Ipeak=2.5A and will be limited by PSE ILIM.

- **UL:** Not to to cause fire hazard or damage to infrastructure if it has internal short circuit when connected to any power source with any current capability.
  - Consider possible scenario:
  - PD is connected to a PSE multiport system with 1KW main power supply. One of the PSE port controller is permanently ON due to a fault in PSE. Now PD sees 1KW power source
  - PD is tested in the LAB with lab power supply that is not PoE current limited or LPS limited.
    - All of the above considered single fault condition in the tested device.

33.3.7.6 PD behavior during transients at the PSE PI

A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after TLIM min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from VPort_PSE min to VPort_PSE max at 2250 V/s.

A Type 2 PD shall meet both of the following: a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5Ω, and a source that supports a current greater than 2.5 A.

Energy Calculations – Figure 33-14

1msec to 50msec	0.628
0 to 1msec, 0.45A	0.0256
0 TO 10usec 50A	0.0285
10us to 1msec, 50A to 0.45A (V*I*t/4)	0.706
Total (Joule)	1.388