33.2.9.1.2 PSE DC MPS component requirements

Editor: Removed existing text

~~A PSE shall consider the DC MPS component to be present if $I_{Port\ 2P}$ or the sum of $I_{port\ 2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if $I_{Port\ 2P}$ or the sum of $I_{port\ 2P}$ of both pairs of the same polarity is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if $I_{Port\ 2P}$ or the sum of $I_{port\ 2P}$ of both pairs of the same polarity is in the range of I_{Hold}.~~

~~The values of $I_{Port\ 2P}$ or the sum of $I_{port\ 2P}$ of both pairs of the same polarity and the corresponding values of I_{Hold} shall meet the conditions specified in Table 33–11.~~

~~A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall monitor either the sum of $I_{port\ 2P}$ of both pairs of the same polarity or the pairset with the highest $I_{Port\ 2P}$ current value and use the appropriate I_{Hold} level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.~~

~~A Type 3 or Type 4 PSE, when connected to a dual-signature PD shall monitor each pairset and use the appropriate I_{Hold} level shown in Table 33–11. The PSE shall remove power from any pairset on which the DC MPS has been absent for a duration greater than T_{MPDO}.~~

~~The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when *$I_{Port\ 2P}$ or the sum of $I_{port\ 2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max* continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.~~

Editor: Replace with following text

All types of PSE, depending on the connected type of PD, will use the applicable I_{Hold} min, I_{Hold} max, T_{MPS} and T_{MPDO} values as defined in Table 33–11. The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component.

A Type 1 and 2 PSE shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}. A Type 1 and 2 PSE shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ is less than or equal to the applicable I_{Hold} min. A Type 1 and 2 PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of the applicable I_{Hold}.

Type 1 and 2 PSEs shall remove power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

A Type 1 and 2 PSE shall not remove power from the port PI when I_{port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every DC MPS has been present every T_{MPS} + T_{MPDO}, as defined in Table 33–11.

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ of the pairset with the highest current or the sum of $I_{port\text{-}2P}$ of both pairsets of the same polarity is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}. A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall consider the DC MPS component to

be absent if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity are less than or equal to the applicable I_{Hold} min. A Type 3 or Type 4 PSE, when connected to a single-signature PD, may consider the DC MPS component to be either present or absent if $I_{Port-2P}$ of the pairset with the highest current or the sum of $I_{Port-2P}$ of both pairsets of the same polarity is within the range of the applicable I_{Hold}.

Type 3 and 4 PSEs, when connected to a single-signature PD, shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

Type 3 or Type 4 PSEs, when connected to a single-signature PD, shall not remove power from the PI when DC MPS has been present within the trailing $T_{MPS} + T_{MPDO}$ window.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present or absent on a pairset independently from the other pairset. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be present on a pairset if $I_{Port-2P}$ is greater than or equal to the applicable I_{Hold} max continuously for a minimum of T_{MPS}. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, shall consider the DC MPS component to be absent on a pairset if $I_{Port-2P}$ is less than or equal to the applicable I_{Hold} min. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may consider the DC MPS component on a pairset to be either present or absent if $I_{Port-2P}$ is within the range of the applicable I_{Hold}.

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}.

Type 3 or Type 4 PSEs, when connected to a dual-signature PD, shall not remove power from a pairset when DC MPS has been present on both pairsets every $T_{MPS} + T_{MPDO}$. A Type 3 or Type 4 PSE, when connected to a dual-signature PD, may maintain power on a pairset if DC MPS has been present on that pairset every $T_{MPS} + T_{MPDO}$.

The DC MPS rules allow a PD to minimize its power consumption.