

COMPATIBILITY CONSIDERATIONS FOR 50 AND 100G



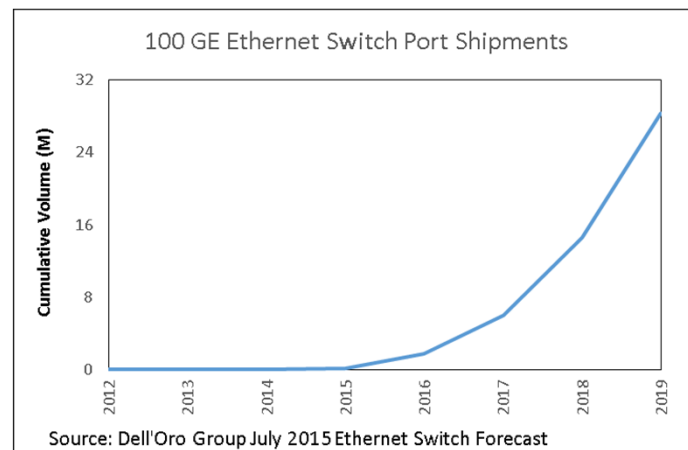
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MARKET NEED



- Both 100GE and 50GEc* are existing MAC rates
- There will be a large and growing installed base of 100GE (~ 15M cumulative in 2018)
 - Data applies to 4 x 25 G interfaces used in switch applications
 - [These ports can typically be configured as 4 x 25GE, or 2 x 50GEc also]



Used with permission

- Do we need to make consideration in 50 / NOGOATH for connection of new 50G based PMDs to these “legacy” 100 & 50G ports based on 25Gb/s serdes?

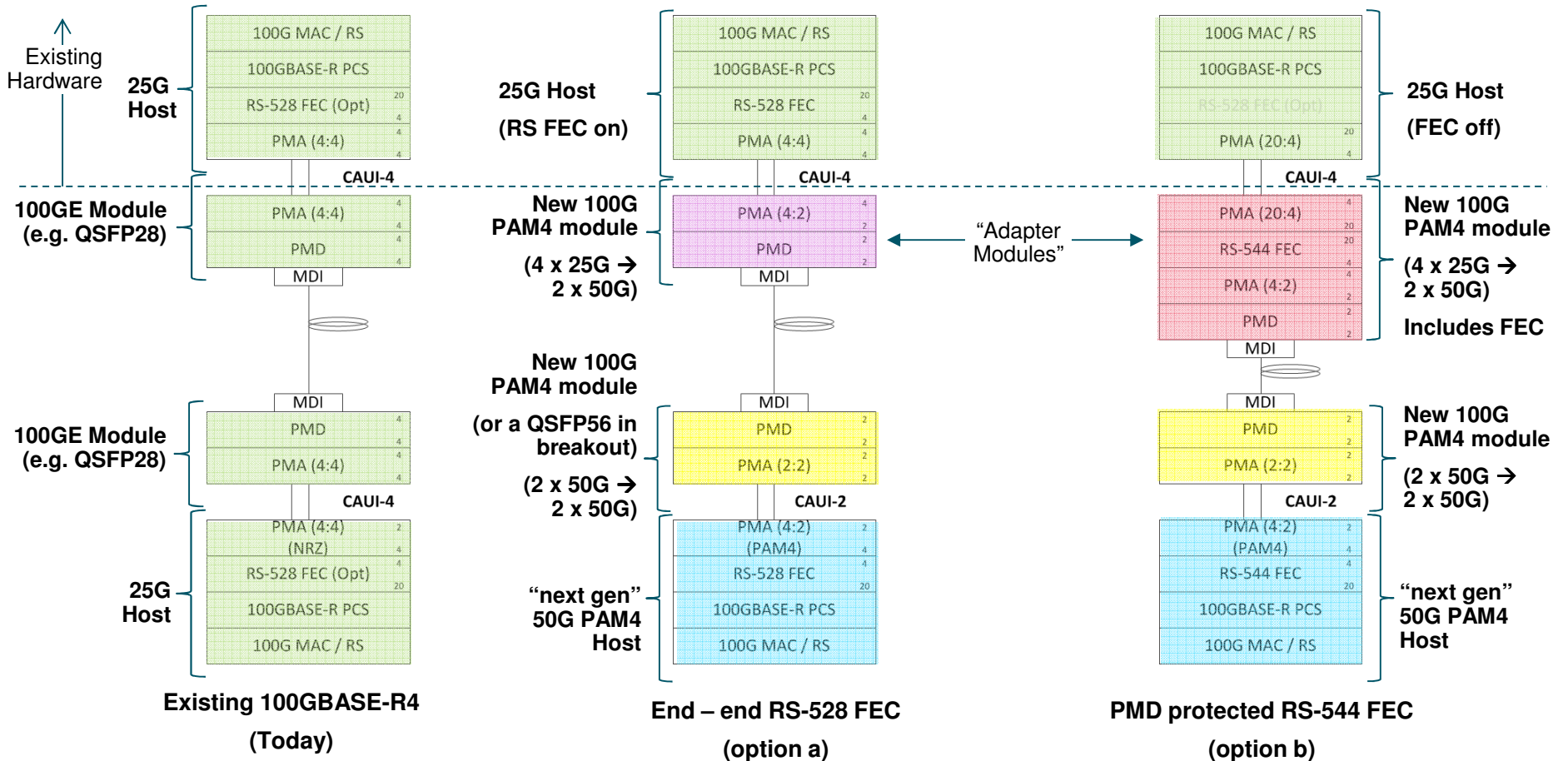
* GEc used to denote 25 / 50G Consortium Specification

POSSIBLE GOALS FOR NEXT SET OF 50G PCS & PMDS



- **An architecture which permits straightforward connection of 50G / lane capable hosts to existing devices / technologies –**
 - 100GBASE-R4 PHYs
 - 50GEc (2 x 25G) PHYs – (non-IEEE variant - 25 / 50G Consortium Specification)
- **Offer low power and low latency where possible**
- **Plug and play for existing hardware**
 - Ideally an “adapter module” which enables use of both 50G / lane PMD and offers connection to next gen 50G capable host
- **Cost optimized**
 - Permits legacy designs to take advantage of new 50G based PMDs
 - Use appropriate FEC where possible to ease implementation challenges (applies to both optics and electrical PMDs)
- **Consider re-use where practical of existing work / developed IP**
 - FEC
 - MACs
 - PMAs
 - Modules / management interfaces

100GE ARCHITECTURE EXAMPLES:



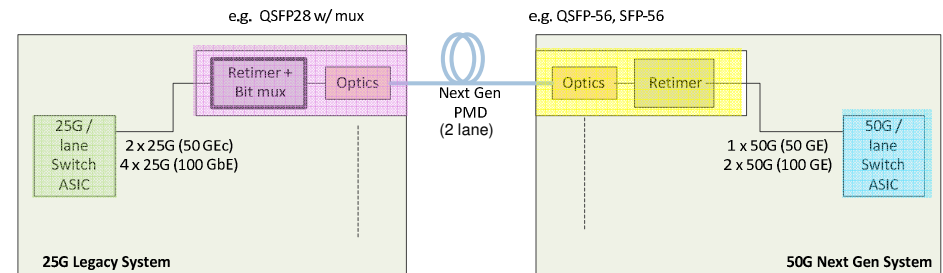
OBSERVATIONS (100G)



- **The simplest architecture relies on end-end FEC borrowed from 100GBASE-R4**

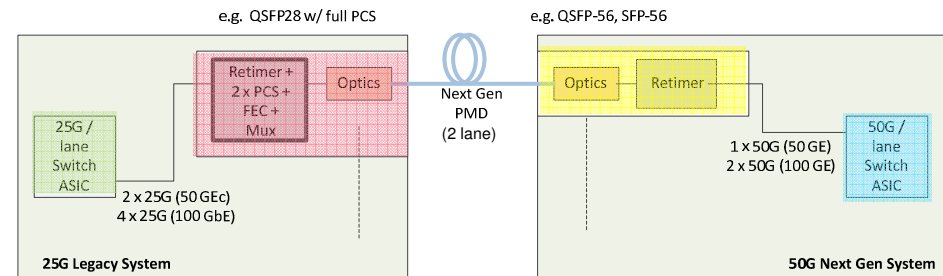
- **(option a)**

- This enables an QSFP28 with a simple PMA mux (4 x 25G → 2 x 50G lanes) – no change to CAUI-4 spec, or module mangement
 - Would enable plug and play upgrade to 100G over 2 lane PMD with no hardware change on legacy designs
 - Open question – does RS-528 provide adequate end – end gain for the 50G based PMDs and AUI?
 - Cons: no passive copper support, as requires the mux function in the module



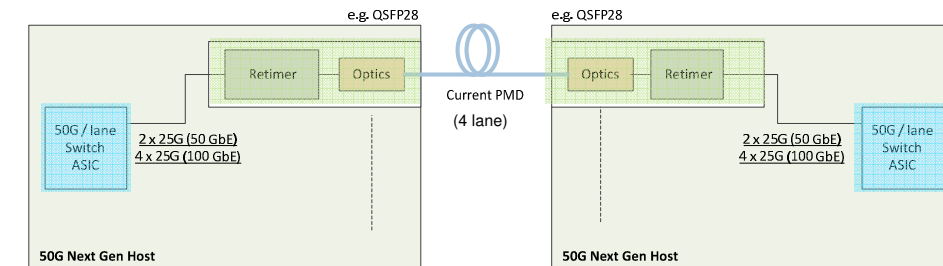
- **Alternative: add RS-544 FEC with appropriate PMAs to Module PHY or Gearbox on PCB (option b)**

- **Drawback for Module:** Power envelope, BOM cost adder
 - **Drawback for PCB:** No longer a legacy hardware design
 - **Drawback for management** – SFF 8636 update / management for full PCS / FEC (would be required to be managed over I2C, or transition to MDIO and use CL45)



- **“Do nothing” alternative is to not make allowance in 50G based projects for backwards compatibility**

- Force 50G next gen designs to run in 25G “down speed” mode to connect to legacy
 - **Drawback:** Increases lane use by x 2 on next gen silicon, reduces switch radix, increases number of required switch stages to span a given network size



FOR DISCUSSION



- **For 50 GE and 100 GE hosts using 50G / lane, should we consider an architecture which enables a streamlined connection to existing hosts based on 25G lane rate technology?**
 - Would enable use of 50G / lane PMDs for cost savings (2 x narrower # lanes)
 - Would enable next gen 50G host to operate at maximum bandwidth
 - Enables 25G and 50G based hosts to be used in the same environment without a significant penalization (hard to coordinate migration of all technologies to next lane speed FPGA, switch, NIC, ...)

- **Simplest architecture (option a) would put a bit-mux in the module CDR, and requires that the AUI / PMD is protected with the existing end – end RS-528 FEC**
 - Is this adequate FEC gain *for a subset* of candidate PMDs?

- **An alternative view: Make no consideration for backwards compatibility with existing 25G based hosts in 50G / NGOATH projects**
 - i.e. require a 200GBASE-R4 port be operated down-speed at 100GBASE-R4 to connect to legacy 25G silicon
 - Drawback: this mode handicaps the next gen 50G host by requiring a down-speed of the AUI to 25G, with associated loss in radix / IO capacity and increase in network size



Thanks!