Leveraging CEI-56G-LR-PAM4 Efforts for IEEE 802.3 50G Backplane

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Purposes

- Review the status of the CEI-56G-LR-PAM4 project, and discuss why and how to leverage this highly relevant effort for the IEEE 802.3 50G backplane (BP) project
- Leveraging to achieve better spec project efficiency, and product development cost effectiveness crossing both Ethernet and OTN markets

I. CEI-56G-LR-PAM4 Highlights

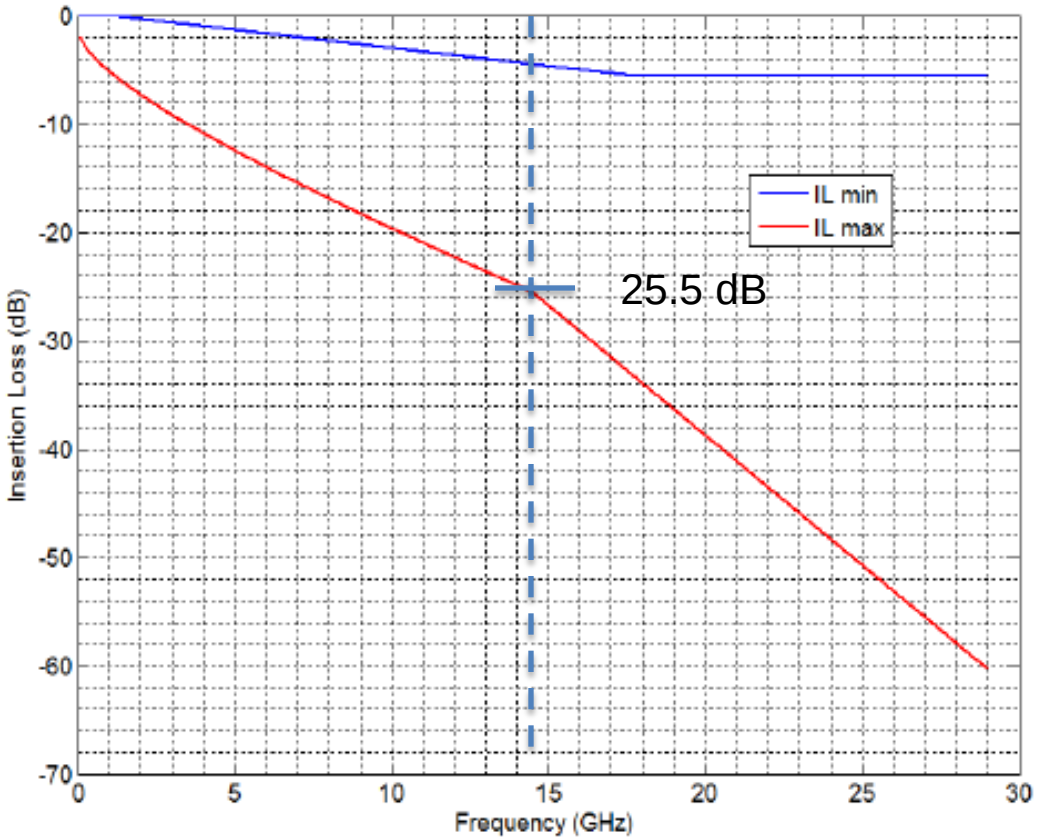
CEI-56G-LR Project Objectives (oif2014.235.01)

- **Project Output:**
  - Single IA specifying backplane interfaces of 1 to N lanes, each lane consisting of W wires.
  - One or more electrical specifications for lane operation at the rate of 19.5 to 28.1 Gb/s per wire.
  - Reach range: 0 to 1000mm (TBD based on max loss and materials) plus two connectors

- **Project Requirements:**
  - Support AC coupling
  - Bit Error Ratio of 1E-15 or better (FEC may be used to achieve this)
  - Document constraints of the backplane applications used to derive the channel model specifications.
  - Minimize power (pJ/bit) requirements.

CEI-56G-LR-PAM4 Spec Highlight (I)

- IL Max target: currently set at 25.5 dB at Nyquist



Latest CEI-56G-LR-PAM4 Spec draft: OIF2016.025.01

CEI-56G-LR-PAM4 Spec Highlight (II)

- The Channel Operating Margin (COM) is the FOM for channel
- Ref TX: 4-tap FIR, 2 pre and 1 post
- Ref RX: CTLE: with both low and high-freq pole/zero pairs; DFE: 12-taps, limit the C-1 <=0.5, and the rest Cn <=0.2

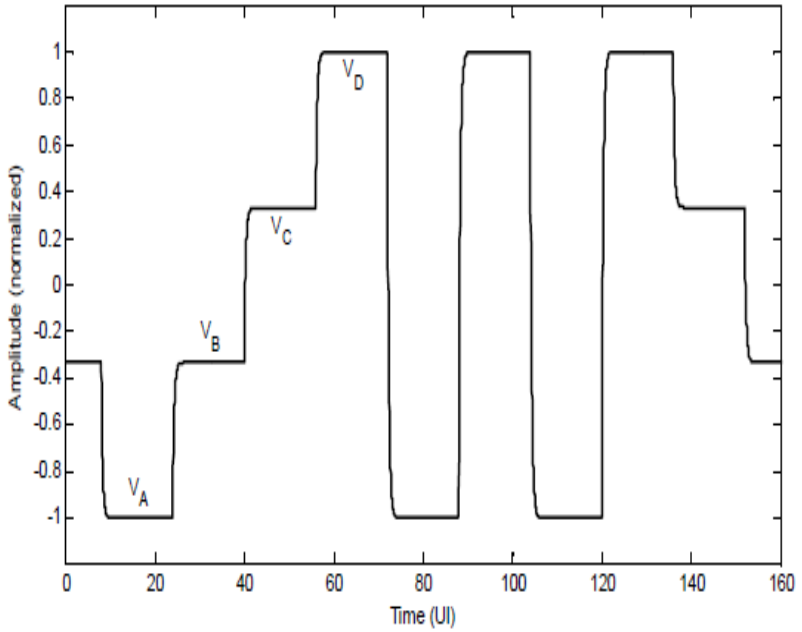
Parameter	Symbol	Value	Units
Signaling rate	f_b	18 - 29	Gsym/s
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Differential impedance	 C_d z_p z_p C_p z_c	 250 12 30 110 90	 fF mm mm fF Ohm
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	0.75 × f_b	
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.60	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 –0.10 0 0.02	 — — —
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.28 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.28 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequencies	f_z f_{z2}	f_b /2.5 f_b /40	GHz GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2} f_{p3}	f_b /2.5 f_b / 40 f_b	GHz GHz

Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.43* 0.43* 0.65	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit for n = 2 to N_b	$b_{max}(1)$ $b_{max}(2\text{-}N_b)$	0.5 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	2.6×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—
Channel operating margin, min	COM	3	dB

See also OIF2015.336.00

CEI-56G-LR-PAM4 Test Parameters/Methodology:TX

- Conventional parameters:
  - Diff and CM voltages, AC and DC
  - Diff and CM RL
  - Jitter (DJ, RJ, DCD/EOJ)
- PAM4 TX
  - SNR
  - Nonlinearity (level separation mismatch ratio, RLM)



$$S_{min} = \frac{min(V_D - V_C, V_C - V_B, V_B - V_A)}{2} \quad \text{(a)}$$

$$V_{avg} = \frac{V_A + V_B + V_C + V_D}{4} \quad \text{(b)}$$

$$ES_1 = \frac{V_B - V_{avg}}{V_A - V_{avg}} \quad \text{(c)}$$

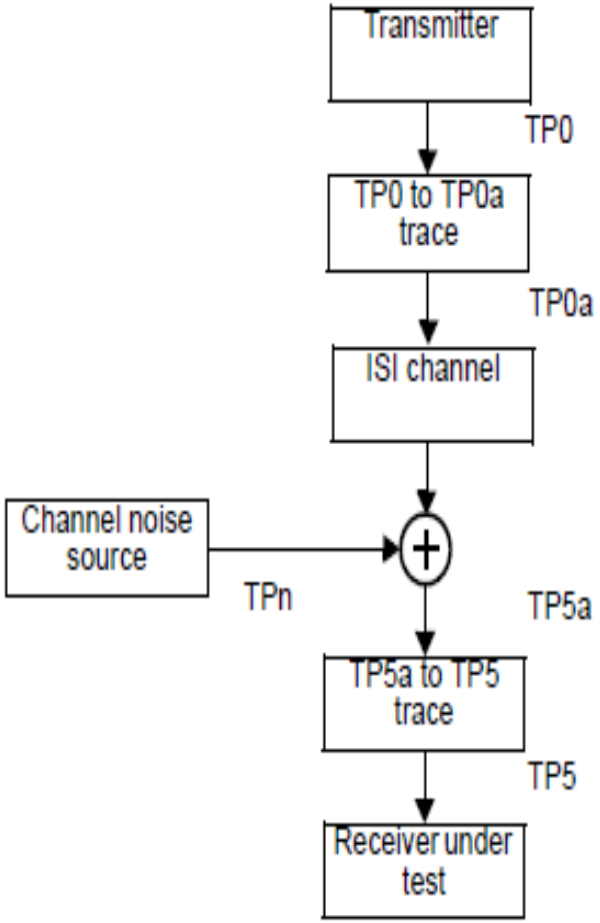
$$ES_2 = \frac{V_C - V_{avg}}{V_D - V_{avg}} \quad \text{(d)}$$

$$R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A} \quad \text{(e)}$$

Note: RLM test method is subject to further improvement and be aligned with new changes in CDAUI-8 c2c

CEI-56G-LR-PAM4 Test Parameters/Methodology:RX

- Three major subtests
  - Diff RL and Diff-to-CM RL
  - Interference tolerance
    - Input with worst TX + worst channel, multiple test conditions
    - Calibration is done with COM
  - Jitter tolerance



II. Leveraging and Benefits

Summary for CEI-56G-LR-PAM4 Spec Characteristics

- Complete spec draft (no TBDs) has been around since Nov/2015 and has gone through two comment/resolution cycles
- Spec bears many similarities to 25GE BP (clause 94, PAM4) and CDAUI-8 C2C in terms of parameters, specification, and test methodologies
- Spec is subject to further change and improvement

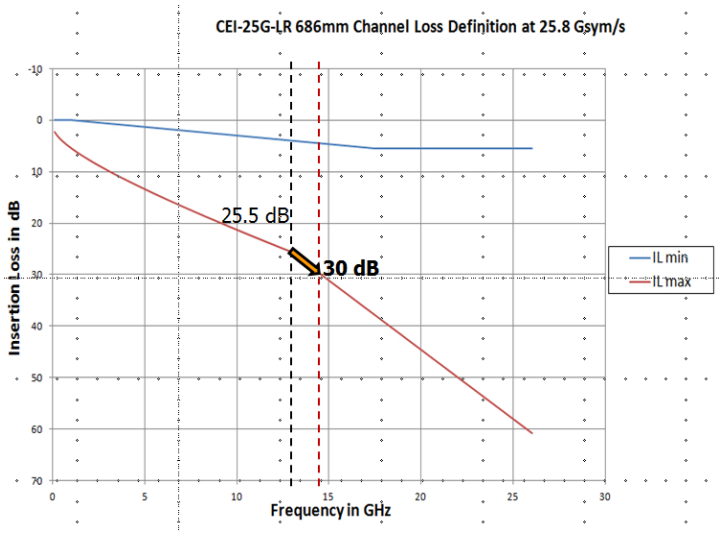
Benefits of Leveraging

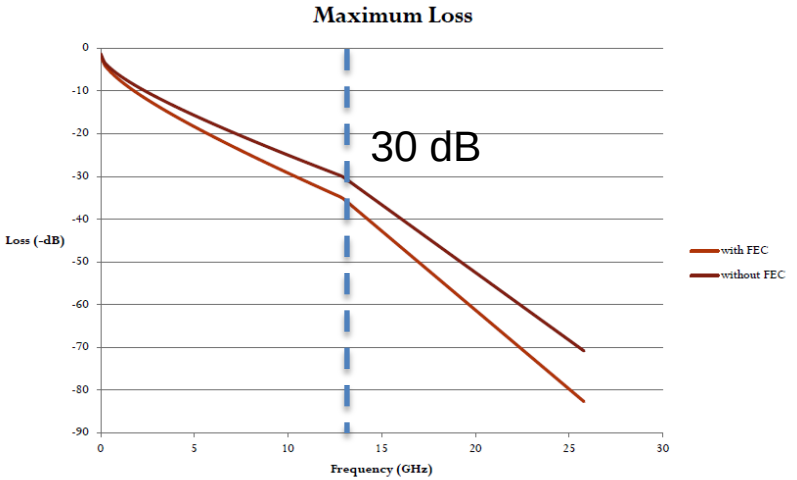
- Reuse the industry investments on CEI-56G-LR-PAM4 for better efficiency of the 50GE BP development
- Appropriate alignment in spec and test methodology will enable efficient product development and manufacture for vendors play in both Ethernet and OTN markets

III. A Path Forward

IL Target Increase Requests

- OIF2016.026.00/ALU suggests to increase the IL target at Nyquist from the current 25.5 dB to 30 dB due to the symbol rate increase in order to be backward compatible with CEI-25G-LR channels
- Cisco suggests IL of ~32 dB would meet the system requirement for 50G Ethernet backplane and cable assembly



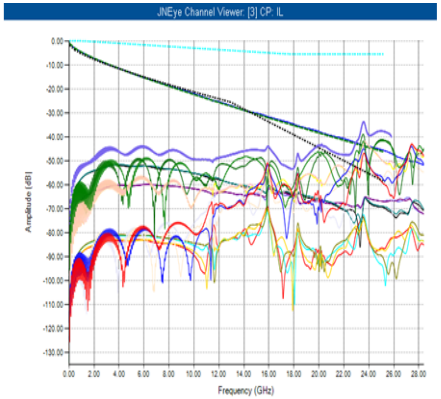


Cel-25G-LR-NRZ IL_max limit

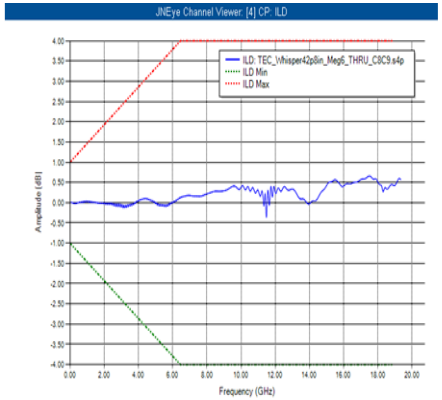
25G Ethernet BP/CA IL_max limit (informative)

A 30 dB BP Channel Study

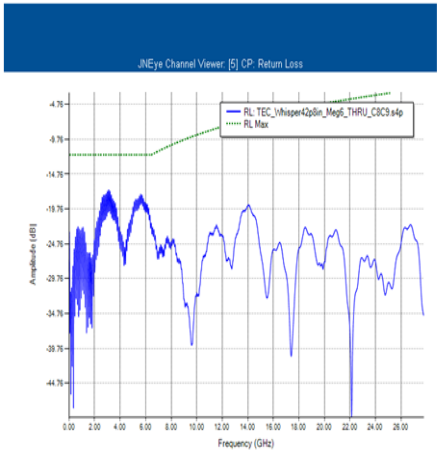
Insertion Loss



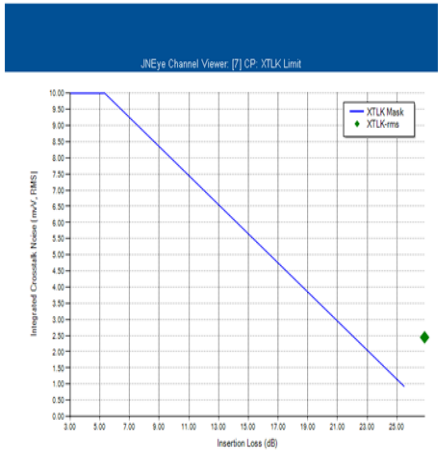
ILD



Return Loss



XTLK Limit



- Channel B: IL ~ 30 dB at Nyquist
- ILD, RL, comply with CEI-25G-LR, but ICN exceeds the limit

Simulation Results

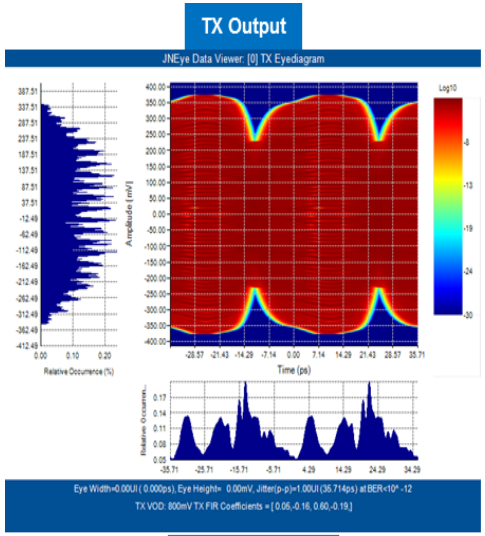
- TX assumptions
  - Largely similar to

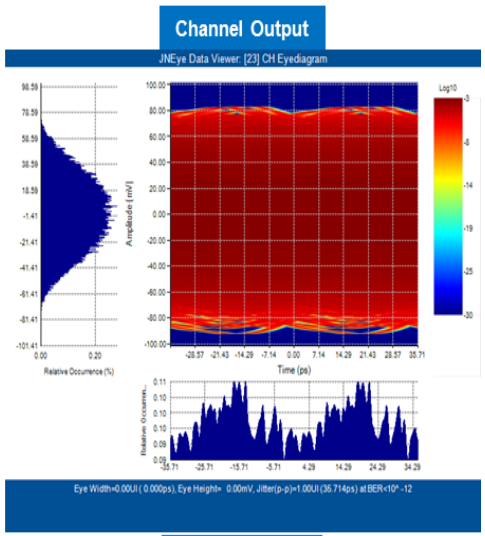
  CEI-56G-LR-PAM4 COM, except that

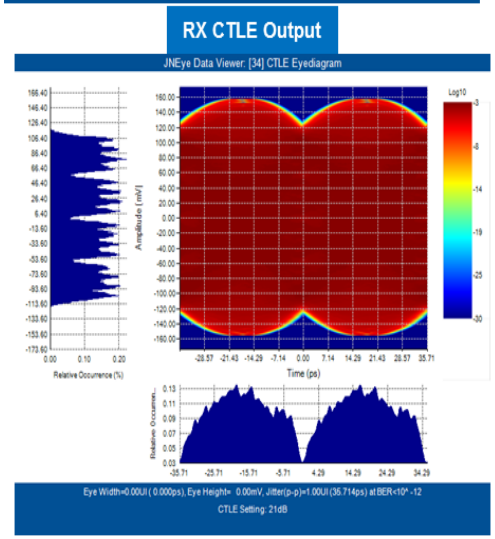
  actual package is used
- RX assumptions
  - Largely similar to

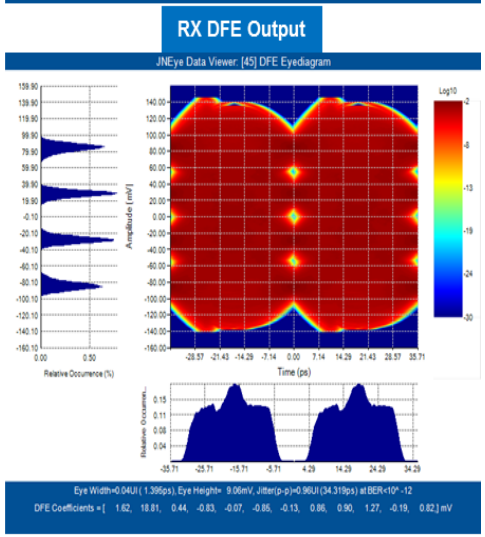
  CEI-56G-LR-PAM4 COM, except that

  actual package is used









DFE Output
BER 1e-15: EW = 0.017 UI, EH = 5 mV
BER 1e-4: EW = 0.16 UI, EH = 17 mV

The Tracking/Alignment Between CEI-56G-LR-PAM4 and 50GE BP

- If 50G SG would adopt the 30 dB IL as its objective, some parameters in the current 56G-LR-PAM4 spec draft will likely be changed/improved to meet the new IL objective, consequently
  - CEI-56G-LR-PAM4 loss objective will likely to increase from the current 25.5 dB to 30 dB at Nyquist
  - It would be good to keep future 50GE BP spec and CEI-56G-LR-PAM4 spec tracked/aligned

IV. Summary and Closing Remarks

Summary

- CEI-56G-LR-PAM4 project started in 2014 and the current spec draft has gone through two comment/resolution cycles
- Leveraging CEI-56G-LR-PAM4 specification will enable
  - 50 GE spec project development efficiency
  - cost effective product development crossing both Ethernet and OTN markets
- If 30 dB IL objective would be adopted for the 50 GE backplane
  - CEI-56G-LR-PAM4 objective and spec will likely to be changed and aligned
  - It is desirable have CEI-56G-LR-PAM4 spec and 50 GE BP spec be tracked and aligned moving forward