# PoDL Feasibility for B10GAUTO Systems

Gitesh Bhagwat



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# Background



- Preliminary discussion on <u>objectives</u> for B10GAUTO group considers:
  - 25Gbps data rate and Symmetrical and Asymmetrical max data rate operation
- Further points to be discussed:
  - The asymmetry ratio and method for implementing
  - PHY modulation schemes, transmit voltage, link length etc.

# **Power Coupling Network Considerations**

- Power coupling circuity is in shunt with data path
- Inductors, in particular, impact Return Loss
  - Low frequency Return Loss is limited by Open Circuit Inductance (OCL)
  - High frequency Return Loss is limited by Parasitic Capacitance (SRF)
- Broadband Return Loss requires cascaded inductors
  - Increased size, component count, complexity



# Sample Single Inductor Topology



Able to meet the MDI Return Loss requirement for 1000Mbps, 2,5Gbps, 5Gbps and 10Gbps symmetric data rate SPE systems

	max. DCR	max. Area	Isat (A) 30%	Irms (A)
Inductors	(ohms)	(mm²)	125 °C	125 °C
1205POC-103 (10 μH)	1	4.48	0.41	0.30 (15°C rise)





Source: https://www.coilcraft.com/pdfs/1205POC.pdf

#### **Sample Cascaded Inductors**

	max. DCR	max. Area	Isat (A) 30%	Irms (A)	
Inductors	(ohms)	(mm²)	125 °C	125 °C	Notes
LPS4018-104 (100 µH)	1.4	15.8	0.31	0.43 (40°C rise)	$2.6 \ k\Omega$ resistor in parallel
1205POC-682 (6.8 μH)	0.41	4.48	0.52	0.46 (15°C rise)	$3.6 \ k\Omega$ resistor in parallel
PFL1005-181 (180 nH)	0.21	0.724	0.97	0.66 (15°C rise)	
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Note: This solution is for a single-ended output



CON1 CON2 VNA VNA 0-Input Output  $C1 = 0.1 \, \mu F$ L1 L = 180 nH PFL1005-181 L2 00 L = 180 nH 00 PFL1005-181 R1 L3R=3.6 k $\Omega$   $\lesssim$  L=6.8  $\mu$ H 1205POC-682  $\begin{array}{c|c} R2 & L4 \\ R = 2.61 \text{ k}\Omega & L = 100 \text{ }\mu\text{H} \end{array}$ LPS4018-104 -11-C2 = 10 µF 내  $C3 = 0.1 \ \mu F$ CON3 DC Power Input Q **Schematic** 

ANALOG DEVICES

Source: Coilcraft (Kurt Smith)

#### Comparison



- Current capacity 0.3A for single inductor as well as cascaded combination
- The following comparison is made based on a differential power coupling network
- For speeds above say 5.6 Gigabaud (802.3ch), the single inductor solution may require an additional series chip inductor per leg to improve high frequency performance

Coupling Network	Total DCR (max)	Total max Area (mm <sup>2</sup> )
Single Inductor per output		
2 X 1205POC-103 (10 μH)	2 ohms	8.96
Cascaded Inductors	4.46 ohms	43.46

# **Increasing Power with Higher Voltage**

- Current capacity limited (by the coupling network for example)
- DCR losses (I<sup>2</sup>R losses) also related to current
- Delivered power can be increased by increasing the transmission voltage
- Example with 0.3 A current limit:
  - Assume 6.5 ohms DC loop resistance and max 30% power loss to ensure stability margin
  - Power loss = MIN (power loss in DC loop resistance, 30% of transmitted power)
  - Delivered power = (Transmitted power power loss)

Transmit Voltage -V <sub>PSE(min)</sub> (V)	Current Limit (A)	DC Loop Resistance (ohms)	Power Delivered (W)
5.6	0.3	6.5	1.176
11.7	0.3	6.5	2.925
14.4	0.3	6.5	3.735
26	0.3	6.5	7.215
48	0.3	6.5	13.815

# **Transmitting with Higher Voltage**



- A single step up/down converter at the PSE and individual step down converters at PDs
  - Step down at PD already required in most applications



Integrated, highly efficient, robust, wide voltage buck, boost and buck-boost converters can be used to step up/ down the transmission voltage

## **Questions for the Task Force**

- PoDL coupling network feasibility will be determined by the following:
- Desired Asymmetry ratio
- Modulation scheme
- Method of implementing asymmetry:
  - Separate forward (high speed) and reverse (low speed) channels?
  - Low Power Idle (LPI) mode?
  - Combination of these?
- Impact on permissible MDI Return Loss





# Thank You!

Questions? Feedback?