Considerations on 200G per lane PAM Signaling

YUCHUN(Louis) LU, Yan Zhuang, Huawei Technologies

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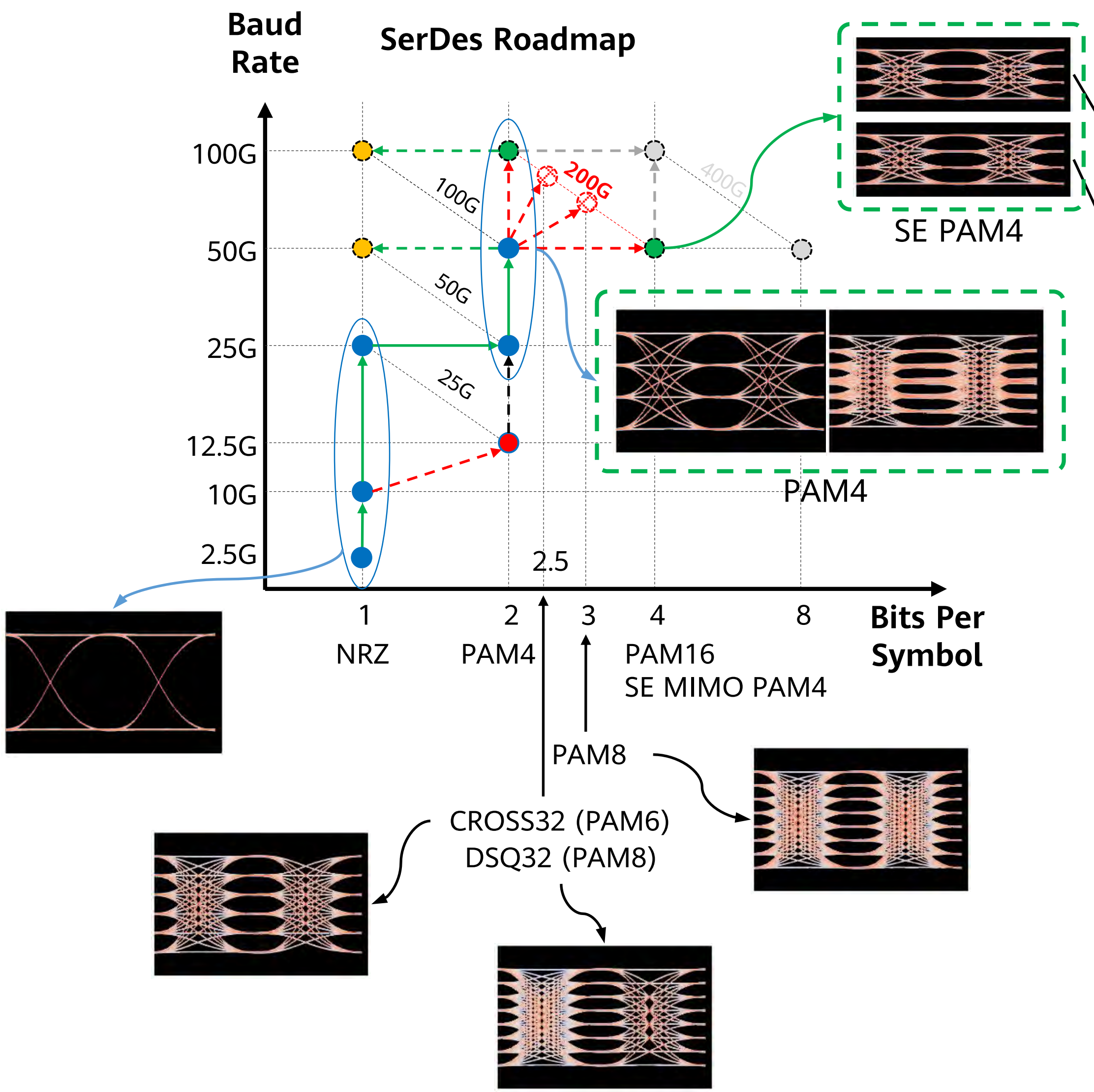
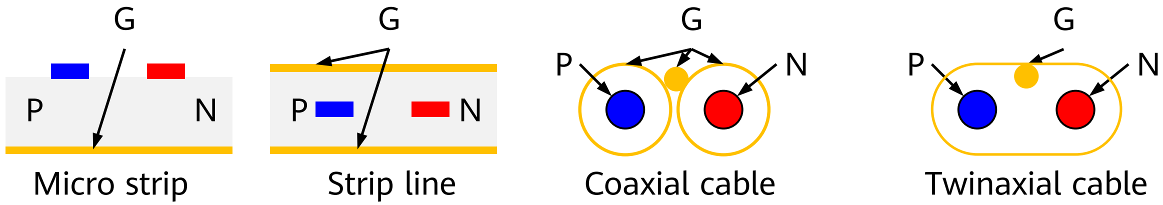
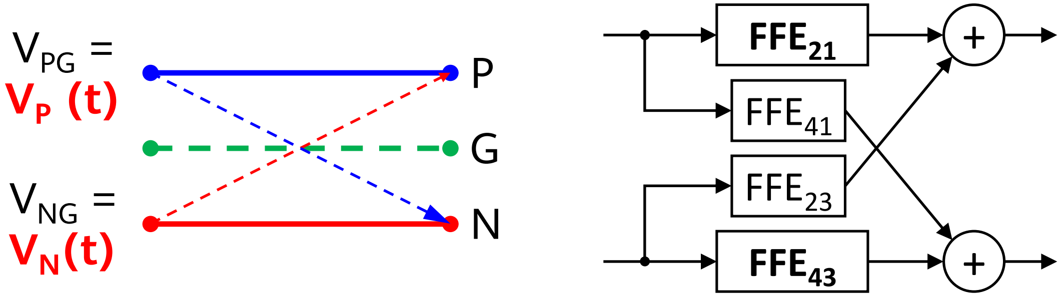
Requirements of Beyond 100Gbps Links

- Line speed:
  - **212.5Gbps** per differential pair (electrical) / lambda (optical).
  - Electrical link:
    - Die-to-die, in/near-package-optics, host-to-CDR, chip-to-module.
    - Chip-to-chip, mid-plane/backplane.
  - Optical link: 100m, 500m, 2km, 10km, ….
- Power efficiency: 3~6pJ/bit → 2~3pJ/bit (C2Optics, C2M, C2C, KR/CR).
- Compatible with 100G and slower speed links.
- FEC Gain & Latency:
  - RS(544, 514) as reference:
    - NCG ~= 7dB (BERin=2e-4); ~100ns@100G, <100ns@200G.
  - Stronger FEC target (If it is necessary.):
    - NCG = 8.0~9.0dB (BERin ~= 1e-3); latency<120ns@100G.

Roadmap for Beyond 100G SerDes

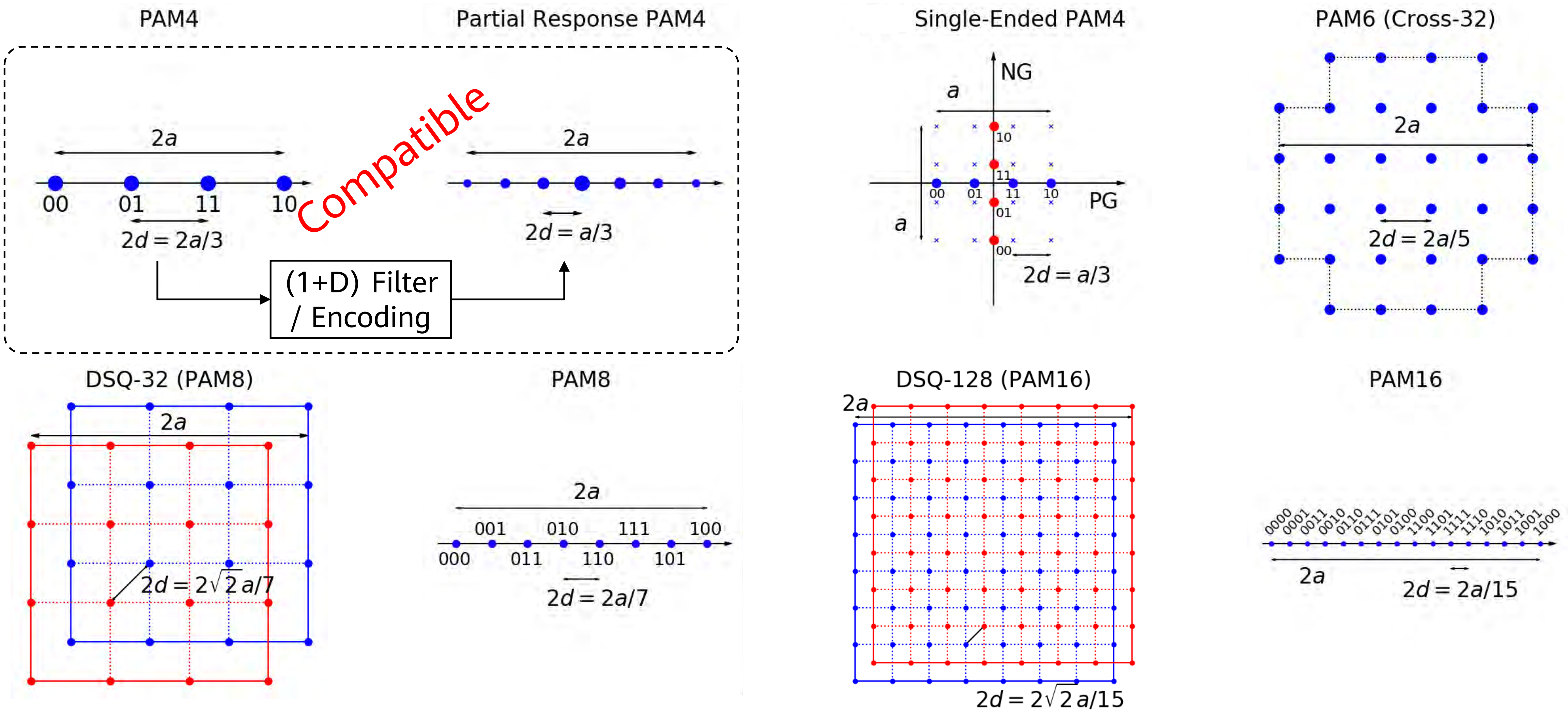






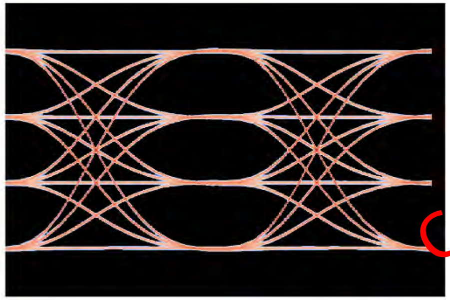
- From NRZ to PAM4, the data rate is doubled with baud rate unchanged. The SNR loss is compensated by RS(544, 514) FEC.
- "Cheat sheet" of upgrading from PAM4 to PAM16 does not work, because the SNR loss is too high and FEC is less cost-effective.
- One possible way to double the data rate of differential pairs and keep the baud rate unchanged is to use single-ended (SE) signaling. The intra-pair crosstalk can be easily canceled by MIMO algorithm which is mature.
- 200G optical links still need 100GBd PAM4, because optical links are native "single-ended" system.

200G PAM Signaling Constellations



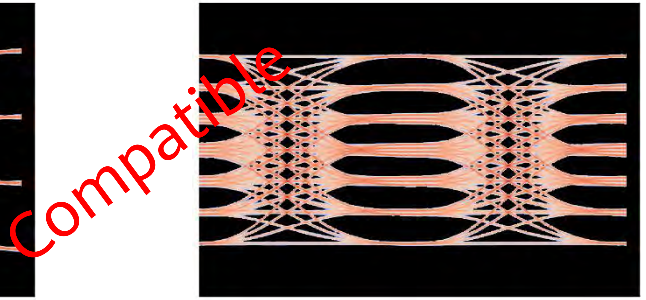
200G PAM Signaling Eye Diagrams

PAM4



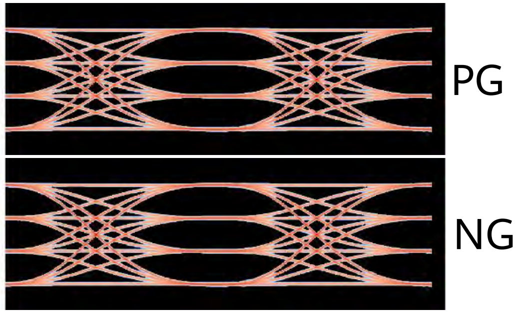
Baudrate: 106.25GBd
Nyquist: 53.125GHz
Bandwidth: 80GHz

Partial Response PAM4



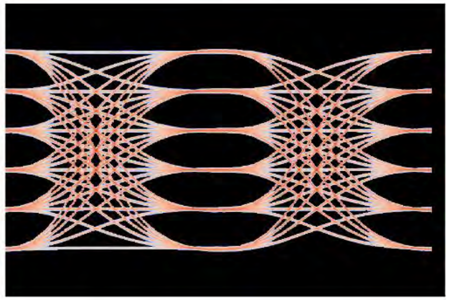
Baudrate: 106.25GBd
Nyquist: 26.5625GHz?
Bandwidth: 40GHz?

Single-Ended PAM4



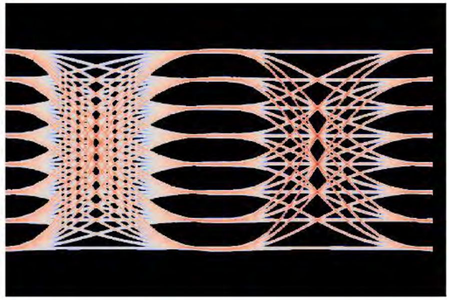
Baudrate: 53.125GBd
Nyquist: 26.5625GHz
Bandwidth: 40GHz

CROSS-32 (PAM6)



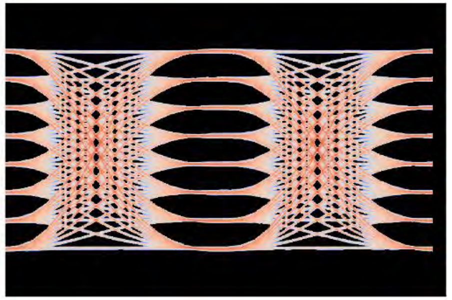
Baudrate: 85GBd
Nyquist: 42.5GHz
Bandwidth: 64GHz

DSQ-32 (PAM8)



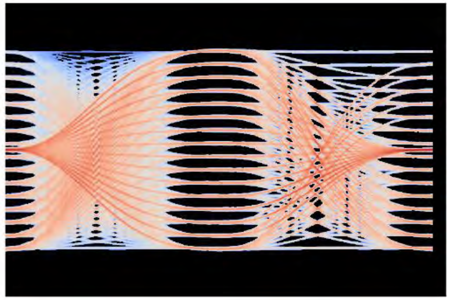
Baudrate: 85GBd
Nyquist: 42.5GHz
Bandwidth: 64GHz

PAM8



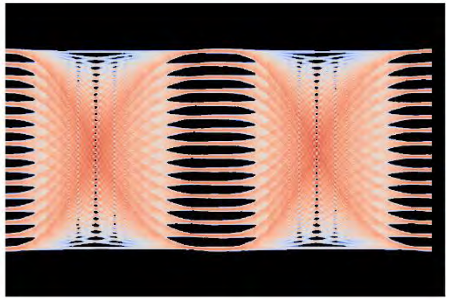
Baudrate: 70.83GBd
Nyquist: 35.42GHz
Bandwidth: 53GHz

DSQ-128 (PAM16)



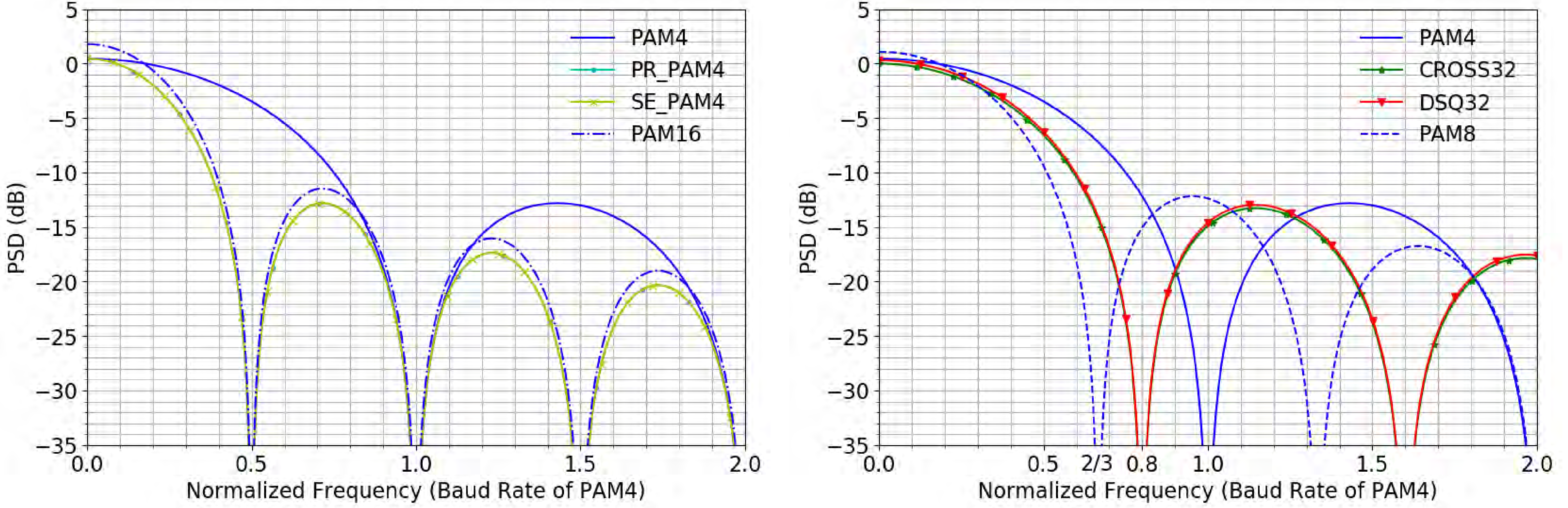
Baudrate: 61.71GBd
Nyquist: 30.36GHz
Bandwidth: 46GHz

PAM16



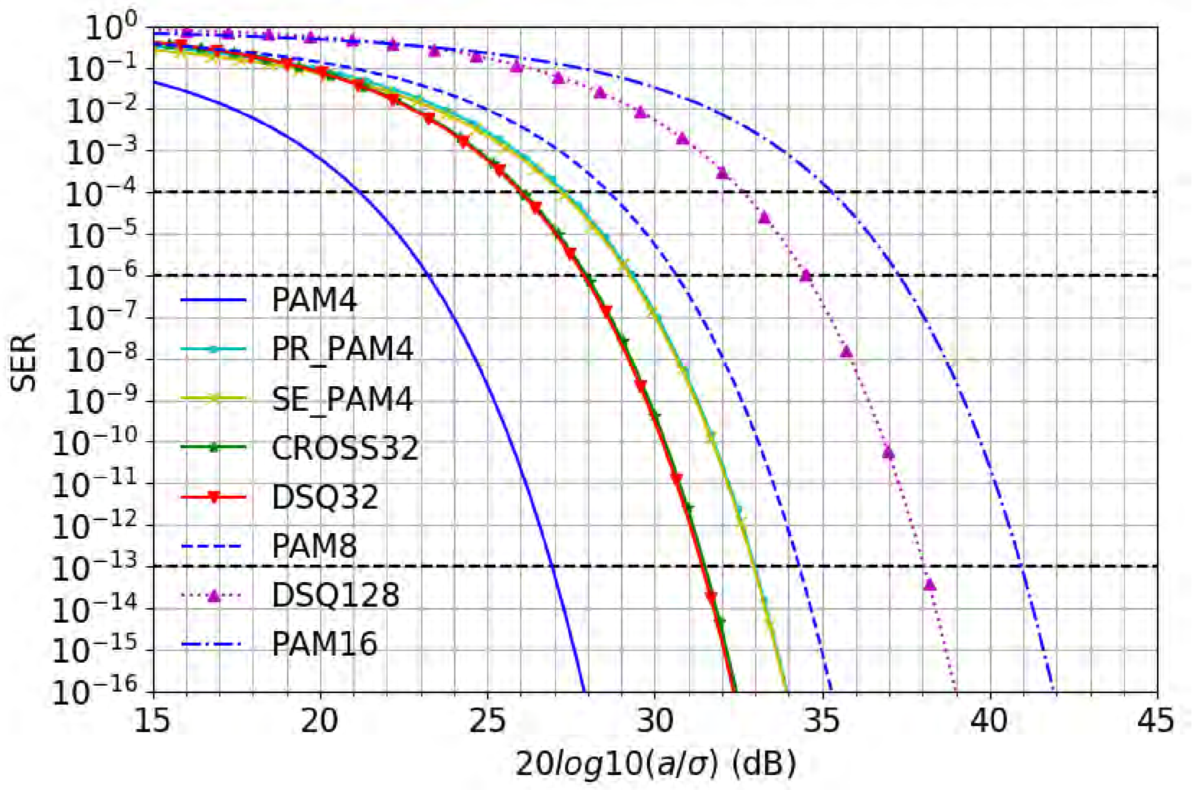
Baudrate: 53.125GBd
Nyquist: 26.5625GHz
Bandwidth: 40GHz

PAM Signaling Power Spectrum Density



- PR-PAM4 and SE-PAM4 and PAM16 has similar PSD. The bandwidth requirement is about half of PAM4.
- CROSS32 (PAM6) and DSQ32 (PAM8) has similar PSD, bandwidth requirement is between PAM8 and PAM16.

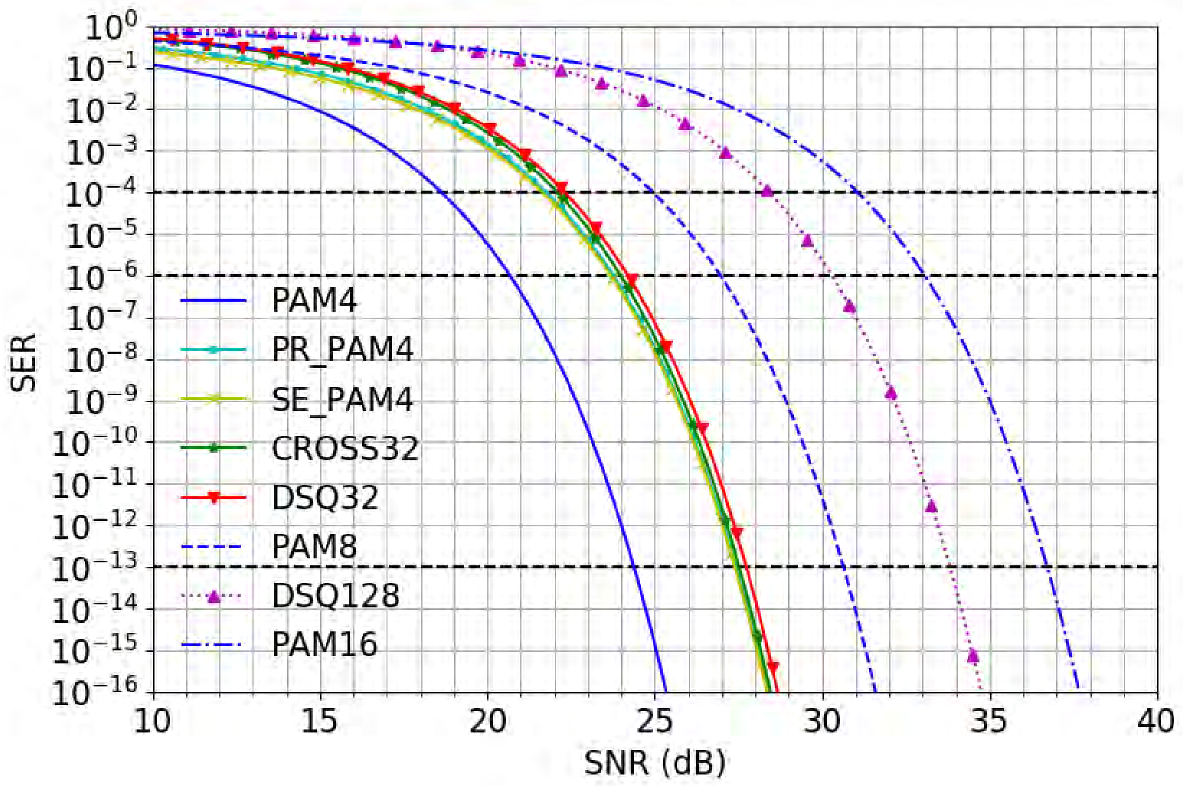
Amplitude-to-Noise Ratio versus SER



	1.00E-04		1.00E-06		1E-13	
	SNR (dB)	SNR Penalty (dB)	SNR (dB)	SNR Penalty (dB)	SNR	SNR Penalty (dB)
PAM4	21.18	0.00	23.23	0.00	26.93	0.00
PR_PAM4	27.33	6.14	29.33	6.10	32.99	6.06
SE_PAM4	27.20	6.02	29.25	6.02	32.95	6.02
CROSS32	26.07	4.89	27.96	4.73	31.50	4.57
DSQ32	25.99	4.81	27.88	4.65	31.41	4.48
PAM8	28.63	7.45	30.64	7.41	34.31	7.38
DSQ128	32.64	11.46	34.52	11.29	38.04	11.11
PAM16	35.29	14.10	37.29	14.06	40.94	14.01

- Assume no crosstalk noises exist, but only signal power independent noises
  - Does not scale with the signal power.
  - Thermal noise, quantization noise, …
- **Insertion loss needs to be reduced.**
  - **Should be normalized @ Nyquist Frequency.**

Signal-to-Noise Ratio versus SER



	1.00E-04		1.00E-06		1E-13	
	SNR (dB)	SNR Penalty (dB)	SNR (dB)	SNR Penalty (dB)	SNR	SNR Penalty (dB)
PAM4	18.63	0.00	20.68	0.00	24.38	0.00
PR_PAM4	21.77	3.13	23.77	3.09	27.42	3.04
SE_PAM4	21.64	3.01	23.69	3.01	27.39	3.01
CROSS32	22.09	3.46	23.98	3.30	27.52	3.14
DSQ32	22.31	3.68	24.20	3.52	27.73	3.35
PAM8	24.95	6.32	26.96	6.29	30.63	6.26
DSQ128	28.41	9.78	30.29	9.61	33.81	9.44
PAM16	31.06	12.43	33.06	12.38	36.72	12.34

- Assume no signal power independent noises exist, but only crosstalk noises
  - Scaled with the signal power.
- **Crosstalk needs to be reduced.**
  - **Should be normalized with signal bandwidth.**

200G PAM Signaling Comparison

Bandwidth limited

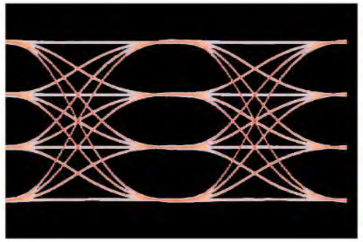
Bandwidth limited

Jitter limited

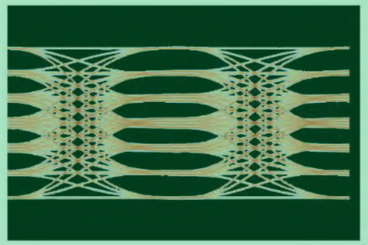
Modulation		Symbol Rate (GBaud)	Unit Interval (ps)	Nyquist Frequency (GHz)	Bandwidth Requirements ** (GHz)	Bits per Symbol	# of Levels	Penalty @SER=1e-4 (Amplitude Normalized)	Penalty @SER=1e-4 (Power Normalized)
PAM4	Regular	106.25	9.4	53.125	80	2/1	4	0.00 @53GHz	0.00 @106GHz
	PR	106.25	9.4	26.5625*	40*	2/1	7	6.14 @26GHz*	3.13 @53GHz
	SE	53.125	18.82	26.5625	40	4/1	4 (x2)	6.02 @26GHz	3.01 @53GHz
PAM6	CROSS-32	85	11.76	42.5	64	5/2	6	4.89 @43GHz	3.46 @85GHz
PAM8	DSQ-32	85	11.76	42.5	64	5/2	8	4.81 @43GHz	3.68 @85GHz
	Regular	70.83	14.12	35.42	53	3/1	8	7.45 @35GHz	6.32 @71GHz

* Estimated as 1 / 4 of Baud Rate. ** frequency range with smooth IL or small ILD.

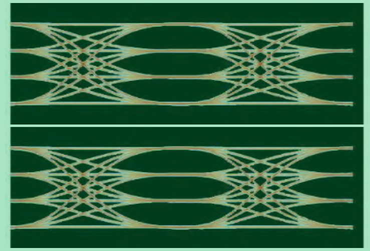
SNR limited



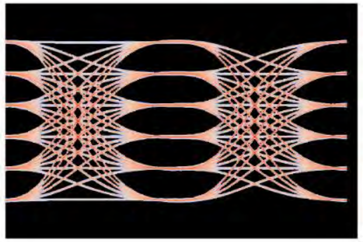
PAM4



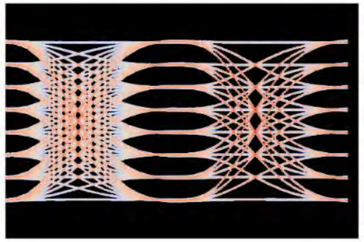
PR PAM4



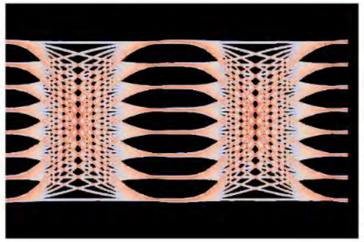
SE PAM4



CROSS-32 (PAM6)



DSQ-32 (PAM8)



PAM8

Summary and Discussion

- Provide the technical feasibility of 200Gbps per lane electrical links.
  - Analyzed PAM signaling schemes for beyond 100G links and their penalties compared with standard PAM4.

- With SE/PR-PAM4, there is a chance to implement 200G KR/CR even with certain 100G PAM4 channels, as well as C2C, C2M and C2Optics interfaces. It may provide an elegant way to upgrade electrical interfaces from 100G to 200G.

- Selection of the PAM signaling scheme highly depends on the channel quality. More channel impairments and design boundaries need to be closely explored in the Task Force.

Channel impairments need to be addressed …

- Insertion Loss, Crosstalk (covered by Salz-SNR model)
  - The first barrier we need to conquer. It is a good “kick-off”, but not the end.

- Jitter, impendence discontinuities & reflection, residue ISI, nonlinearity, etc. (further covered by COM or IBIS-AMI model)
  - These effects may be dominant and overturn conclusions about “feasibility”.

- Multi-mode interference (MII) effect should be closely considered, it will introduce ISI that cannot be equalized.
  - It is difficult to achieve "single mode" operation in larger than 50GHz frequency range, unless the "waveguide” size is greatly reduced.
  - MMI introduces **“Fast roll-off” / “Notches”** for beyond 40GHz range.
  - MMI may happen in or between any “discontinuities” along the channel: Bump, Ball, Via, Stub, mating plane of connectors, etc.

More work in Task Force…

- Investigate design boundaries for **end-to-end** channels in a system level, including packages, PCB, cable, and connectors. Assumptions about specific points may affect the overall feasibility (Bucket effect / Short board effect). (Related to **channel quality**.)
- Analyze and compare the performance of different PAM signaling schemes with real channels. The transceiver architecture should be considered, e.g. FFE / DFE / MLSE / MIMO. Analyze the complexity and cost of transceivers, including gate count, power, latency, etc. (Related to the **signal processing**.)
- Analyze the possibility of leverage existing error correction architecture, or introduce a new one. (Related to the **FEC coding**.)

Thanks!
Q&A