On the Technical Feasibility of 200G/Lane Chip-to-Module

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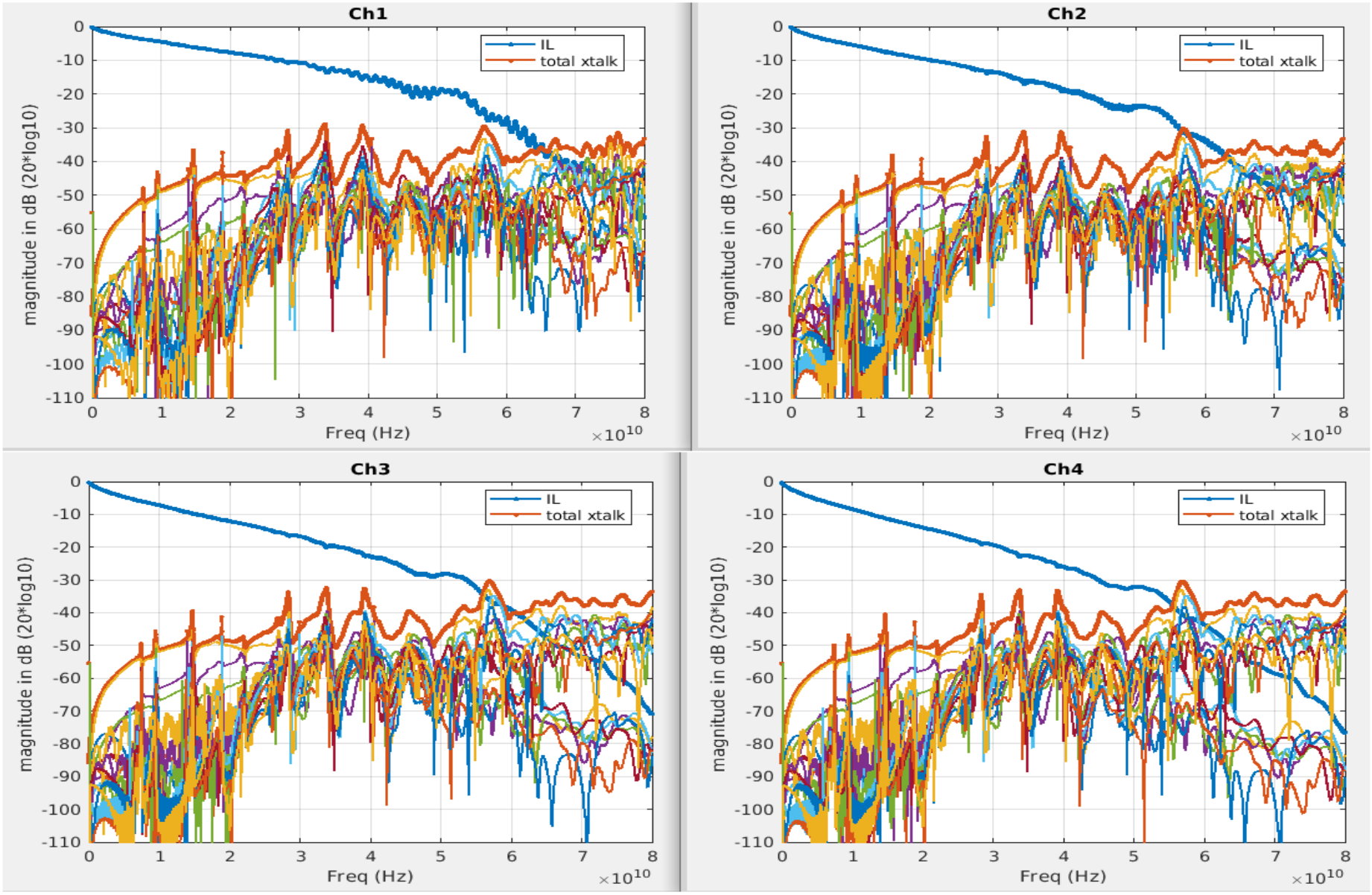
Summary

- C2M Channel Models
- FEC Assumptions and Model
- PAM4 and PAM6 Theoretical Bound Results
- PAM4 and PAM6 Time Domain Simulations
- Conclusions and Future Work

Chip-to-Module Channel Models

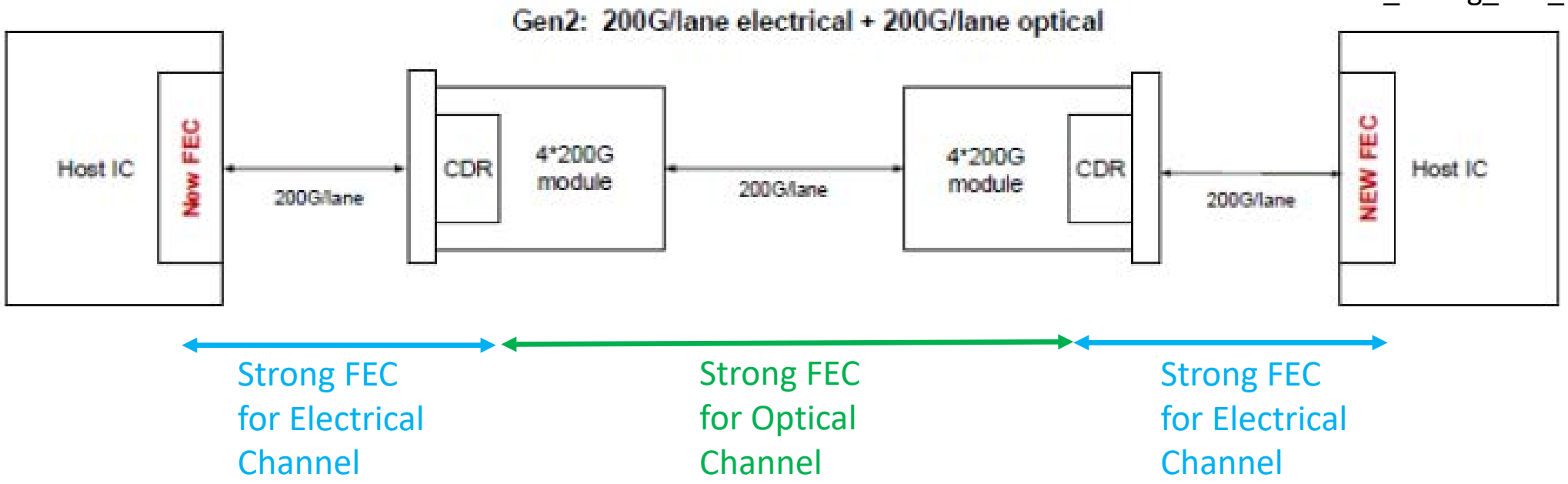
- Including switch pkg/bga break out, trace, OSFP connector, and module break out
- Nvidia simulations based on real components



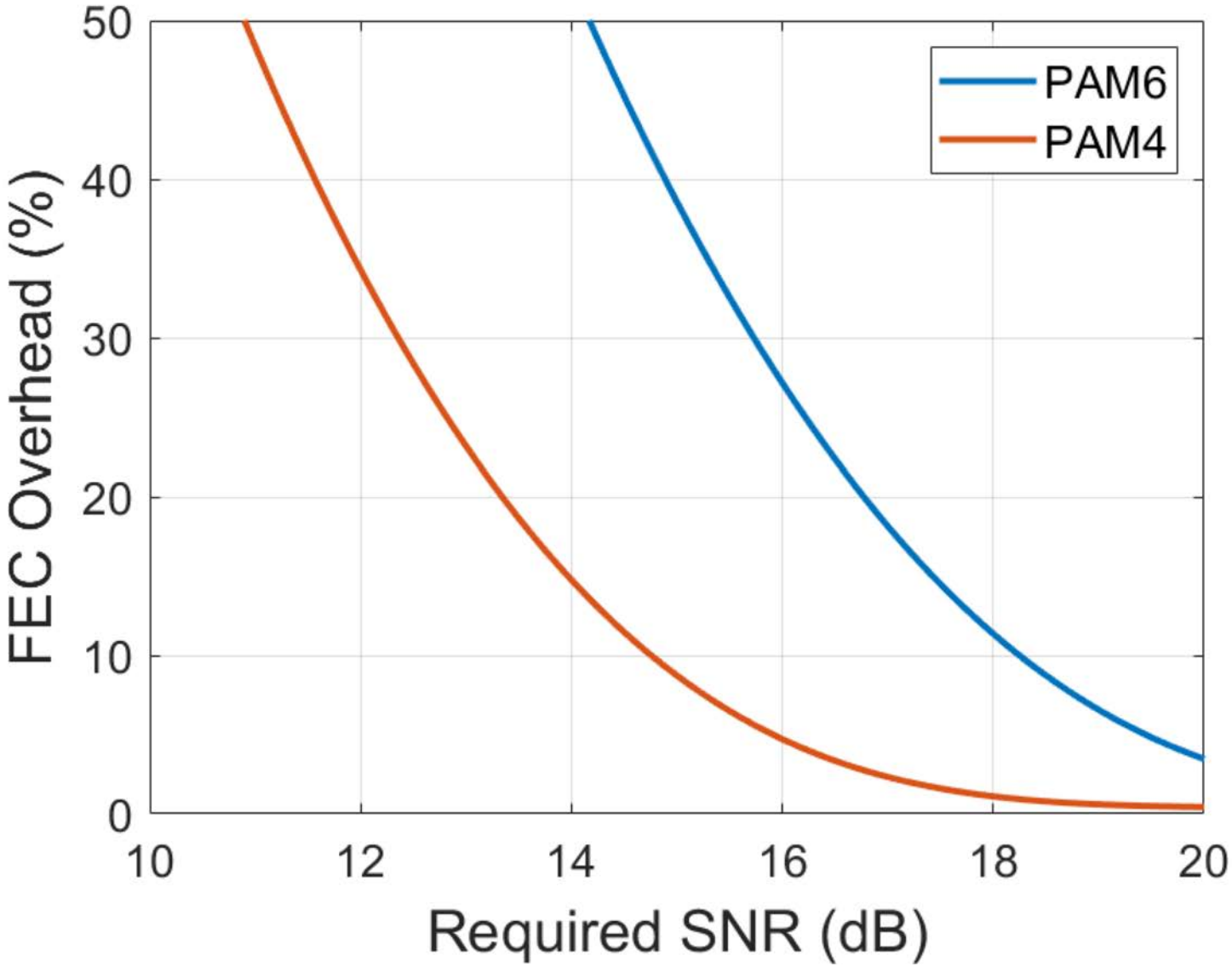
FEC Assumptions

- For 200G per lane, the electrical channel is very challenging, IL ~ 30 dB with high cross talk
- Optical channel is similarly challenging requiring strong FEC, see recent ISSCC presentation I. Lyubomirsky, “DSP and FEC Architectures for Beyond 400Gb/s Data Center Interconnects,” ISSCC, Forum, Feb. 2021
- Segmented FEC architecture allows to de-couple electrical and optical channels to enable optimum design/performance on each segment; we adopt this approach to simplify initial technical feasibility analysis

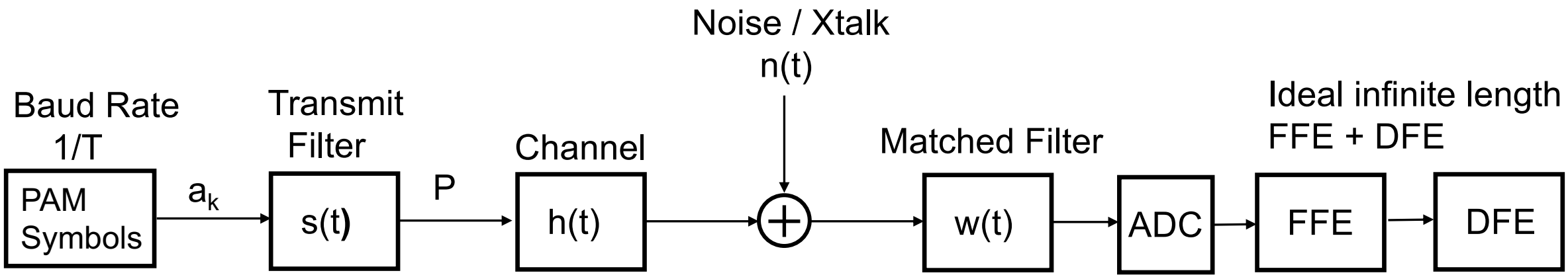
Source: bruckman_b400g_01a_210211



Shannon Limit for HD FEC with 1 dB Implementation Margin



System Model for Salz SNR Bound

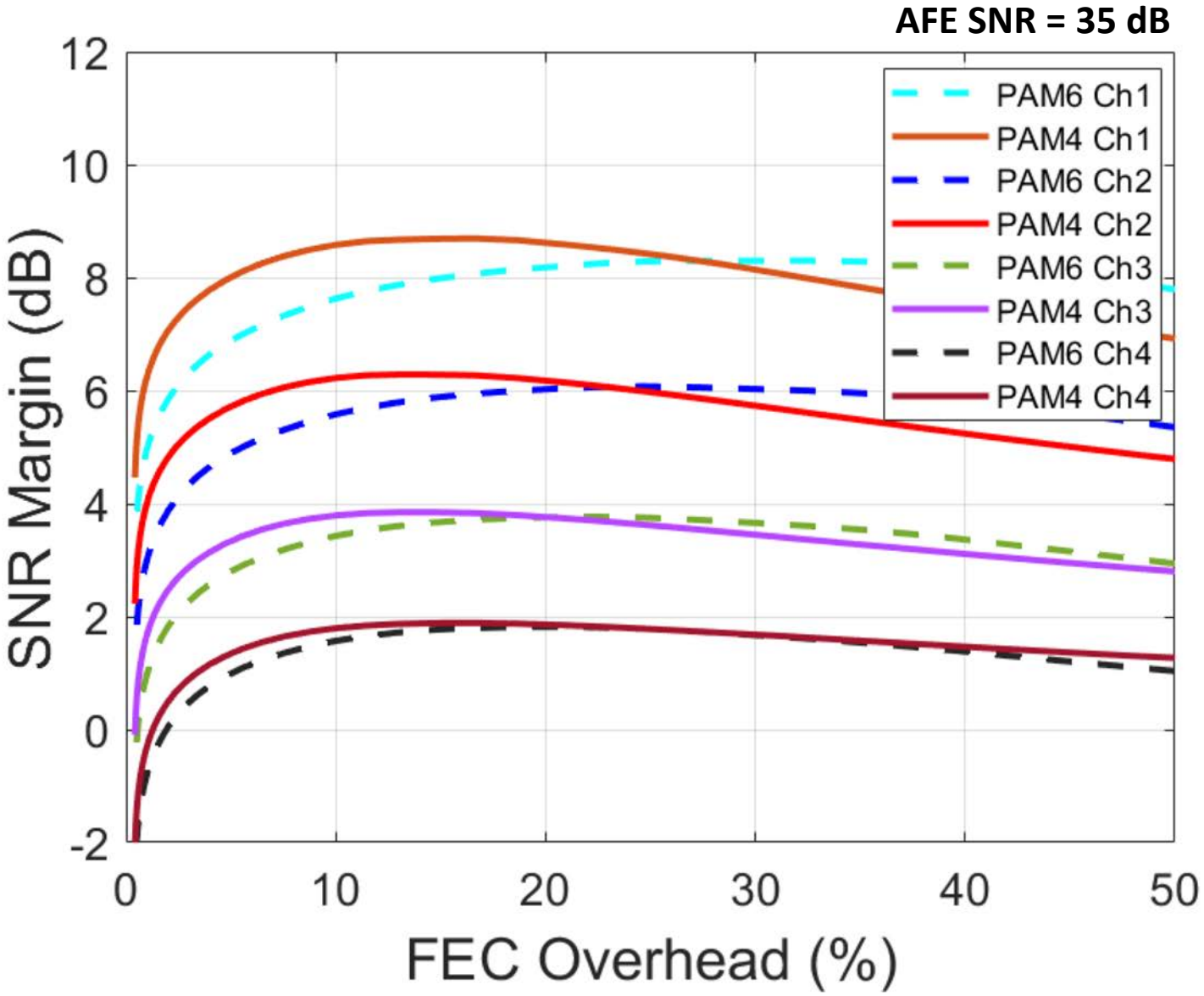


$$SNR = e^{\left[2T\int_0^{\frac{1}{2T}} \ln(Y(f)+1)df\right]} = e^{\frac{1}{f_{NY}}\int_0^{f_{NY}} \ln(Y(f)+1)df}$$

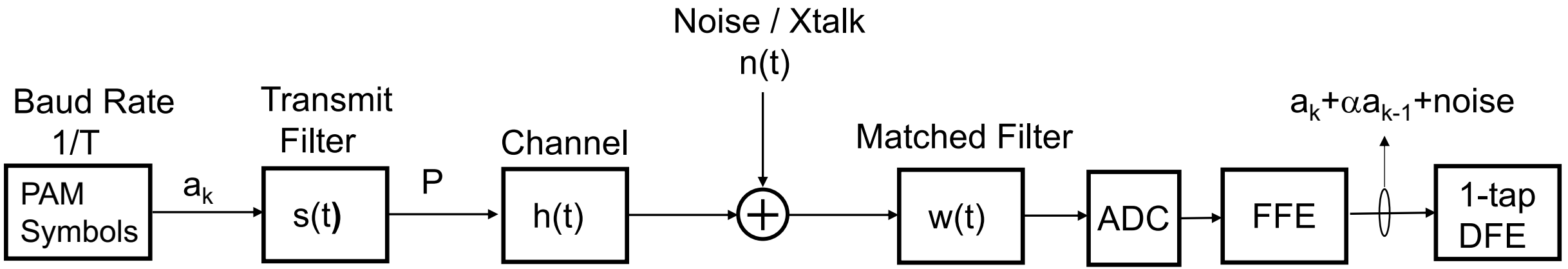
$$Y(f) = \frac{P(f)}{N(f)}|H(f)|^2$$

P(f) = signal power spectral density
N(f) = noise power spectral density
Note when N(f) is due to Xtalk, then Y(f)=ICR(f)

SNR Margin vs. FEC Overhead: Salz Theoretical Bound



System Model for FFE+1-tap DFE SNR Bound

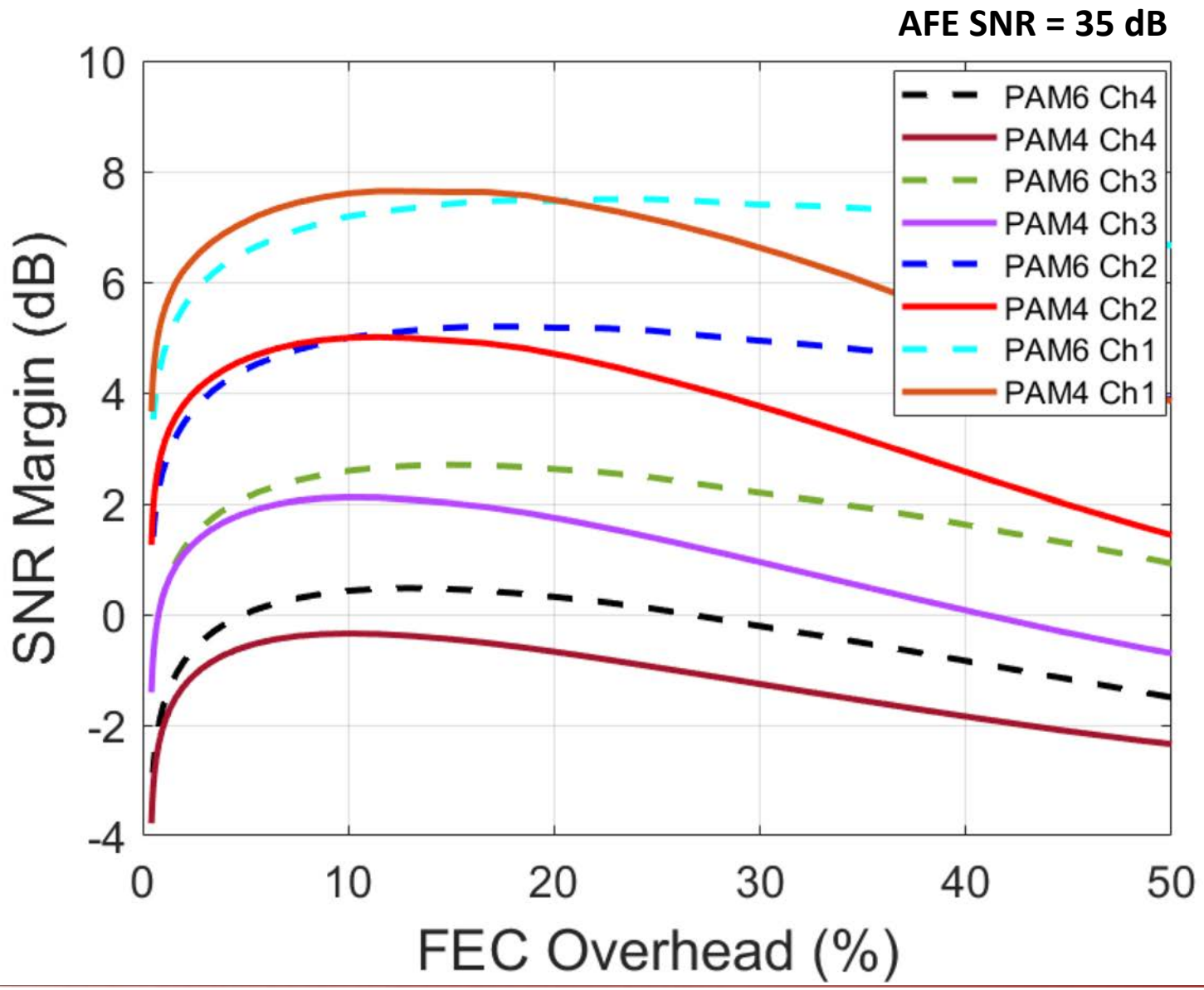


- Infinite length FFE with target response g(D)= 1+αD
- Optimized α for PAM4 and PAM6
- 1-tap DFE to cancel first post cursor tap

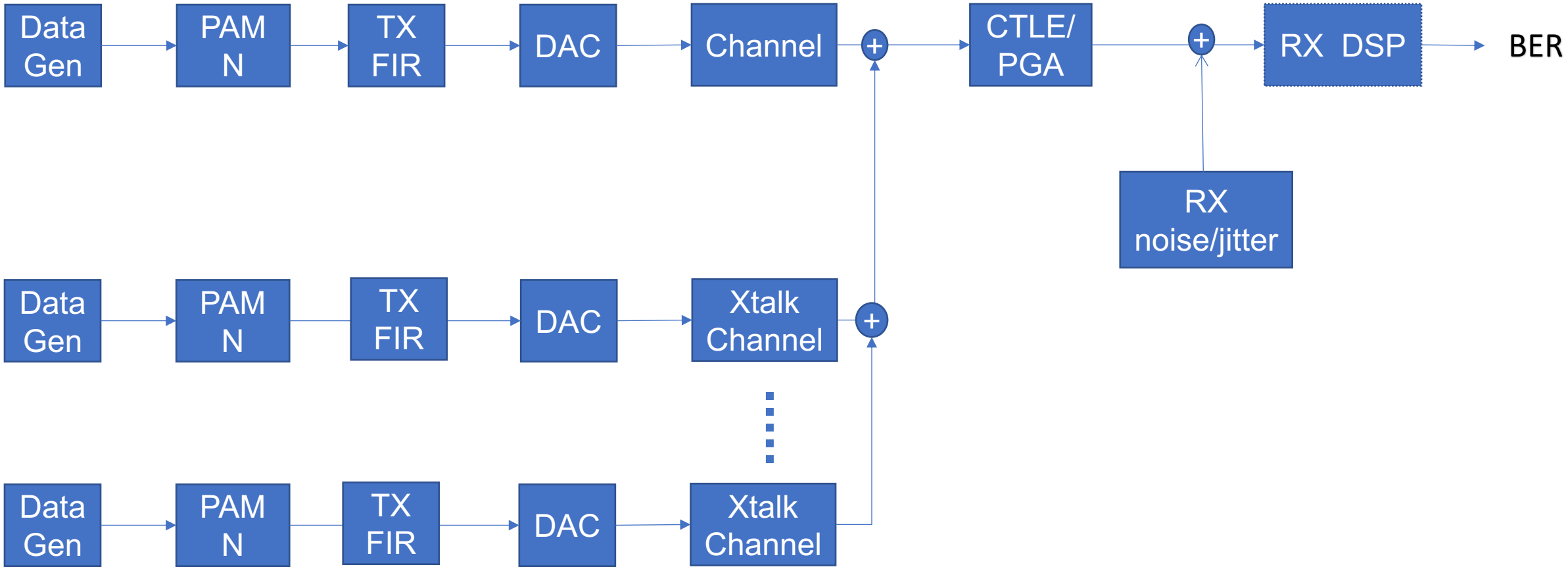
$$SNR = \frac{1}{\frac{1}{f_{NY}}\int_0^{f_{NY}} \frac{|G(f)|^2}{Y(f)+1}\,df}$$

Reference: Jan W. M. Bergmans, “Digital Baseband Transmission and Recording,” Kluwer Academic Publishers, 1996

SNR Margin vs FEC Overhead: FFE+1-tap DFE Theoretical Bound



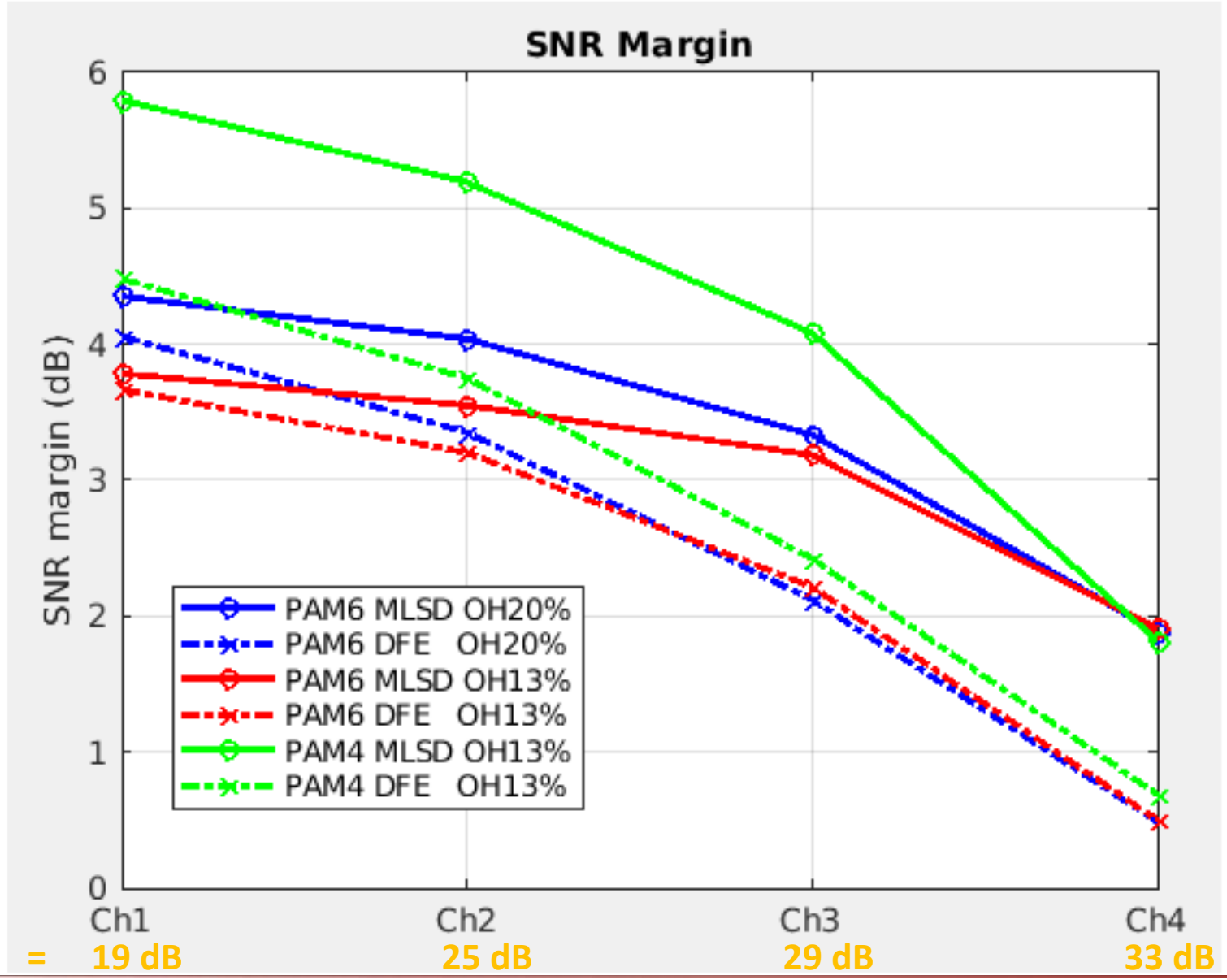
Time Domain Simulator



Simulation Parameters

- Channels:
  - Four bump-to-bump electrical channels for chip-to-module (see slide 4)
  - Simulated channels included switch package/brake out, trace loss, and OSFP connector/break out
- Equalization Schemes
  - Tx FIR with 6 dB boosting
  - Rx 30-tap FFE + 1-tap DFE
  - Rx 30-tap FFE + MLSD
- Baud rate and FEC
  - FEC OH = 13.3%, BER Limit 8e-3
    PAM4 Baud rate 113.3 GBd
    PAM6 Baud rate = 90.7 GBd
  - FEC OH = 20%, BER Limit =1.45e-2
    PAM6 Baud Rate = 96 GBd
- Realistic components and parameters are included in the simulation model.
  - DAC, CTLE/PGA, jitter, etc
- RX AFE noise included and scaled according to baud rate

Time Domain Simulation Results



IL (@53GHz) = 19 dB 25 dB 29 dB 33 dB

Conclusions and Future Work

- Theoretical bounds and time domain simulations indicate 200G/Lane PAM is feasible with stronger FEC on channels IL(53GHz) < 30 dB
- Channels with higher IL may be feasible with improvements in channel cross talk, AFE noise, and stronger MLSD equalization
- The optimum HD FEC overhead for PAM4 is in the range ~ 10-16%, while PAM6 prefers a higher FEC overhead ~ 16-22%
- Future work to consider additional C2M channel models, stronger Tx/Rx equalization, specific FEC implementations, and feasibility of end-to-end FEC
- Encourage working toward approval of 200G/Lane chip-to-module objective