FEC Architecture of B400GbE to Support BER Objective

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Previous Discussions – BER Objective Straw Polls

Straw Poll #4 - BER

For the following proposed objective in support of 800 Gb/s operation, I would support the following – Support a BER of better than or equal to _____ at the MAC/PLS service interface (or the frame loss ratio equivalent)	Results
a) 10^{-13}	42
b) 10^{-14}	26
c) 10^{-15}	4
d) Better than 10^{-15}	2
e) Need more information	10
f) Abstain	7

Straw Poll #5 BER

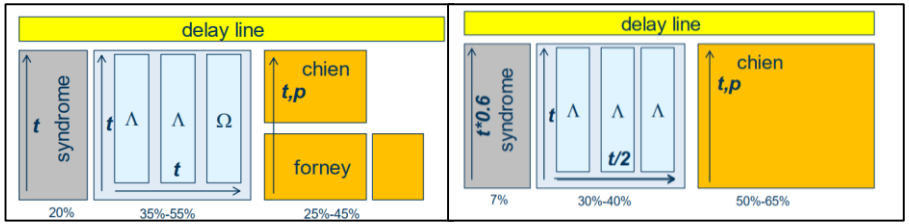
For the following proposed objective in support of 1.6 Tb/s operation,, I would support the following – Support a BER of better than or equal to _____ at the MAC/PLS service interface (or the frame loss ratio equivalent)	Results
a) 10^{-13}	13
b) 10^{-14}	26
c) 10^{-15}	2
d) Better than 10^{-15}	0
e) Need more information	38
f) Abstain	6

https://www.ieee802.org/3/B400G/public/21_04/motions_b400g_2104.pdf

- Concerns on 1E-13 objective: too many errors per hour/minute.
- Concerns on 1E-14 objective: may introduce huge cost due to stronger FEC.
- This contribution tries to answer the following questions:
  - What is the cost in terms of area and latency for Soft-Decision BCH?
  - How much improvement do we need for pre-FEC BER in order to get to 1E-14?
  - How shall we perform error marking to ensure MTTFPA for concatenated FEC?

Method Used to Analyze FEC Coding Gain, Area and Latency

- FEC coding gain can be evaluated by code rate, pre-FEC BER and post-FEC BER.
- FEC area and latency model used in 802.3bs:



RS FEC BCH FEC

langhammer_3bs_01_1114

$t_{syndrome}$ = n/p1, p1=16 for KR4/KP4 FEC implementation in this slides

t_{KES} = x2t, (if $t_{KES} > t_{syndrome}$, duplicate KES in this slides)

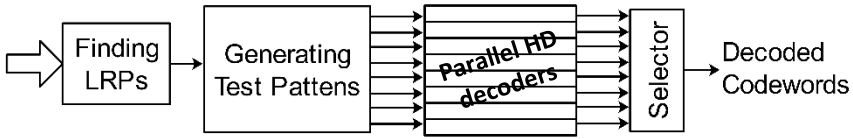
x=1 for t<=15, x=2 for t>15; For longer RS FEC, level of pipelining in the iterative calculation may increase due to longer critical path

$t_{chien} + t_{forney}$ = n/p2+1, p2=66/68 for KR4/KP4 FEC implementation in this slides, p2≥p1

FEC Decode Latency = ~($t_{syndrome} + t_{KES} + t_{chien} + t_{forney}$)

wang_x_3bs_01a_0115

- Soft-decision decoding FEC is an enhancement technique in a FEC decoder to improve coding gain, which **does not affect the interoperability since it does not alter the content in the codewords**.
- SD decoder usually has multiple HD decoders implemented, with additional logic for sorting and calculations.



A Simplified view of a SD decoder

Latency and Area Estimation of Different FEC Codes

FEC code		Operating rate	Latency[1], ns	Relative Area
Hard Decision RS	2-way RS(544,514)	850G	51.2	~4.00
	2-way RS(544,514)	212.5G	89.6	1.00 (Synthesized, 7nm)
	Single RS(576,514)	900G	70.4	~7.60
	Single RS(576,514)	225G	89.6	1.90 (Synthesized, 7nm)
Hard Decision BCH	BCH(144,136)	225G	1.6	0.003
	BCH(180,170)		1.6	0.004
	BCH(360,340)		2.4	0.013 (Synthesized, 7nm)
	BCH(720,680)		4.8	0.042
Soft Decision BCH (LRP = 6)[2]	BCH(144,136)	225G	9.6	0.17
	BCH(180,170)		9.6	0.22
	BCH(360,340)		11.2	0.51 (Synthesized, 7nm)
	BCH(720,680)		15.2	1.36

1: Latency is evaluated based on 1.25 GHz clock frequency (0.8 ns per cycle).
2: Latency and/or area will go higher along with the performance if more LRP is selected. All simulations in the following slides are based on LPR = 6.

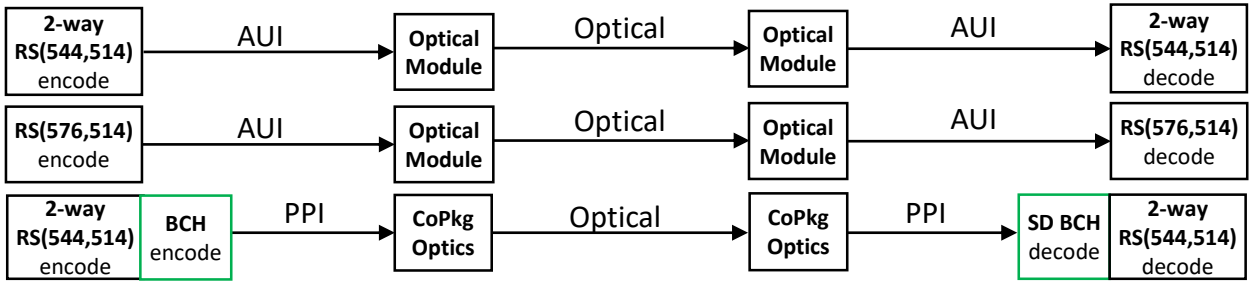
Examples of Different FEC Architectures Considered

1. End-to-end FEC

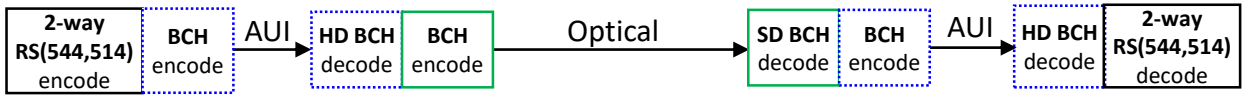
1-1. 2-way RS(544,514)

1-2. RS(576,514)

1-3. RS(544,514) + SD BCH concatenated FEC



2. Encapsulated concatenated FEC

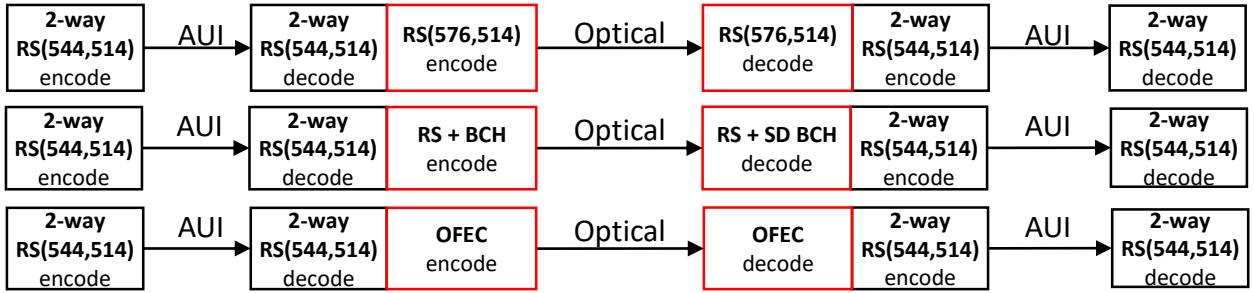


3. Segmented FEC

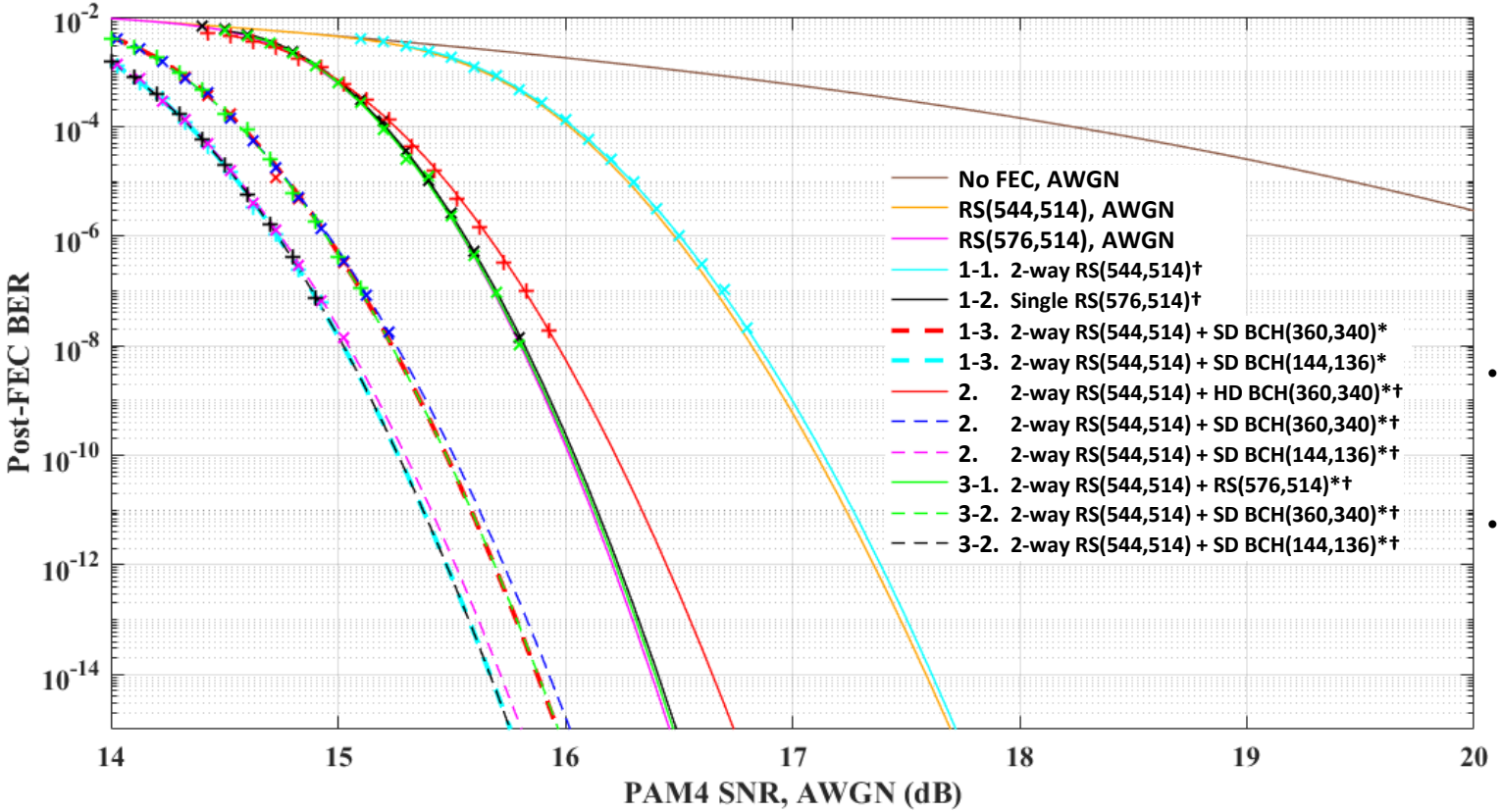
3-1. RS(576,514)

3-2. RS(544,514) + SD BCH concatenated FEC

3-3. OpenFEC (OFEC)

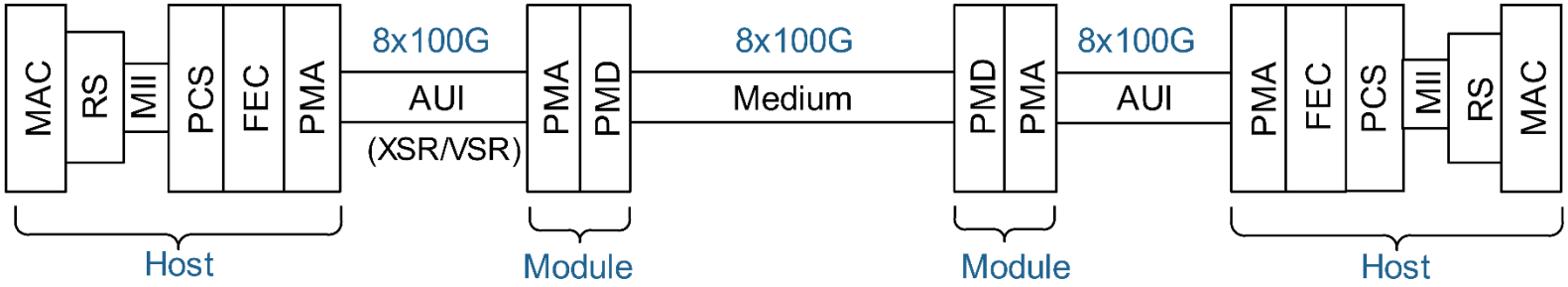


Performance Overview of Different FECs



- Curves marked with "*" are extrapolated from simulated data.
- Curves marked with "†" considered the AUI BER of **4E-5, including** the additional errors due to bursts.

1-1. **End-to-End FEC – 2-way RS(544,514)** for 100G/lane Optical & Electrical Interfaces

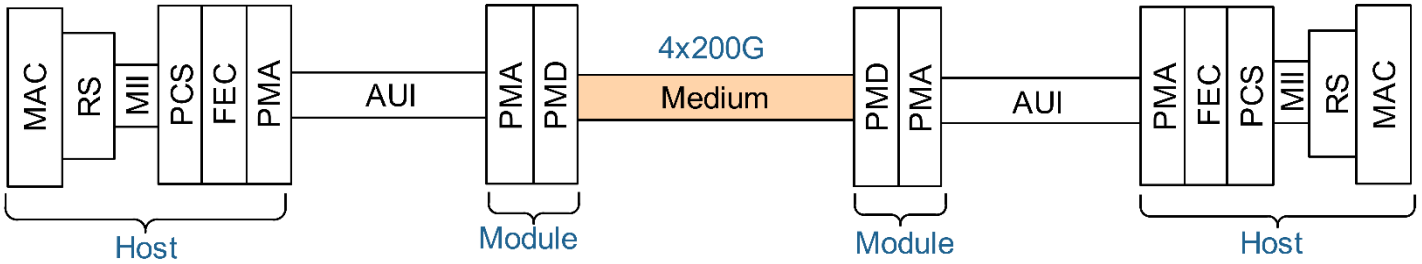


- E2E 100G/lane can be supported by E2E 2-way interleaved RS(544,514) FEC.
  - Both **1E-13** and **1E-14** BER objectives can be met with today's optical (802.3cu) and C2M(802.3ck) spec.
  - Breakout to 8x100 GbE and 2x400 GbE can be supported.

FEC	Optical BER	Post-FEC BER*	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate
2-way RS(544,514)	2.2E-4	1.1E-15	51.2 ns	YES	YES	8x106.25 Gb/s	
2-way RS(544,514)	2.4E-4	4.1E-15		YES	YES		

*Please refer to wang_b400g_01a_210315 for the two-part link model used in this evaluation.
All simulations in this contribution assume the AUI BER is **4E-5, including** the additional errors due to bursts, unless specified otherwise.

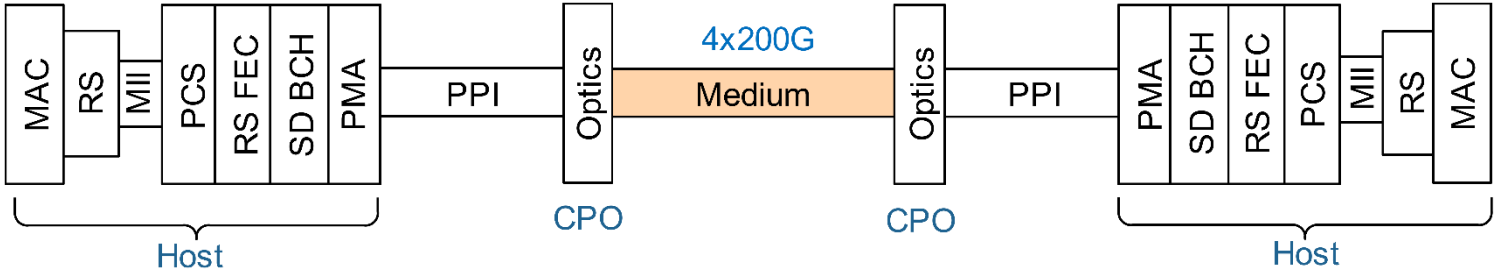
1-2. **End-to-End FEC – Single RS(576,514)** for 200G/lane Optical Interfaces



- 200G/lane optics require stronger FEC than the 2-way interleaved RS(544,514), e.g. RS(576,514).
  - Both **1E-13** and **1E-14** BER objectives could be met if optical BER is 1.1E-3 and AUI BER is 1E-5.
  - **112.5 or 225 Gb/s C2M spec is incompatible with 802.3ck @106.25 Gb/s.**
- If upgrading AUI to 225 Gb/s per lane, more analysis is needed wrt burst length, power, loss, etc.

FEC	Optical BER	Post-FEC BER	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate
RS(576,514)	1.1E-3	7.9E-15	70.4 ns	YES	YES	8x112.5 Gb/s Or 4x225 Gb/s	
RS(576,514)	1.2E-3	5.9E-14		YES	NO		
RS(576,514)	1.3E-3	1.8E-13		NO	NO		

1-3. **End-to-End Concatenated FEC – RS + SD BCH** for 200G/lane CPO

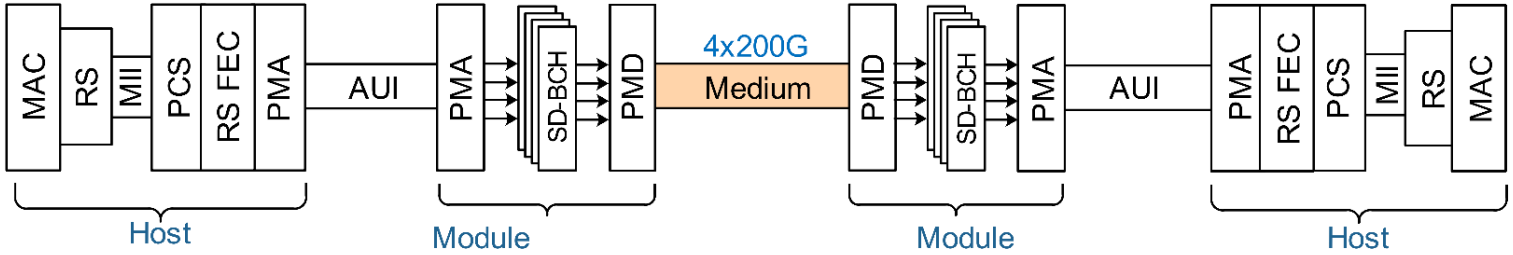


- E2E concatenated FEC with inner soft-decision BCH can be used when using PPI or “Direct Drive”.
  - Both **1E-13** and **1E-14** BER objectives can be met with up to 2.4E-3 optical raw BER.
- Can be interoperable with FPP modules in example 2 on the next slide.

FEC	Optical BER	Post-FEC BER*	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate
2-way RS(544,514) + SD BCH(360,340)	2.0E-3	7.3E-15	51.2+11.2 = 62.4 ns	YES	YES	8x112.5 Gb/s Or 4x225 Gb/s	
2-way RS(544,514) + SD BCH(144,136)	2.4E-3	4.5E-15	51.2+9.6 = 60.8 ns	YES	YES		

* Assuming inter-sub layer electrical interface BER <1E-6.

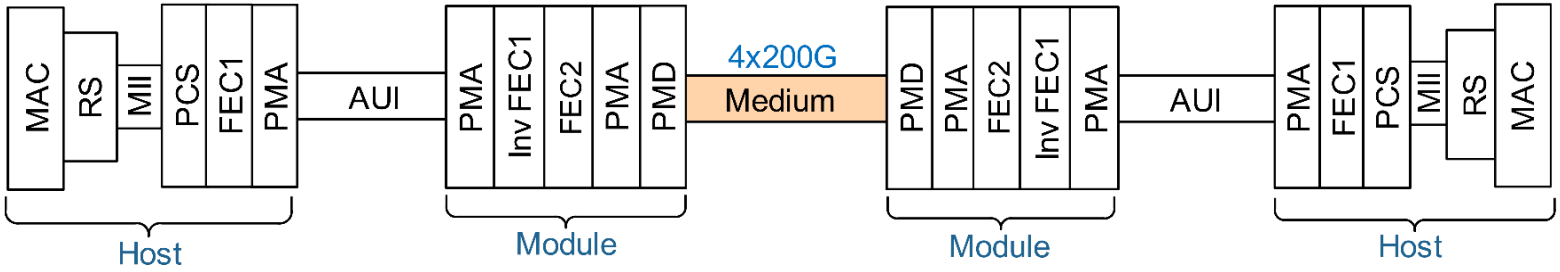
2. **Encapsulated Concatenated FEC – RS + SD BCH** for 200G/lane Optical Interfaces



- 200G optical lanes are protected by both inner and outer codes, AUI is covered by outer code only.
  - Both **1E-13** and **1E-14** BER objective could be met with up to 2.3E-3 optical raw BER.
  - **C2M data rate can be compatible with 802.3ck @106.25 Gb/s.**

FEC	Optical BER	Post-FEC BER	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate
2-way RS(544,514) + HD BCH(360,340)	1.0E-3	1.0E-13	51.2+2.4 = 53.6 ns	YES	NO	8x106.25 Gb/s or 4x212.5 Gb/s	4x225 Gb/s
2-way RS(544,514) + SD BCH(360,340)	1.9E-3	7.3E-15	51.2+11.2 = 62.4 ns	YES	YES		
2-way RS(544,514) + SD BCH(144,136)	2.3E-3	4.6E-15	51.2+9.6 = 60.8 ns	YES	YES		

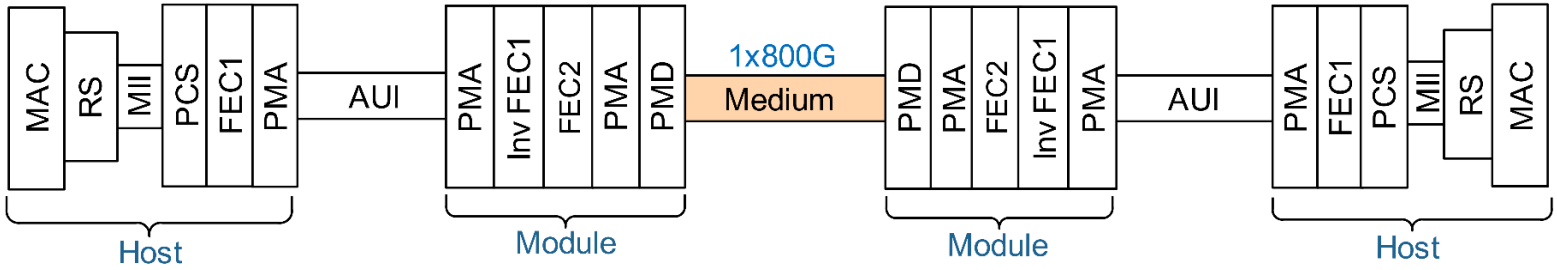
3-1 & 3-2. **Segmented FEC – RS or RS + SD BCH** for 200G/lane Optical Interfaces



- AUI has dedicated FEC protection, which may allow relaxation on AUI spec.
  - Both **1E-13** and **1E-14** BER objectives could be met with up to 2.4E-3 optical raw BER.
  - Making FEC3 and FEC1 the same means simpler design for host devices.

FEC1 & FEC3	FEC2	Optical BER	Post-FEC BER	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate
2-way RS(544,514)	RS(576,514)	1.1E-3	1.7E-15	51.2+70.4+51.2 = 172.8 ns	YES	YES	8x106.25 Gb/s or 4x212.5 Gb/s	4x225 Gb/s
2-way RS(544,514)	RS(576,514)	1.2E-3	1.6E-14		YES	NO		
2-way RS(544,514)	2-way RS(544,514) + SD BCH(360,340)	2.0E-3	1.0E-14	51.2+(51.2+11.2)+51.2 = 164.8 ns	YES	YES		
2-way RS(544,514)	2-way RS(544,514) + SD BCH(144,136)	2.4E-3	4.5E-15	51.2+(51.2+9.6)+51.2 = 163.2 ns	YES	YES		

3-3. **Segmented FEC – OFEC** for Coherent Optical Interfaces



- Suitable for applications where FEC latency is less sensitive, e.g. 10km+ where fiber latency dominates.
  - Both **1E-13** and **1E-14** BER objectives could be met with up to 1.95E-2 optical raw BER.
  - Advanced FEC codes with decoding latency typically in the order of micro seconds.
  - Improving pre-FEC BER from 1.97E-2 to 1.953E-2 could bring down the post-FEC BER from 1E-13 to 1E-14.

FEC1 & FEC3	FEC2	Optical BER	Post-FEC BER	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate
2-way RS(544,514)	OFEC	1.970E-2	1.00E-13	~1µs	YES	NO	8x106.25G or 4x212.5G	~1 Tb/s
2-way RS(544,514)	OFEC	1.953E-2	1.00E-14	~1µs	YES	YES		

Data from ITU-T G.709.3/Y.1331.3 (12/20) Table III.1

Summary Table

Example	FEC			Optical BER	Post-FEC BER	FEC Latency	1E-13	1E-14	SerDes Rate	Optical Rate	Total Relative Area
1-1	2-way RS(544,514)			2.2E-4	1.1E-15	51.2 ns	YES	YES	8x106.25 Gb/s		4.0
				2.4E-4	4.1E-15		YES	YES			
1-2	RS(576,514)			1.1E-3	7.9E-15	70.4 ns	YES	YES	8x112.5 Gb/s or 4x225 Gb/s	4x225 Gb/s	7.6
				1.2E-3	5.9E-14		YES	NO			
				1.3E-3	1.8E-13		NO	NO			
1-3	2-way RS(544,514) + SD BCH(360,340)			2.0E-3	7.3E-15	62.4 ns	YES	YES			6.04
	2-way RS(544,514) + SD BCH(144,136)			2.4E-3	4.5E-15	60.8 ns	YES	YES			4.68
2	2-way RS(544,514) + HD BCH(360,340)			1.0E-3	1.0E-13	53.6 ns	YES	NO	8x106.25 Gb/s or 4x212.5 Gb/s	4x225 Gb/s	4.05
	2-way RS(544,514) + SD BCH(360,340)			1.9E-3	7.3E-15	62.4 ns	YES	YES			6.04
	2-way RS(544,514) + SD BCH(144,136)			2.3E-3	4.6E-15	60.8 ns	YES	YES			4.68
3-1	2-way RS(544,514)	RS(576,514)	2-way RS(544,514)	1.1E-3	1.7E-15	172.8 ns	YES	YES	8x106.25 Gb/s or 4x212.5 Gb/s	4x225 Gb/s	15.60
				1.2E-3	1.6E-14		YES	NO			
3-2	2-way RS(544,514)	2-way RS(544,514) +SD BCH(360,340)	2-way RS(544,514)	2.0E-3	1.0E-14	164.8 ns	YES	YES			14.04
		2-way RS(544,514) +SD BCH(144,136)		2.4E-3	4.5E-15	163.2 ns	YES	YES			12.68
3-3	2-way RS(544,514)	OFEC	2-way RS(544,514)	1.970E-2	1.0E-13	~1µs	YES	NO		~1 Tb/s	--
				1.953E-2	1.0E-14		YES	YES			

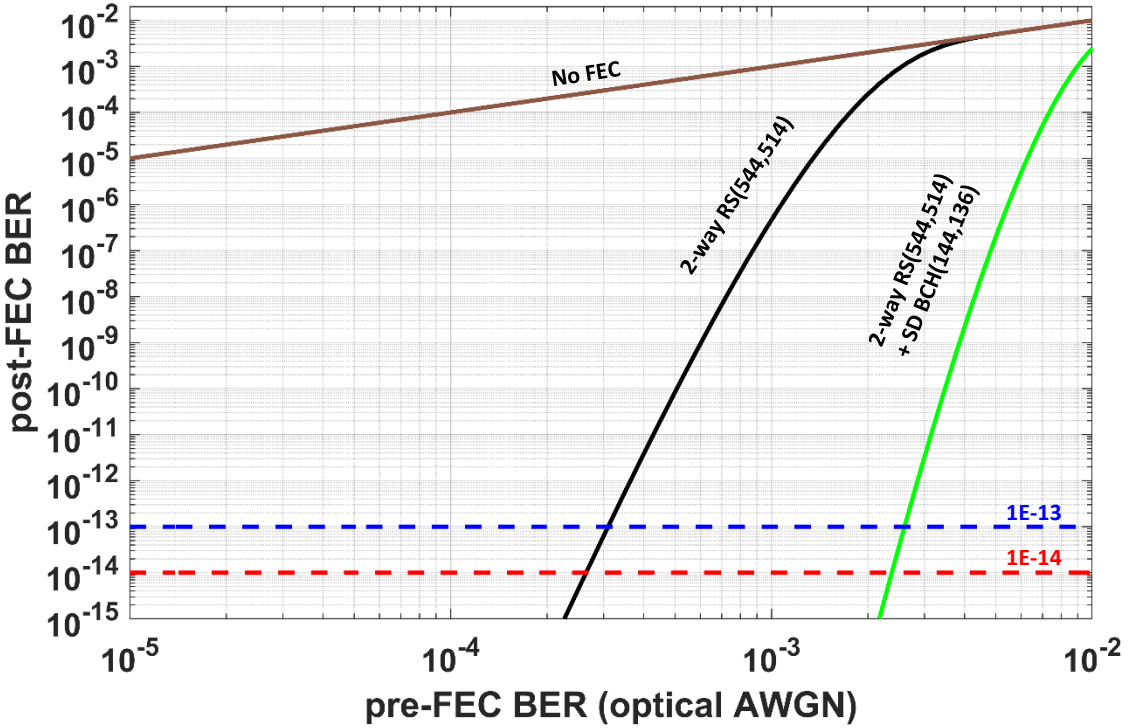
- RS(544,514) + SD BCH concatenated FEC has advantages in performance, latency and area for 200G/lane optical links, while being compatible with 100G/lane AUI specifications.

Example: Pre-FEC BER Required Improvement for 1E-14

- The FEC performance waterfall curve becomes steeper as coding gain increases.

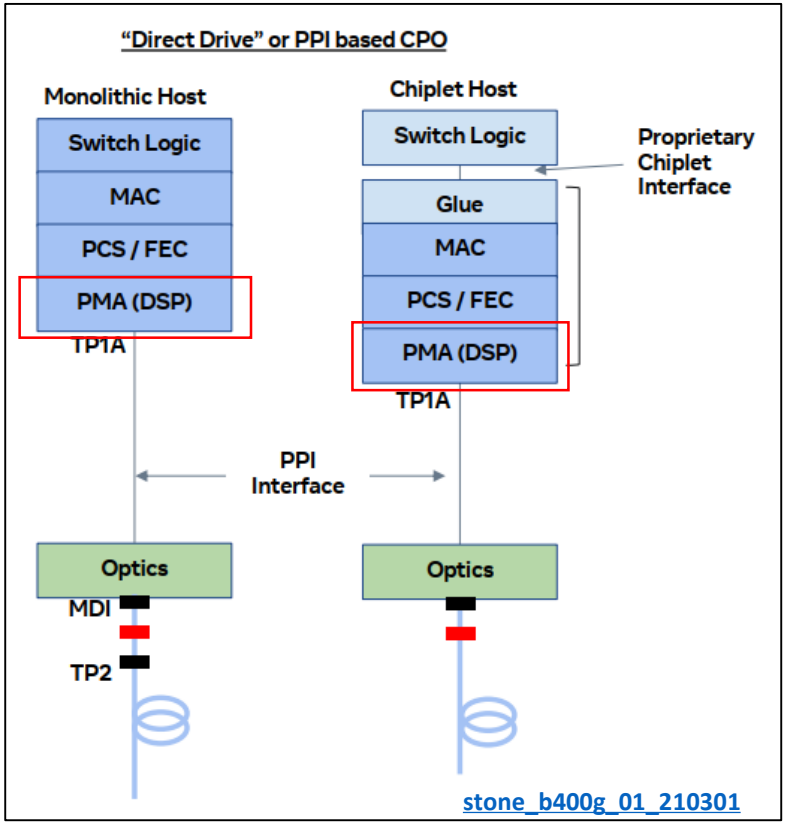
FEC	Pre-FEC BER	Post-FEC BER
2-way RS(544,514) + SD BCH(144,136)	2.60E-3	1.0E-13
	2.37E-3	1.0E-14

- For the RS + SD BCH concatenated FEC, improving pre-FEC BER from 2.60E-3 to 2.37E-3 could bring down the post-FEC BER from 1E-13 to 1E-14, which is within the manufacturer margin.

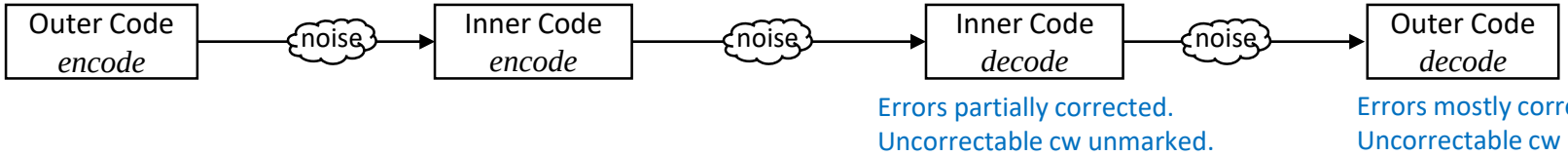


Application Considerations – CPO Feasibility and Interop with FPP

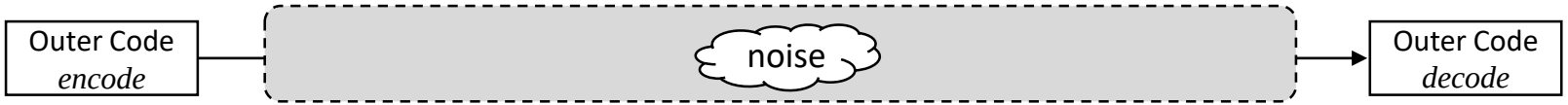
- End-to-End RS FEC or concatenated FEC:
  - Both FPP and PPI based CPO can use E2E FEC scheme.
  - Naturally supports interop between CPO and FPP modules.
- Encapsulated concatenated FEC:
  - Both FPP and AUI based CPO can use encapsulated concatenated FEC scheme.
  - Can be interoperable with FPP with inner code in modules.
- Segmented FEC:
  - Segmented FEC does not support PPI based CPO.



FEC Error Marking Mechanism to Ensure Proper MTTFPA



- **Concatenated FEC:** Error Marking is performed by the outer code only.
  - Uncorrectable inner codewords have a second chance to be corrected by the outer code.
  - Errors introduced by the link segments and inner code could be treated as a black box noise source.



- Same idea has been used in 802.3cw, where inner soft extended hamming code does not require error marking, and outer staircase code has the responsibility for error marking.

- **Segmented FEC:** Uncorrectable codewords SHOULD be properly marked every time a FEC is terminated.
  - Each segment must have proper MTTFPA in order to meet the end-to-end MTTFPA requirement.
  - Each segment must have proper BER/FLR in order to meet the end-to-end BER/FLR requirement.

Summary

- The purpose of this contribution is to answer the questions and concerns brought up during BER objective discussions, especially on FEC cost.

- 1E-14 BER objective could be supported by affordable FEC architectures.

Acknowledgements

- The authors would like to thank Huijian Zhang and Xianwen Qiu from Huawei for their help in FEC area and latency estimation.

Thank you.

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