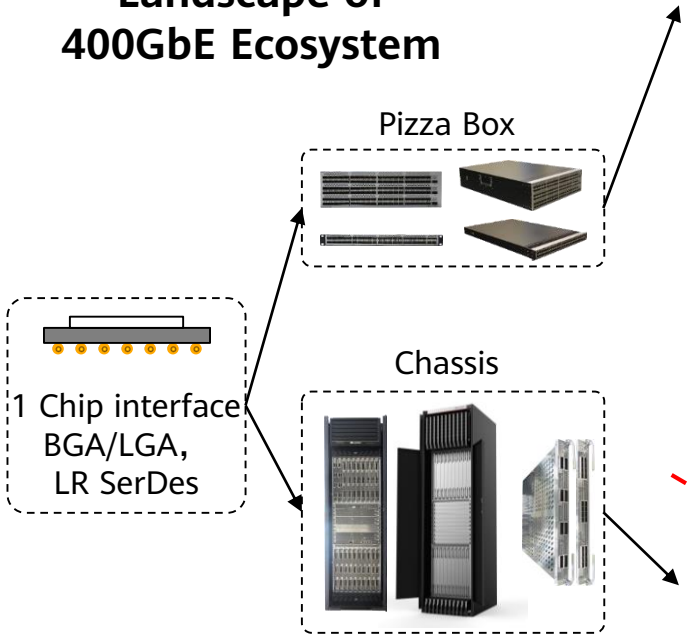
# Considerations on beyond 100G per lane electrical objectives

Yuchun LU, Yan ZHUANG, Huawei Technologies

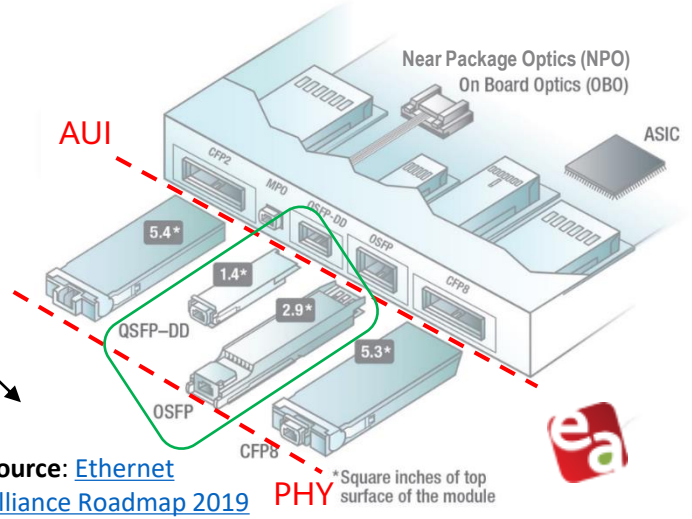
IEEE P802.3 B400G Study Group, Interim, 17 May 2021

# Electrical interfaces are critical: a historical view!

**Landscape of 400GbE Ecosystem**




| Standards | Interface | Modulation |
|---|---|---|
| IEEE 802.3bs | ~~400GAUI-16~~ | ~~NRZ~~ |
| | 400GAUI-8 | PAM4 |
| IEEE 802.3ck | 400GAUI-4 | PAM4 |
| Future | 800GAUI-8,<br>200GAUI-1, 400GAUI-2<br>800GAUI-4, 1600GAUI-8 | SE-PAM4?<br>PAM-4? |




**Source**: Ethernet Alliance Roadmap 2019

PHY

| Standards | Interface | Reach | Media | Architecture |
|---|---|---|---|---|
| IEEE 802.3bs | SR16 | 100m | MMF | 16*25G NRZ 850nm |
| | **DR4** | **500m** | **SMF** | **4*100G PAM4 1300nm** |
| | FR8 | 2km | SMF | 8*50G PAM4 LWDM |
| | LR8 | 10km | SMF | 8*50G PAM4 LWDM |
| IEEE 802.3cm | SR8 | 100m | MMF | 8*50G PAM4 850nm |
| | SR4.2 | 100m | MMF | 8*50G PAM4 BiDi 850/910nm |
| IEEE 802.3cn | ER8 | 40km | SMF | 8*50G PAM4 LWDM |
| IEEE 802.3cw | ZR | 80km | SMF | Coherent DP-QAM16 DWDM |
| IEEE 802.3cu | FR4 | 2km | SMF | 4*100G PAM4 CWDM |
| | LR4-6 | 6km | SMF | 4*100G PAM4 CWDM |
| IEEE 802.3db (In progress) | VR4 | 50m | MMF | 4*100G PAM4 850nm |
| | SR4 | 100m | MMF | 4*100G PAM4 850nm |
| 100G Lambda MSA | FR4 | 2km | SMF | 4*100G PAM4 CWDM |
| | LR4-10 | 10km | SMF | 4*100G PAM4 CWDM |
| CWDM8 MSA | CWDM8-2 | 2m to 2km | SMF | 8*50G NRZ CWDM |
| | CWDM8-10 | 2m to 10km | SMF | 8*50G NRZ CWDM |
| Future | 800GbE DR4/ FR4/LR4 …<br>1600GbE DR8/ FR8/LR8 … | ? to ? Km | SMF<br>MMF? | 4*200G PAM4<br>…<br>8*200G PAM4<br>… |

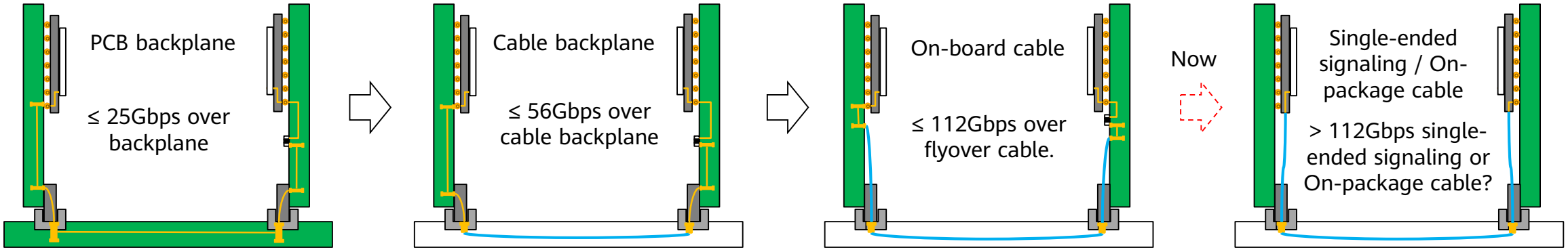
* Electrical PHYs are not listed.

**1 chip interface** → 2 types of equipment → **1~2 mainstream** types of module → **Many types of physical medium**

"Co-Packaging Optics (CPO)" means the AUI interface might different, or even disappear depends on the CPO implementation, "Optical interfaces" become the only maintainable interface which is diverse;
"Near-Package Optics (NPO)" needs standard AUI interface definition. But the pluggable feature may disappear. The "linecard/box" type may be diverse.
The "CPO" and "NPO" lead to diverse "chip" or "linecard/box" design.

# Roadmap for Long Reach SerDes technology

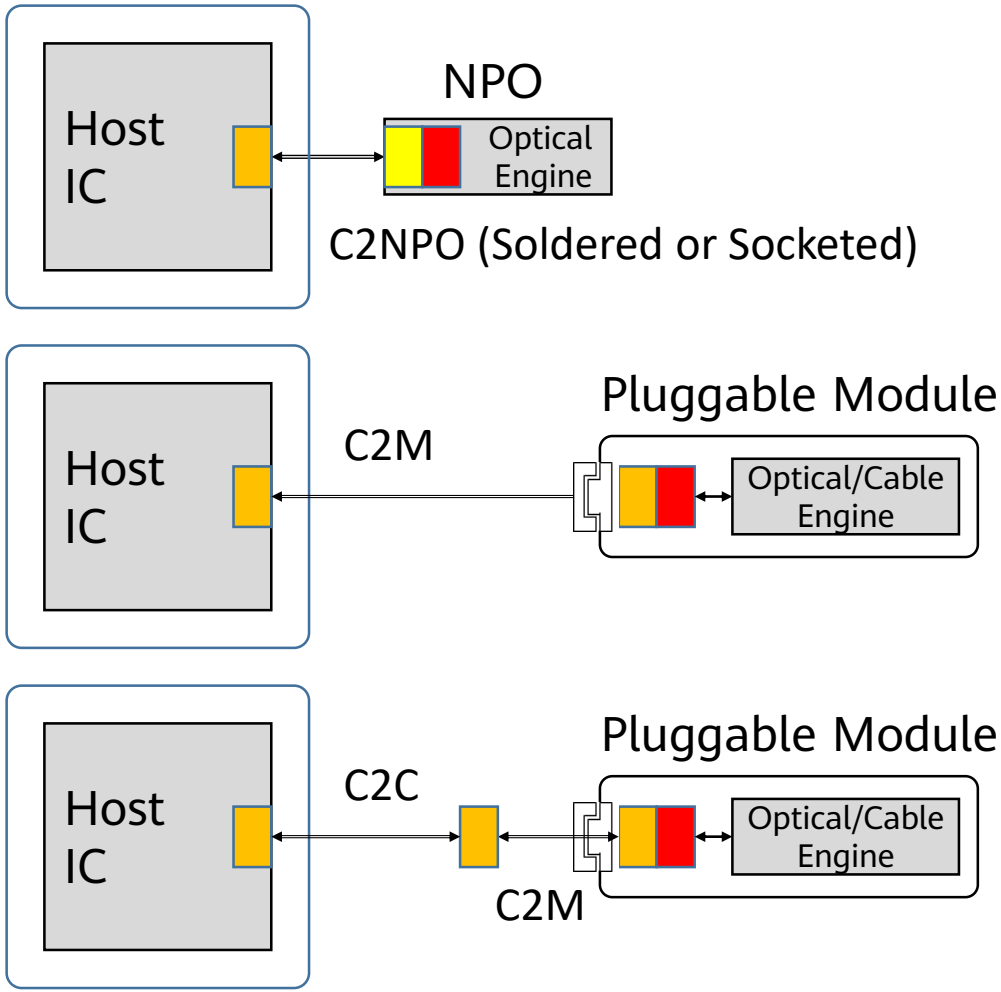
| IEEE Project | IEEE802.3ap | IEEE802.3bj | IEEE 802.3cd | IEEE 802.3ck | TBD |
|---|---|---|---|---|---|
| Ethernet Rate | 10G | 100G | 50/100/200G | 100/200/400G | 800/1600G |
| Timeline | 2004~2007 | 2011~2014 | 2016~2018 | 2018~2021? | 2021 ~ ? |
| Per-lane rate & modulation | 10G NRZ | 25G NRZ / ~~PAM4~~ | 50G PAM4 | 100G PAM4 | 200G<br>SE-PAM4? / PAM-4? |
| Insertion loss & Reach objectives | 1m PCB backplane w/o cable definition | **35dB**@12.89GHz NRZ<br>~~33dB@7GHz PAM4~~ | **30dB**@13.28GHz | **28dB**@26.56GHz | **22dB**?@?GHz |
| | | **5m** cable | **3m** cable | **2m** cable | **1.5 or 2.0m** cable? |
| Transceiver architecture | Analog<br>DFE | Analog<br>DFE | Analog / DSP<br>DFE / FFE+DFE | DSP<br>FFE+DFE / MLSE | DSP<br>MLSE / MIMO ? |



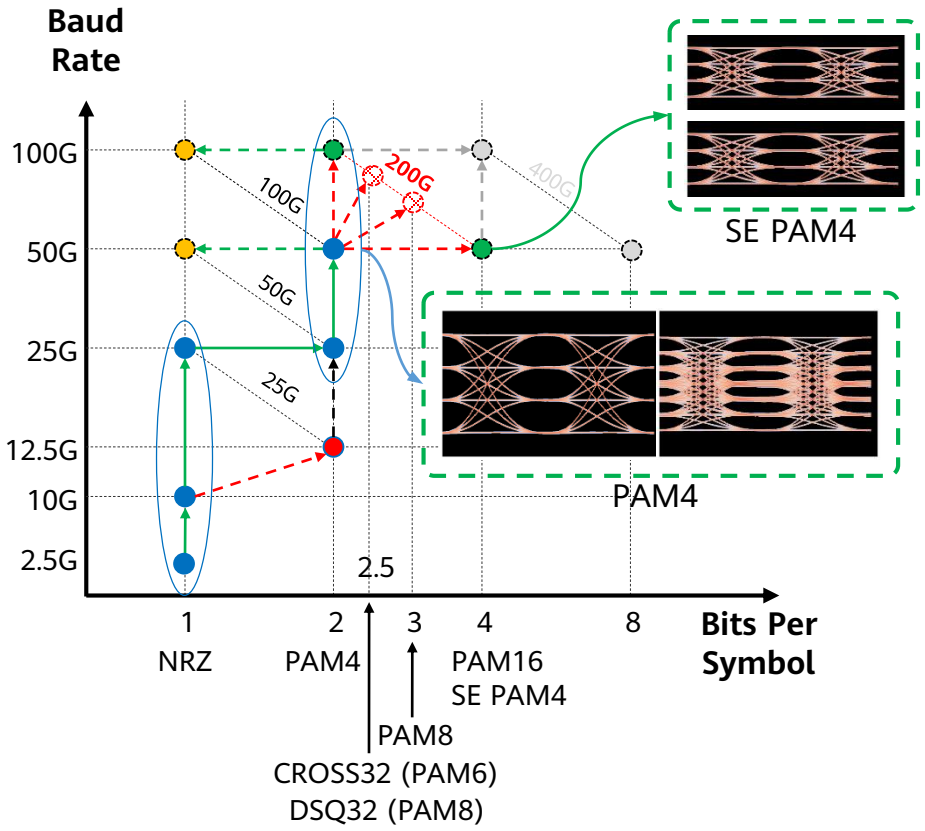

* Show only backplane applications.

# Scenarios for electrical links

- Scenarios for electrical link:
  - Die-to-die, in/near-package-optics, host-to-CDR, chip-to-module.
  - Chip-to-chip, mid-plane/backplane/cable.
- Scenarios need to be considered for standardization:
  - Chip-to-Near-Package-Optics (C2NPO)
  - Chip-to-module (C2M)
  - Chip-to-chip (C2C)
  - Backplane & Cable (KR & CR)



# Roadmap for beyond 100G SerDes



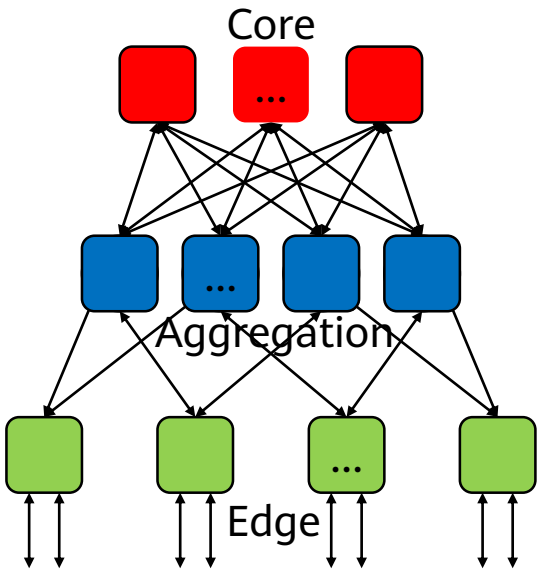

lu_b400g_01_210322

- **Commonality** should be reserved as much as possible. Common signaling with application-specific performance is always preferred!
- **Compatibility** with at least one generation of slower speed SerDes should be reserved to support the hieratical deployment of networks.

- Analysis shows that 200G electrical interfaces are feasible. More investigations are needed in task force phase.
  - lyubomirsky_b400g_01_210329, healey_b400g_01a_210329, lu_b400g_01_210322.
- With “advanced signaling schemes”, “advanced DSP algorithms” as well as “better channel design”, 200G/lane KR/CR electrical interfaces are feasible.
- Technically, the “Commonality” and “Compatibility” can be reserved for 200G/lane electrical itnerfaces.

# Commonality and Compatibility

- **Commonality**: 200G/lane transceiver with application-specific performance.
  - 25G NRZ: AMS (e.g. n-tap DFE) cover all the scenarios with configurable settings.
  - 50G PAM4:
    - AMS (e.g. n-tap DFE) covers all scenarios (CR/KR/C2C/C2M) with small margin and low power.
    - DSP (e.g. n-tap FFE + 1-tap DFE) covers all scenarios (CR/KR/C2C/C2M) with large margin.
  - 100G PAM4:
    - AMS (e.g. n-tap DFE) covers C2C/C2M for low power applications.
    - DSP (e.g. n-tap FFE + 1-tap DFE) covers all the scenarios (CR/KR / C2C/C2M).
  - 200G Signaling TBD:
    - AMS (e.g. n-tap DFE) covers C2M/C2NPO for low power applications.
    - DSP (e.g. m-tap FFE+1-tap DFE/MLSE) covers CR/KR/C2C / C2M/C2NPO.
- **Compatibility**: Support 100G/lane link with 200G/lane transceiver.
  - Support the hieratical deployment of networks.



# Proposed Objectives (100G/lane for 800GbE)

- Define an eight-lane 800Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100Gb/s per lane optical signaling. **(C2M)**
- Define an eight-lane 800Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications. **(C2C)**
- Define an eight-lane 800Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ 28 dB at 26.56 GHz. **(KR)**
- Define an eight-lane 800Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 2 m. **(CR)**

Follow 100G/lane electrical objectives defined in 802.3ck for 8*100GbE

# Proposed Objectives (200G/lane for 800GbE)

- Define a four-lane 800Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(C2M)**
- Define a four-lane 800Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications. **(C2C)**
- Define a four-lane 800Gb/s Attachment Unit interface (AUI) for chip-to-near-package-optics applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(or merged with C2C and C2M objectives)**
- Define a four-lane 800Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ TBD(22?) dB at TBD GHz. **(KR)**
- Define a four-lane 800Gb/s PHY for operation over copper cables with lengths up to at least TBD(1.5 or 2.0?) m. **(CR)**

# Proposed Objectives (200G/lane for 1.6TbE)

- Define an eight-lane 1.6Tb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(C2M)**
- Define an eight-lane 1.6Tb/s Attachment Unit Interface (AUI) for chip-to-chip applications. **(C2C)**
- Define an eight-lane 1.6Tb/s Attachment Unit interface (AUI) for chip-to-near-package-optics applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(or merged with C2C and C2M objectives)**
- Define an eight-lane 1.6Tb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ TBD(22?) dB at TBD GHz. **(KR)**
- Define an eight-lane 1.6Tb/s PHY for operation over copper cables with lengths up to at least TBD(1.5 or 2.0?) m. **(CR)**

# Proposed Objectives (200G/lane for 200GbE)

- Define a single-lane 200Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(C2M)**
- Define a single-lane 200Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications. **(C2C)**
- Define a single-lane 200Gb/s Attachment Unit interface (AUI) for chip-to-near-package-optics applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(or merged with C2C and C2M objectives)**
- Define a single-lane 200Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ TBD(22?) dB at TBD GHz. **(KR)**
- Define a single-lane 200Gb/s PHY for operation over copper cables with lengths up to at least TBD(1.5 or 2.0?) m. **(CR)**

# Proposed Objectives (200G/lane for 400GbE)

- Define a two-lane 400Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(C2M)**
- Define a two-lane 400Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications. **(C2C)**
- Define a two-lane 400Gb/s Attachment Unit interface (AUI) for chip-to-near-package-optics applications, compatible with PMDs based on 200Gb/s per lane optical signaling. **(or merged with C2C and C2M objectives)**
- Define a two-lane 400Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ TBD(22?) dB at TBD GHz. **(KR)**
- Define a two-lane 400Gb/s PHY for operation over copper cables with lengths up to at least TBD(1.5 or 2.0?) m. **(CR)**

# Summary and Recommendation

- Proposed objectives for 100G/lane 800GbE electrical interfaces (follow 100G/lane electrical objectives defined in 802.3ck for 8*100GbE).
  - 8*100G/lane based AUIs including C2M and C2C.
  - 8*100G/lane PHYs including CR and KR.
- Proposed objectives for 200G/lane electrical interfaces.
  - N*200G/lane based AUIs including C2M, C2C and C2NPO(or merged with C2M and C2C).
  - N*200G/lane PHYs including CR and KR.
  - N=1, 2, 4, 8.
- End-to-End FEC covers all potential B400G AUIs and optical PHYs (200G/lane)?

- Recommendation
  - Commonality: 200G/lane transceiver with application-specific performance.
  - Compatibility: Support 100G/lane link with 200G/lane transceiver.

# Thanks!
# Q&A

# 200G PAM Signaling Comparison

Bandwidth limited

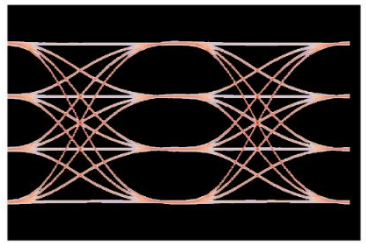
Bandwidth limited

Jitter limited

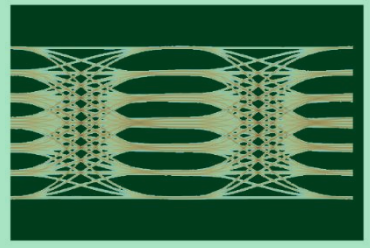
| Modulation | | Symbol Rate (GBaud) | Unit Interval (ps) | Nyquist Frequency (GHz) | Bandwidth Requirements ** (GHz) | Bits per Symbol | # of Levels | Penalty @SER=1e-4 (Amplitude Normalized) | Penalty @SER=1e-4 (Power Normalized) |
|---|---|---|---|---|---|---|---|---|---|
| PAM4 | Regular | 106.25 | 9.4 | 53.125 | 80 | 2/1 | 4 | 0.00 @53GHz | 0.00 @106GHz |
| | PR | 106.25 | 9.4 | 26.5625* | 40* | 2/1 | 4 | 6.14 @26GHz* | 3.13 @53GHz |
| | SE | 53.125 | 18.82 | 26.5625 | 40 | 4/1 | 4 (x2) | 6.02 @26GHz | 3.01 @53GHz |
| PAM6 | CROSS-32 | 85 | 11.76 | 42.5 | 64 | 5/2 | 6 | 4.89 @43GHz | 3.46 @85GHz |
| PAM8 | DSQ-32 | 85 | 11.76 | 42.5 | 64 | 5/2 | 8 | 4.81 @43GHz | 3.68 @85GHz |
| | Regular | 70.83 | 14.12 | 35.42 | 53 | 3/1 | 8 | 7.45 @35GHz | 6.32 @71GHz |

* Estimated as 1 / 4 of Baud Rate. ** frequency range with smooth IL or small ILD.

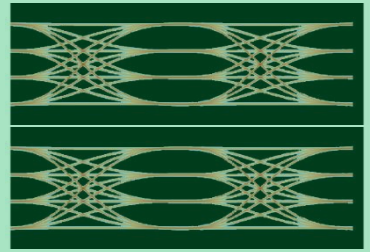
SNR limited



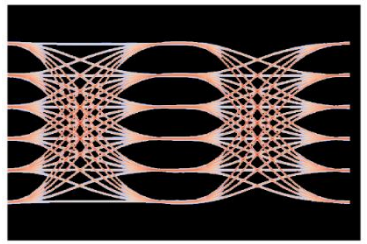
PAM4



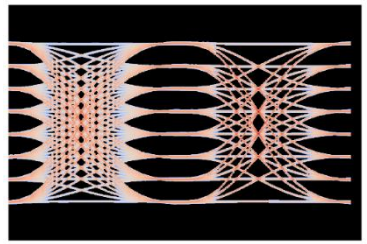
PR PAM4



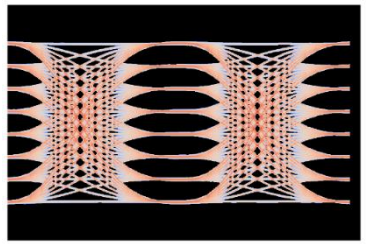
SE PAM4



CROSS-32 (PAM6)



DSQ-32 (PAM8)



PAM8