Electrical Interface Objective Wording

May 2021 Session

Kent Lusted, Intel

Adam Healey, Broadcom

r(0)

May 17, 2021

Supporters and Contributors

- Supporters:
  - Matt Brown, Huawei Canada
  - Chris Cole, II-VI
  - Dave Ofelt, Juniper
  - Adee Ran, Cisco
  - Scott Schube, Intel
  - Rob Stone, Facebook
- Contributors:
  - Matt Brown, Huawei Canada

Overview

- This presentation is focused on the approach to the electrical interface objectives for consideration by the IEEE 802.3 Beyond 400 Gb/s Ethernet Study Group
  - Other participants provided technical feasibility contributions
- It does not include guidance for any electrical backplane and copper cable physical layers

A Brief Historical Look at Electrical Interface Objectives

- The approaches in the past have been inconsistent. More recently, the electrical interface objectives are being called out.
- IEEE P802.3bs defined a "high level" objective for the AUIs:
  - "Support optional Attachment Unit Interfaces for chip-to-chip and chip-to-module applications" (see 3bs archive)
- IEEE P802.3cd did not have any AUI objectives (see 3cd archive)
  - Defined 10 AUIs even though there were no AUI objectives
- IEEE P802.3ck defines detailed objectives for the AUIs:
  - "Define a single-lane 100 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling"
  - "Define a single-lane 100 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications"
  - Similarly for two-lane 200 Gb/s AUIs and four-lane 400 Gb/s AUIs

See also https://www.ieee802.org/3/B400G/public/21_0118/dambrosia_b400g_01_210118.pdf slide 9

AUI C2M

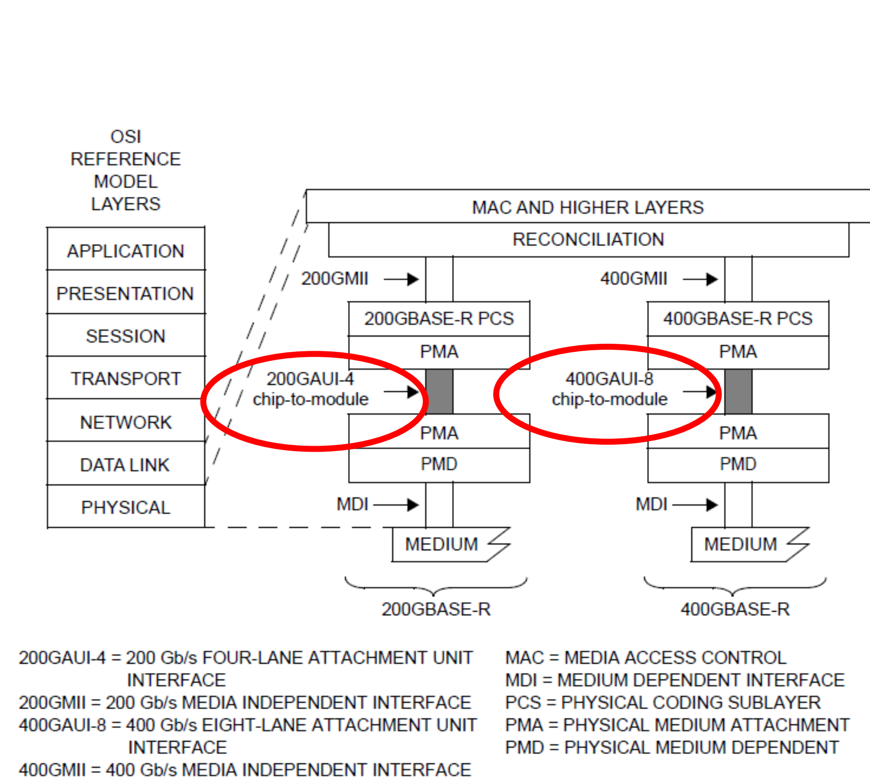
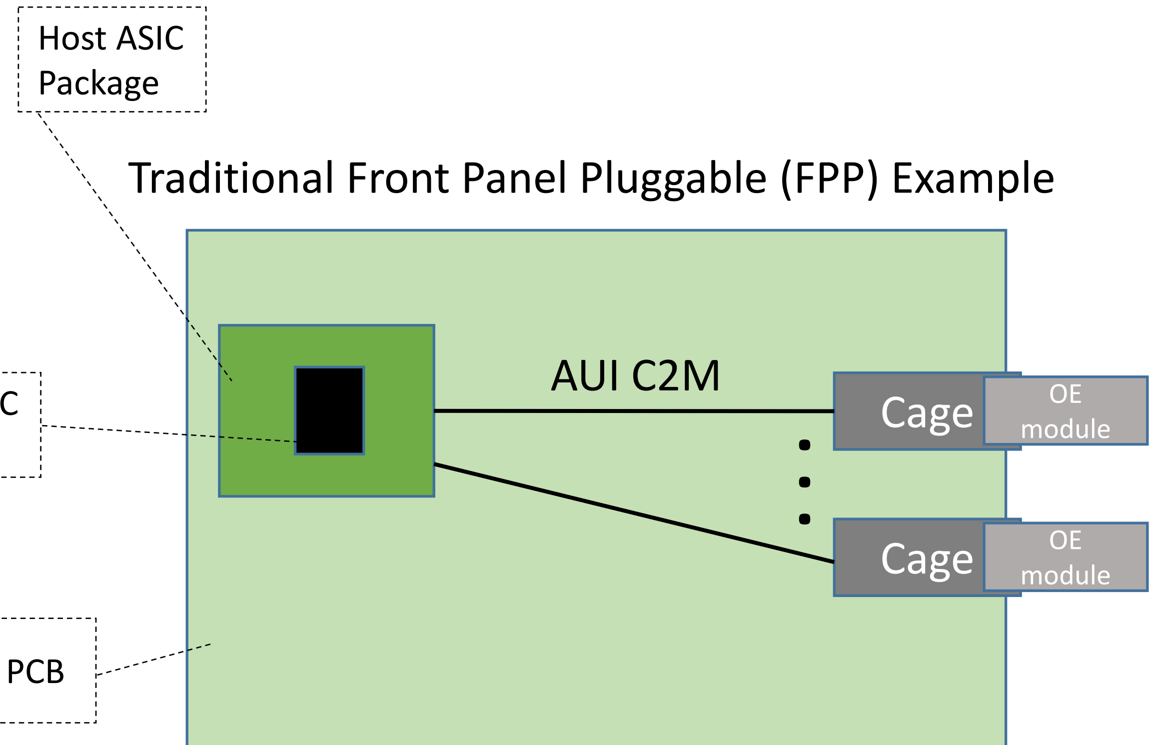


Figure 120E–1—Example 200GAUI-4 and 400GAUI-8 chip-to-module relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

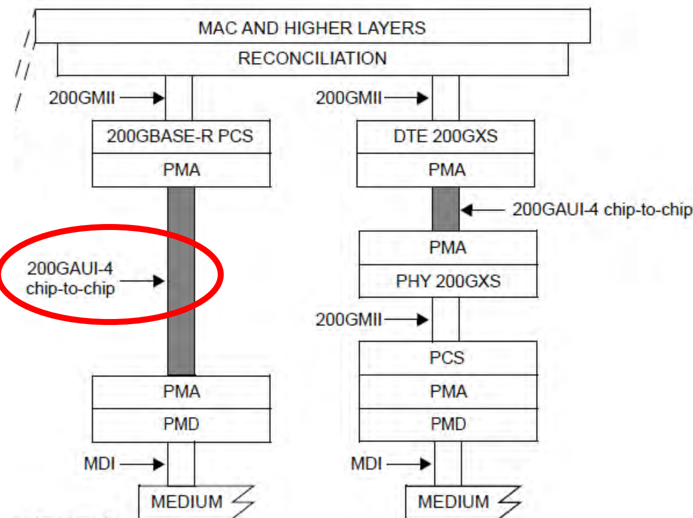
Figure above is an example architectural diagram of existing chip-to-module electrical interfaces and is not intended to represent the direction this group must take.



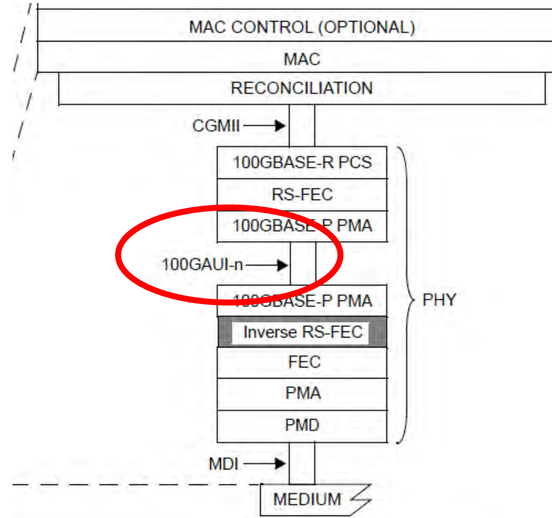
Compliance measurements are done at a separable connector

AUI C2C

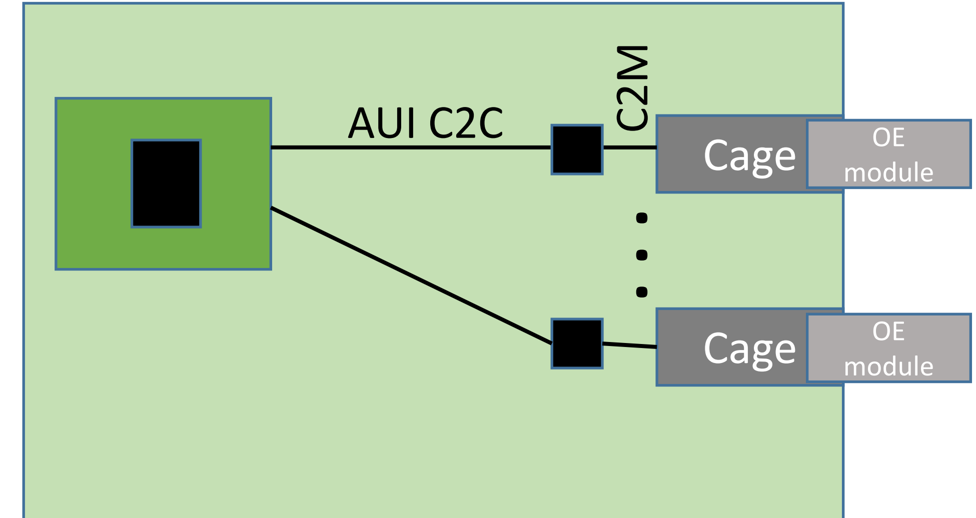
Annex 120D:
Figure 120D-1



Clause 152:
Figure 152-1



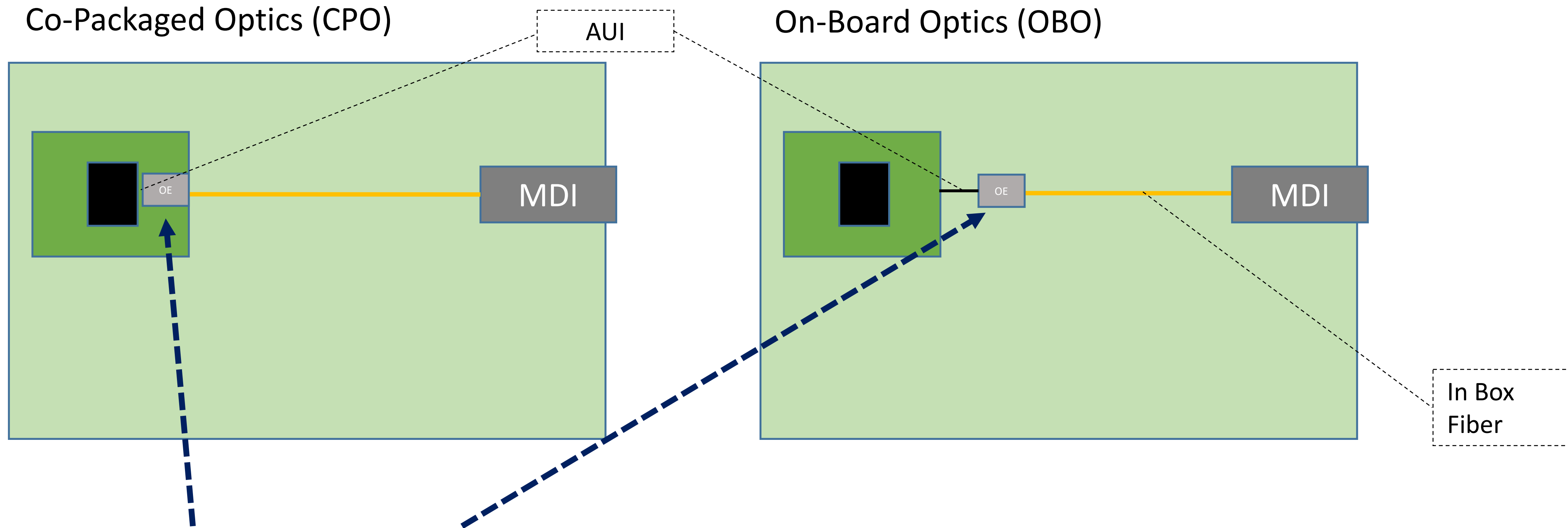
Traditional Examples



Figures above are example architectural diagrams of existing chip-to-chip electrical interfaces and are not intended to represent the direction this group must take.

Compliance measurements are done on components (via test fixtures for Tx/Rx) prior to assembly into a fixed configuration (on which compliance tests can no longer be performed)

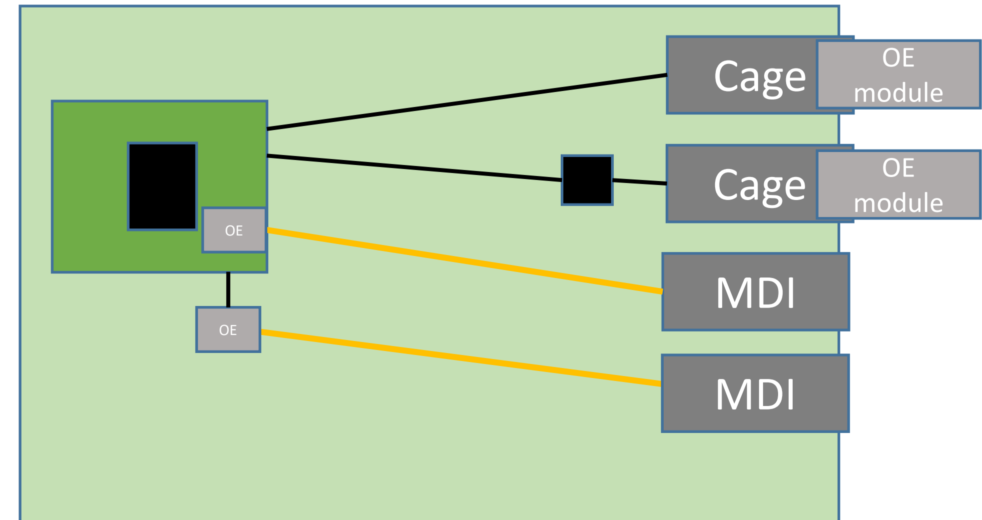
New Use Cases Emerging: CPO, OBO



- Co-packaged/On-Board optics may have fixed (soldered) and pluggable (e.g. socketed) instantiations
- Such instantiations map to "traditional" AUI C2C and C2M compliance test models
- May warrant specialized AUI C2C and C2M variants optimized for reduced maximum reach (loss)

Summary

- Objectives for both chip-to-module (C2M) and chip-to-chip (C2C) AUIs are necessary to address the “traditional” usage cases
- CPO and OBO use cases are chip-to-module or chip-to-chip AUIs
  - CPO and OBO are different physical realizations of the “traditional” use case
  - Conceivable to optimize these AUI variants for the shorter reach/loss
- PPI interfaces are not included at this time
- Objectives for chip-to-module and chip-to-chip AUIs are proposed



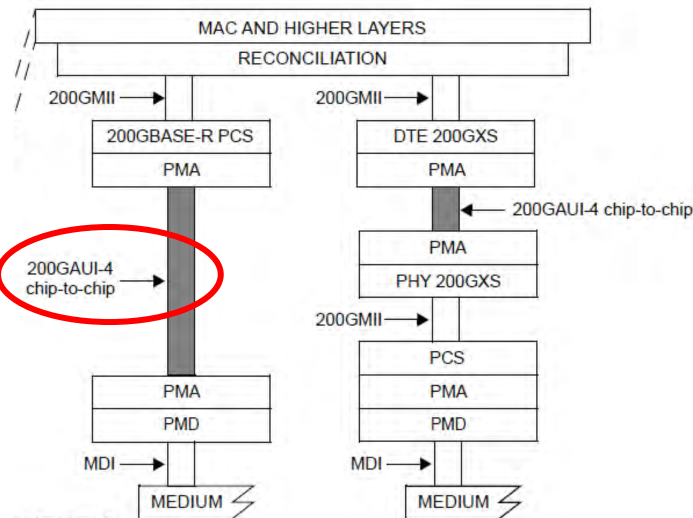
Proposed Straw Poll(s)

- I would support adopting the following objective:
  - Support optional eight-lane 800 Gb/s attachment unit interfaces for chip-to-module and chip-to-chip applications
- I would support adopting the following objective:
  - Support optional four-lane 800 Gb/s attachment unit interfaces for chip-to-module and chip-to-chip applications

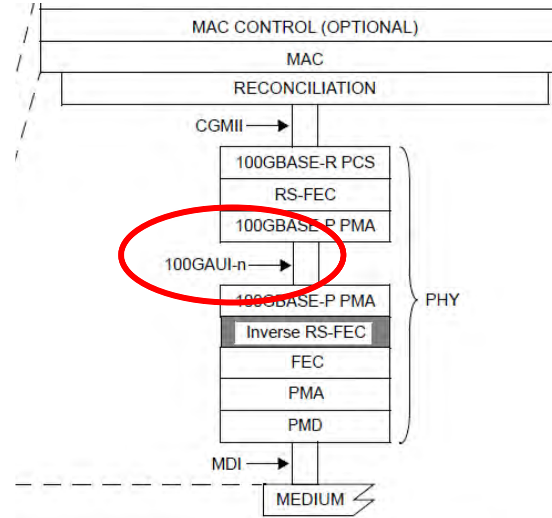
Thanks!

AUI C2C

Annex 120D:
Figure 120D-1



Clause 152:
Figure 152-1



Traditional Examples