16-lane 1.6TbE AUI Objective Proposal

A test & measurement perspective

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Introduction

- A case will be made for 16-lane 1.6 Tb/s AUI objective is as follows:
  - A wide AUI is consistent with previous Ethernet generations for early deployment
  - A 16-lane AUI essential for early development and for test equipment
  - Many relevant form factors support a 16-lane interface
  - Digital architecture is a simple extension of an 8-lane architecture and would be consistent with 400GbE
  - Per-lane electrical specifications would be the same or similar to those for 8-lane 800 Gb/s AUI

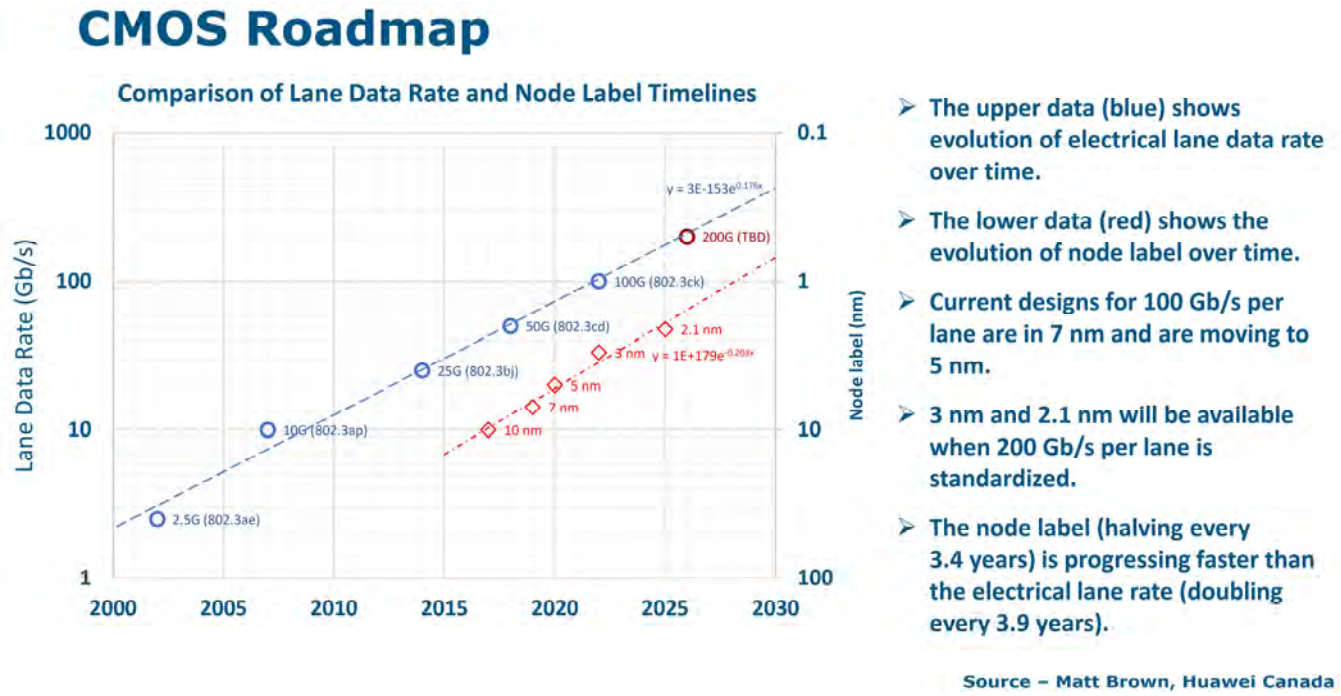
Background and 1.6TbE Standard Objectives Progress

- In June 3 meeting, 1.6 Tb/s rate and some related objectives were adopted, such as 8-lane AUI for C2M and C2C applications.
- For previous ratified Ethernet standards, multiple AUIs were developed, in 50/100/200/400GbE to support different implementation schemes.
- For 800 Gb/s standard, both 8-lane and 4-lane AUI objectives have been adopted.

	AUI Per-lane Signaling Rate				
	10 Gb/s	**25 Gb/s**	**50 Gb/s**	**100 Gb/s**	**200 Gb/s**
25GbE		25GAUI			
40GbE	XLAUI				
50GbE		LAUI-2 50GAUI-2	50GAUI-1		
100GbE	CAUI-10	CAUI-4 100GAUI-4	100GAUI-2		
200GbE		200GAUI-8	200GAUI-4		
400GbE		400GAUI-16	400GAUI-8	400GAUI-4	
800GbE				8-lane	4-lane
1.6TbE				16-lane?	8-lane

Potential 200 Gb/s SerDes Standard Timeline

- 200 Gb/s lane rate is estimated to be available >2025, while 100 Gb/s lane rate can be available from 802.3ck at an earlier time.
- 100 Gb/s SerDes ICs for both module and switch silicon have been in use since ~2020. A growing ecosystem around 100 Gb/s SerDes is gaining traction with multi-vendor interoperating.



CFI: Beyond 400 Gb/s Ethernet

More Historical Data of Electrical I/O

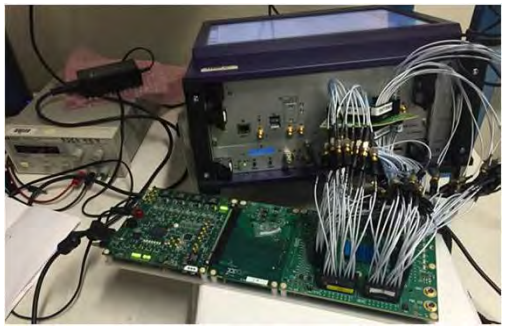
Ethernet rate (Gb/s)	1st electrical I/O		High volume electrical I/O		~years between 1st million units shipped
	# of lanes	Gb/s	# of lanes	Gb/s	
10	16	0.62	1	10	10
40	16	2.5	4	10	10
100	10	10	4	25	5
200	8	25	4	50	4
400	16	25	4	100	5

See : cole_b400g_01b_210322

Role of Test Equipment in B400GbE Standard Development

- Test & measurement play a critical role in new technology role out and are critical for providing real data for validation of assumptions in performance.
- Test equipment (often based on large FPGAs) needs to be ready 1-2 years before formal standardization so vendors can start to develop key elements (including pluggable optics & IP – FEC/PCS).
- Without access to test equipment the ecosystem can stall and key decisions on implementation are delayed impacting cost and time to market and leaving key assumptions on technology performance unverified until very late in the standardization process.
- A healthy multi-vendor test and measurement ecosystem is critical in bringing to market reliable products that can inter-operate in an open ecosystem to deliver confidence to end users.

802.3bs 400GE Timeline from Test & Measure Perspective



IEEE 802.3bs standardized already 'healthy' ecosystem underway and key elements validated and functional

2015 **2016** **2017** **2018** **2019**

Early 400GE technology
16 x 25G
Support traffic, FEC, PCS testing

1st PAM-4 (external gearbox + FPGA)
L1 support for debugging

Native FPGA PAM-4
Full feature coverage – L1 to full traffic

Ecosystem needs
Electrical inter-connect
IC & module
IP development (PCS/FEC)

Ecosystem needs
Alpha modules
1st network elements
Performance validation

Ecosystem needs
Mainstream turn up
SVT & system S/W
Production
Field deployment

Test Equipment Rely on FPGA and 100 Gb/s SerDes for 1.6TbE

- Today we are beginning to see the emergence of large scale FPGAs that natively support 100G SERDES I/O.
- Test & measurement solutions needed to develop, debug and validate high speed Ethernet need a demanding combination of
  - Large fast fabric that supports functional blocks such as FEC, PCS and MAC with the addition ‘features’ that T&M must support such as error injection, PCS manipulation and MAC runt frame generation.
  - Fast SERDES, ideally at the designed AUI rate as external gearbox's and mux devices can interfere with many test scenarios and may cause uncertainty in the nature of certain errors. External gearbox ICs also may impede the test sets abilities to generate other stresses including frequency variation and skew which play a major role in IC and module development, debugging and validation.
- Within the next ~ 5 year window the only viable path for T&M equipment to service the needs of an earlier 1.6TbE ecosystem is based around the emerging 100G SERDES based FPGAs.
- 200G SERDES technology is extremely challenging and many other factors including connectors, PCBs and packaging may impact 200G based interconnect to such an extent that interconnect between a DUT and T&M equipment could dominate any test results.

16-lane 1.6TbE AUI Enables X16 Form Factors

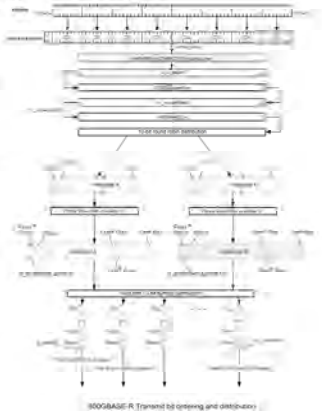
- 1.6TbE objectives right now, supporting 16-lane AUI objective will enable industry to develop specification based on mature 100 Gb/s per lane technology as per any potential 8 lane AUI for 800G, either from MSA or other SDO.
- In "booth_b400g_01_210301":
  - 4, 8 and 16 lane modules exist or are in development (i.e. QSFP112, QSFP-DD, OBOx16)
- In "New OSFP-XD form factor could challenge co-packaged optics"
  - https://www.lightwaveonline.com/optical-tech/transmission/article/14205029/new-osfpxd-form-factor-could-challenge-copackaged-optics
  - The OSFP-XD specifications will feature a power envelope of 33 W and a (2x8) 16-lane electrical interface, with optical interfaces that vary by module scheme.
- In "OIF launches 3.2T Co-Packaged Module project"
  - https://www.lightwaveonline.com/optical-tech/components/article/14199184/oif-launches-32t-copackaged-module-project
  - The module codified within the IA is expected to use 100G electrical lanes

Include 16-lane 1.6TbE AUI from 1.6TbE Logic Layer Perspective

- In "wang_b400g_01_210208": 16 FEC lanes is necessary to support 16-lane AUI as interoperating issue, which is feasible and minor additional cost comparing to supporting 8-lane AUI objective only.
  - 16-lane 1.6TbE AUI specification is similar as 8-lane 800GbE AUI.

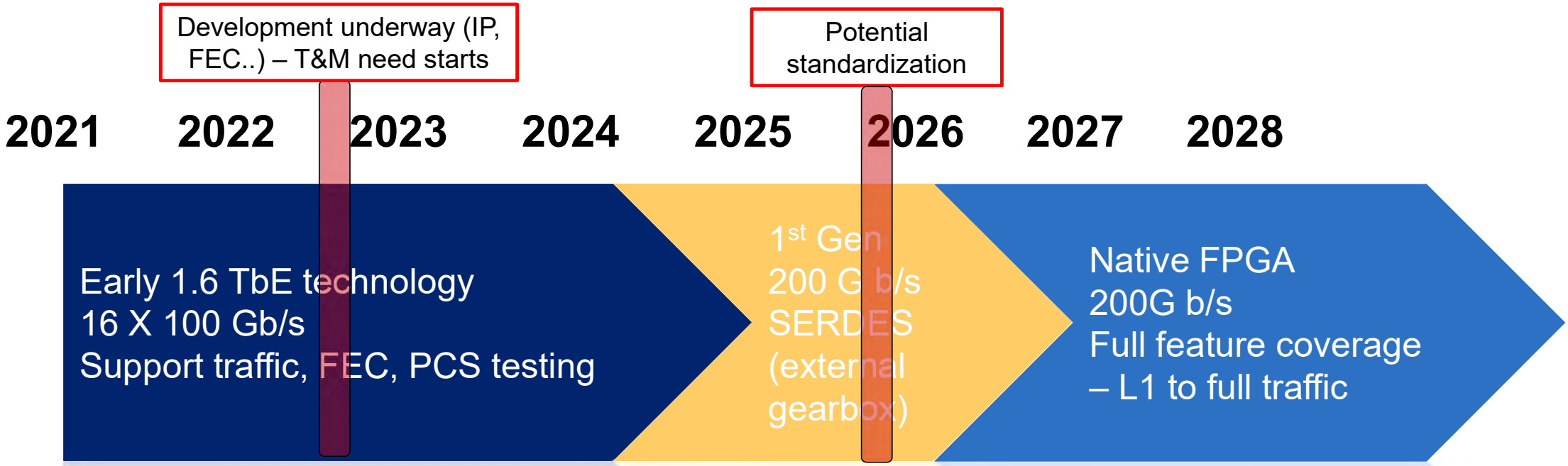
FEC Approach A: End to End with RS(544,514)

- Assume refer to current specification of 802.3bs/cu/ck for 100G/s per lane, it is feasibility to double the rate of CL119 Architecture for 400GbE to achieve 800Gb/s capability of 7nm node ASIC, 640bit@1.33GHz for RS(544,514) decode with the following advantage:
  - Two 400Gb/s capability code words interleave to be fully backward compatible 802.3bs/cu/ck specification for 100G/s per lane, further lower power
  - Lower latency comparing to 400GbE with 12.8ns Versus 25.6ns for block time of RS(544,514) decode
  - 8 FEC Lanes, low complex and permit 100Gb/s and great per lanes AUI, Electrical/Optical Medium
  - For future ≤5nm node ASIC: same architecture with 1280bit@1.33GHz can enable 1.6Tb/s throughput RS(544,514) decode with 16 FEC Lanes



- In 802.3bs for 200GbE/400GbE development,16 FEC lanes for 400GbE and 8 FEC lanes for 200GbE to support 25 Gb/s signaling rate AUI.

Leveraging X16 AUI to Support Successful 1.6TbE



R&D work on ASICs and modules for 1.6Tb Ethernet typically starts ~3 years before standardization (early 2026) and this is best served by a X16 AUI as it can be supported from a T&M perspective (electrical I/O compatibility).

Proposal

- From application and feasibility perspective, the following potential objective for 1.6 Tb/s Ethernet will benefit the industry:
  - Support optional **sixteen-lane** 1.6 Tb/s attachment unit interfaces for chip-to-module and chip-to-chip applications.

Thank you