2.5G/5G PHY/MAC interface and Architecture in 802.3bz

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2.5G/5GBASE-T

Overview

- 802.3bz has established Clause 125 for 2.5G/5G architecture overview
  - Currently Draft 1.2 is in Task Force review
  - Expected to go to WG Ballot in January
- 802.3bz chose NOT to specify an IEEE 802-standardized PHY/MAC extender or AUI
  - Extended XGMII to 2.5G/5Gbps rates as the logical PHY/MAC interface
  - Favored vendor differentiation and technology flexibility

Clause 125 – 2.5G/5G Ethernet

125. Introduction to 2.5 Gb/s and 5 Gb/s networks

125.1 Overview

125.1.1 Scope

This clause describes the general requirements for 2.5 Gigabit and 5 Gigabit Ethernet. 2.5 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 2.5 Gb/s, coupled with any IEEE 802.3 2.5GBASE Physical Layer implementation. 5 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 5 Gb/s, coupled with any IEEE 802.3 5GBASE Physical Layer implementation. 2.5 Gb/s and 5 Gb/s Physical Layer entities, such as those specified in Table 125–1, provide a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface.

2.5 Gigabit and 5 Gigabit Ethernet is defined for full duplex operation only.

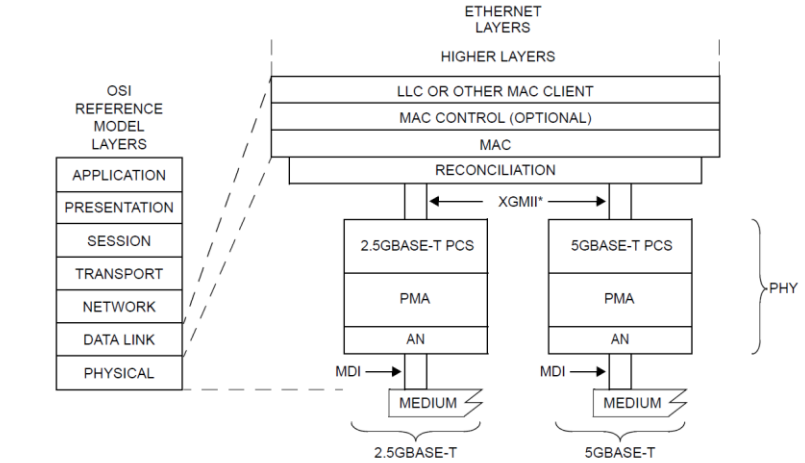


Figure 125–1—Architectural positioning of 2.5 Gigabit and 5 Gigabit Ethernet

Table 125–2—Nomenclature and clause correlation (2.5GBASE and 5GBASE)

Nomenclature	Clause[a]					
	28	46		78	126	126
	Auto-Negotiation	RS	XGMII	EEE	2.5GBASE-T PCS/PMA	5GBASE-T PCS/PMA
2.5GBASE-T	M	M	O	O	M	
5GBASE-T	M	M	O	O		M

[a]O = Optional, M = Mandatory.

So far, all are defined only for BASE-T, ready for new PHY insertion

Clause 45 Management in bz

- Defines selection of new speeds
  - PMA/PMD
  - PCS (not shown)
- 2.5G/5G extended abilities register for PMA/PMD selection

Table 45–4—PMA/PMD control 1 register bit definitions

Bit	Name	Description	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved ~~x 1 x x = Reserved~~ 0 1 1 1 = 5Gb/s 0 1 1 0 = 2.5Gb/s 0 1 0 1 = 400Gb/s 0 1 0 0 = 25Gb/s 0 0 1 1 = 100Gb/s 0 0 1 0 = 40Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10Gb/s	R/W

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change Reserved row and

Insert rows below it in Table 45-6 to include speeds of 2.5Gb/s and 5Gb/s as shown (unchanged rows not shown):.

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.4.15~~:13~~	Reserved for future speeds	Value always 0	RO
1.4.14	5G capable	1 = PMA/PMD is capable of operating at 5 Gb/s 0 = PMA/PMD is not capable of operating as 5 Gb/s	RO
1.4.13	2.5G capable	1 = PMA/PMD is capable of operating at 2.5 Gb/s 0 = PMA/PMD is not capable of operating as 2.5 Gb/s	RO

[a]RO = Read only

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.14	~~Reserved~~2.5/5G extended abilities	~~Value always 0~~1 = PMA/PMD has 2.5/5G extended abilities listed in register 1.21 0 = PMA/PMD does not have 2.5/5G extended abilities	RO

[a]RO = Read only

The MII

- 802.3bz amends Clause 46 to extend XGMII to include 2.5Gbps and 5Gbps operation
  - Several point edits, see examples

46.1.3 Rate of operation

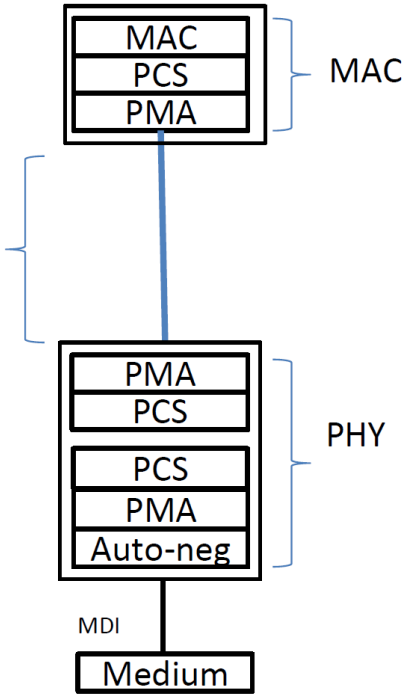
Change Clause 46.1.3 as shown:

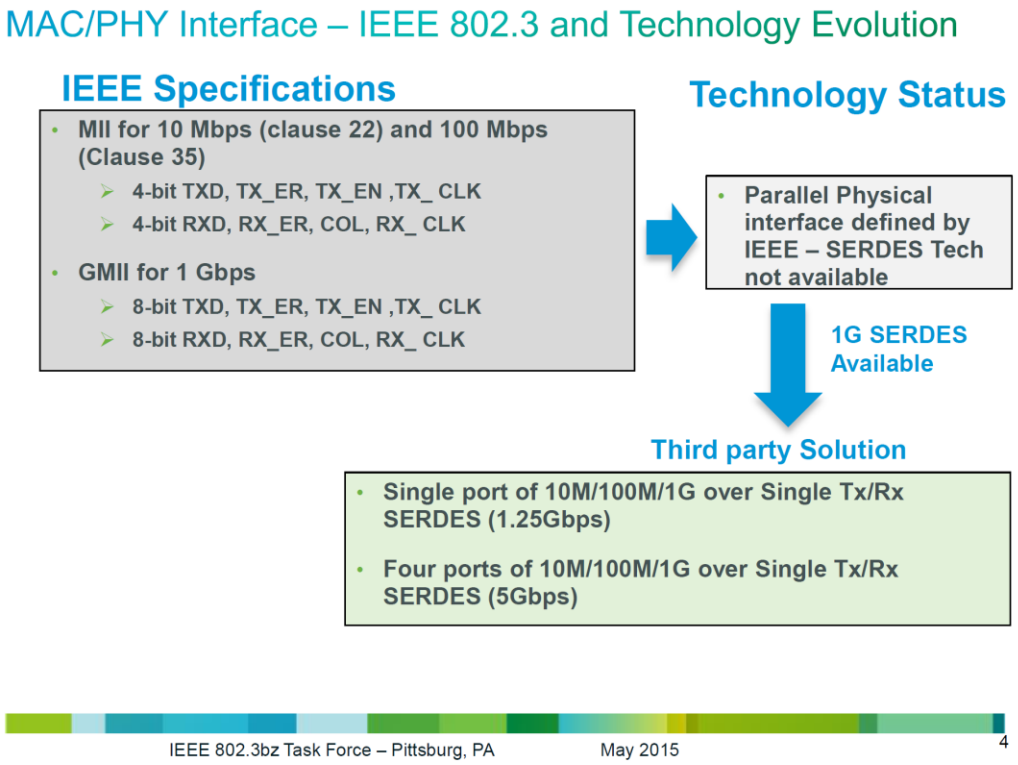
The XGMII supports ~~only the 10 Gb/s~~ MAC data rates of 10 Gb/s, 5 Gb/s, and 2.5 Gb/s as defined within this clause. A compliant device may implement any subset of these rates. Operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35.

The TX_CLK frequency shall be ~~156.25 MHz ±0.01%,~~ one-sixty-fourth of the MAC transmit data rate ±0.01%.

An Electrical Interface Extender?

- See http://www.ieee802.org/3/bz/public/may15/bains_3bz_01b_0515.pdf
- Current PHY/MAC extension interfaces are defined outside of IEEE 802.3
  - Allows multiport interfaces (IEEE 802.3 generally works on a per-port basis)
  - Allows technology evolution and vendor differentiation (MSAs handle this well)





End Result – Specific to BASE-T PHYs?

Summary

- No consistency for IEEE defined MAC/PHY interface - IEEE can only define interface using available technology at time of standardization
- IEEE MAC/PHY specification is limited to one physical port per SERDES
- Third parties MAC/PHY interface will evolve as
  - **Higher SERDES is available at lower cost/power**
  - **More than 1 port over single SERDES – For example with 64b/66b PCS**
    - **8x 1G over 10.3125 Gbps**
    - **4 x 2.5G over 10.3125G**
    - **2 x 5G over 10.3125G**
    - **2 x 10G over 20.6250 etc.**

=> MAC/PHY Interface at IEEE should remain as a logical interface!

Thank You!