Thoughts on Objectives and changing the PLCA RS



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



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What is latency?

- **Proposed definition:**
  Time from when a packet is presented by the MAC client until it is transmitted onto the network.

- **In PLCA, this latency is largely due to:**
  - Waiting for nodes transmit opportunity,
  - Waiting for all other nodes in the cycle to (possibly) transmit, and
  - Backoff due to logical collision

- **The maximum latency is bounded.**

Can we reduce this maximum latency for some traffic?

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Conservation of Latency?

- **Considering the Law of Conservation of Mass:**

In a closed system, mass is neither created nor destroyed in chemical reactions

- **Do we have something similar for latency in PLCA?**

Overall PLCA Latency cannot be eliminated, only removed from some traffic classes or nodes and transferred to others.

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Station-to-Station Interoperability and Compliance

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Interoperability and Compliance

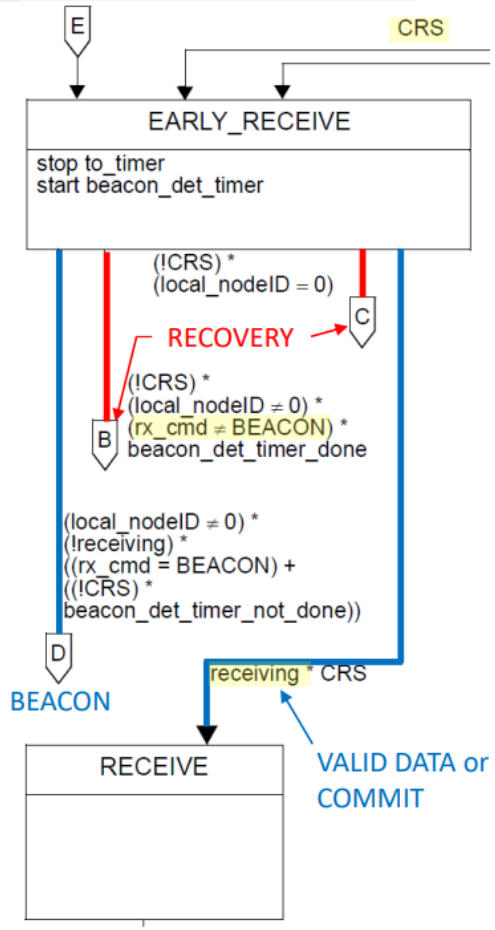
- **Need an objective to support interoperability with existing 10BASE-T1S (Clause 147) and 10BASE-T1M (Clause 188) PHYs.**
  - This implies we shall support existing Clause 148 (PLCA) interoperability when adding a method for latency control.
- **Basic set of requirements:**
  - Do not make changes that would rule existing Clause 148 compliant implementations non-compliant
    - New, optional features shall not break compliance – see D-PLCA
  - Keep interoperability with non E-PLCA capable nodes as well as PLCA capable nodes
    - Addition of a new optional feature is not incompatible with compliance to the original feature set
    - Mixed-node segment may not achieve latency goals, but communication shall be retained
  - Preserve the existing layering structure
  - Improve existing latency predictability

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Preserve PLCA ↔ PHY Compatibility

Constraints to preserve 802.3cg compatibility

- We shall not rely on handling detected collisions
  - Collision detection belongs to the Physical Layer but collision **handling** does not
- Do not add any new physical layer signaling
  - Any signal other than a valid preamble, BEACON or COMMIT will be incompatible with Clause 148
  - That would make existing PLCA nodes go into a recovery/resync state →
- We should avoid **periodic** physical layer signaling on the line
  - PLCA nodes would react to that by signaling a collision in case of concurrent transmissions
  - non-PLCA enabled nodes will assert CRS at each transmission, causing deferral and possibly hampering media access fairness
  - may (likely) impact EMC/EMI performance



https://www.ieee802.org/3/da/public/0321/beruto_3da_01_031021.pdf

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Interoperability with different feature options

- **The addition of a new optional feature is not incompatible with compliance to the original feature set**

- **Mixed PLCA and non-PLCA nodes on the same mixing segment**
  - Reverts to normal CSMA/CD performance with loss of PLCA benefits

- **D-PLCA with non-PLCA nodes**
  - Not prohibited, but not encouraged with a warning: (148.4.4.1)

    Nodes that are not operating with PLCA enabled do not have a specific transmit opportunity assigned to them and should not be present in the collision domain. The existence of nodes with PLCA disabled will prevent D-PLCA enabled nodes from automatically selecting and converging on unique node IDs.

E-PLCA interoperability with non-PLCA and D-PLCA

- **E-PLCA with non-PLCA nodes**
  - Reverts to normal CSMA/CD performance with loss of PLCA and E-PLCA benefits
  - Not recommended
- **E-PLCA with PLCA nodes**
  - Reverts to normal PLCA performance with loss of E-PLCA benefits
  - Not recommended
- **E-PLCA with D-PLCA**
  - Recommend to only D-PLCA during provisioning of mixing segment nodes

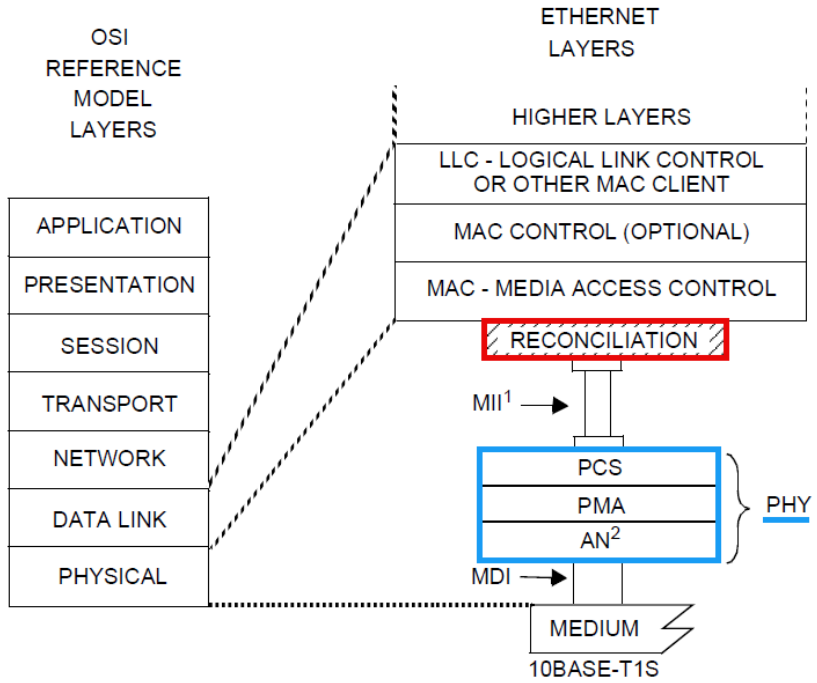
Compliance and Interoperability with the PHY

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The PLCA RS

- **PLCA is specified as a Reconciliation Sublayer**
  - An RS is defined as a box interfacing MII to the MAC Physical Layer Signaling (PLS) service
  - Separate from the PHY

Compatibility with existing PHYs, therefore, mandates compatibility at the MII



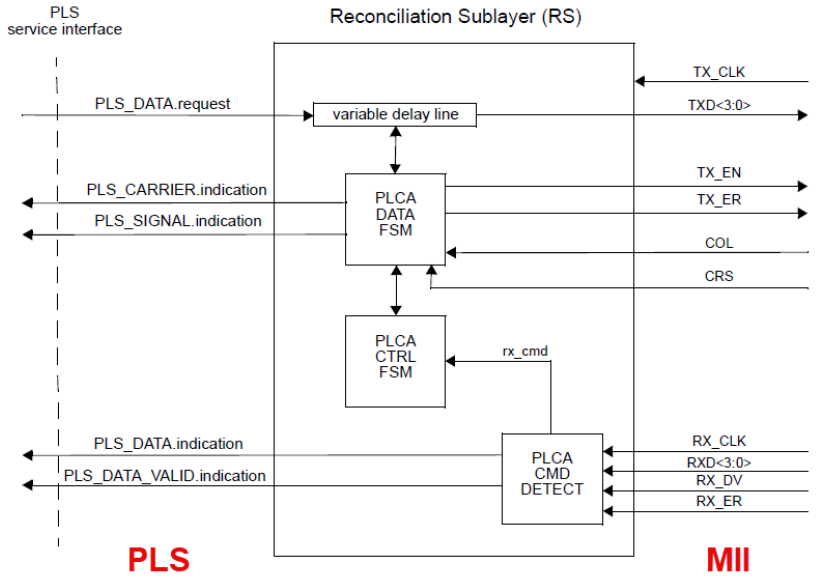


Figure 148–2—PLCA functions within the Reconciliation Sublayer (RS)

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The PLCA RS MII interaction with the PHY

- **There are some very critical timing in the PLCA RS that is related to the PHY and communication over MII**
  - See Table 147-6 (Clause 147.11) and Table 188-5 (Clause 188.11)

Table 147–6—10BASE-T1S delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
TX_EN/TX_ER sampled to MDI output	120	440	ns	Rising edge of MII TX_CLK	First DME clock transition at the MDI
MDI input to CRS asserted	400	1040	ns	First DME clock transition at the MDI	Rising edge of CRS
MDI input to CRS deasserted	640	1120	ns	Last DME encoded zero clock transition at the MDI	Falling edge of CRS
MDI input to COL asserted	0	5	µs	Start of corrupted transmitted signal at the MDI	Rising edge of COL
MDI input to COL deasserted	0	3.2	µs	End of transmission at the MDI	Falling edge of COL
MDI input to RX_DV asserted	2.4	4	µs	First DME clock transition at the MDI	Rising edge of RX_DV
MDI input to RX_ER asserted	1.6	4	µs	First DME clock transition at the MDI	Rising edge of RX_ER

Table 188–5—10BASE-T1M delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
TX_EN/TX_ER sampled to TCI output	120	440	ns	Rising edge of MII TX_CLK	First DME clock transition at the TCI
TCI input to CRS asserted	400	1040	ns	First DME clock transition at the TCI	Rising edge of CRS
TCI input to CRS deasserted	640	1120	ns	Last DME encoded zero clock transition at the TCI	Falling edge of CRS
TCI input to COL asserted	0	5	µs	Start of corrupted transmitted signal at the TCI	Rising edge of COL
TCI input to COL deasserted	0	3.2	µs	End of transmission at the TCI	Falling edge of COL
TCI input to RX_DV asserted	2.4	4	µs	First DME clock transition at the TCI	Rising edge of RX_DV
TCI input to RX_ER asserted	1.6	4	µs	First DME clock transition at the TCI	Rising edge of RX_ER

The PLCA RS MII interaction with the PHY

- **Significant detailed effort was put in to meet PHY timing constraints over MII**

  IEEE 802.3cg Out-of-Cycle Interim, August 14-15, 2019, Milwaukee, WI

  See: https://www.ieee802.org/3/cg/public/Aug2019/r02-33%20Proposed%20Response.pdf

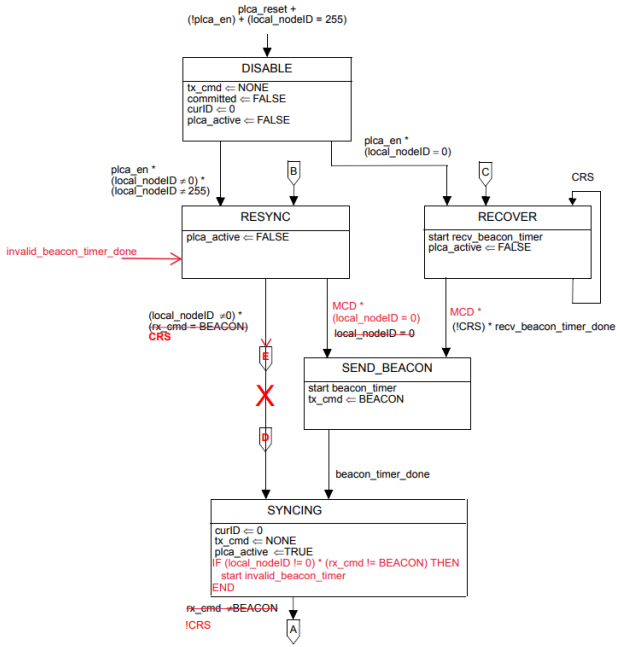


Figure 148–3—PLCA Control state diagram

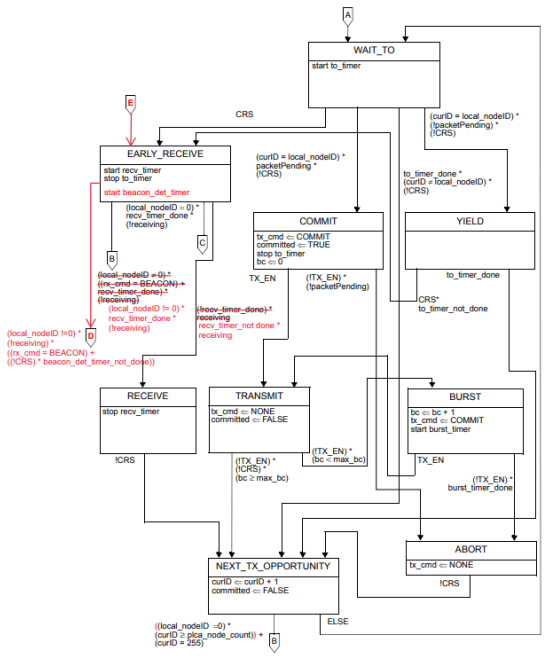


Figure 148–3—PLCA Control state diagram *(continued)*

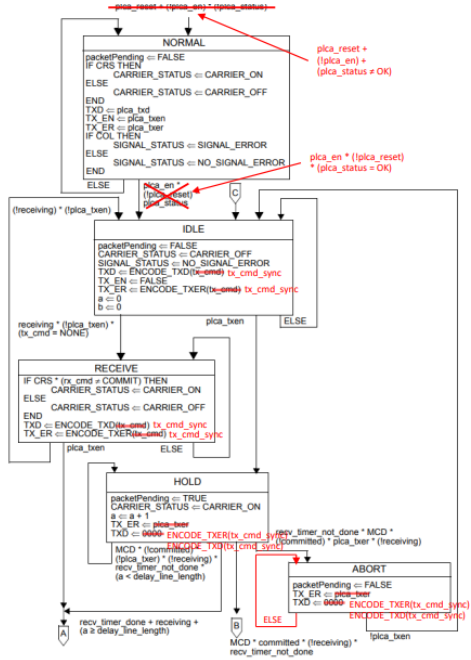


Figure 148–4—PLCA Data state diagram

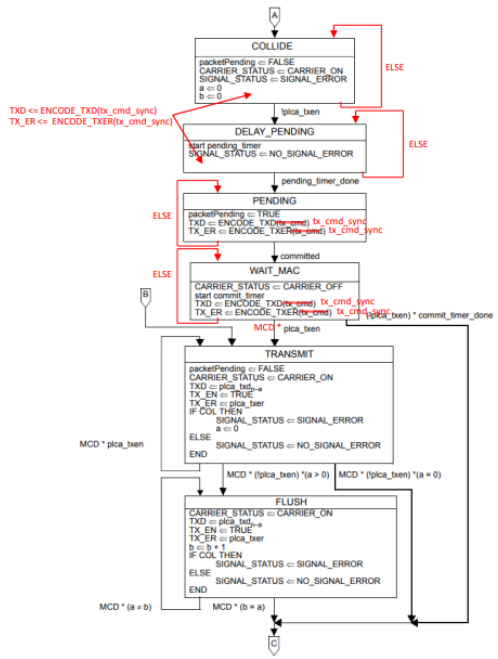


Figure 148–4—PLCA Data state diagram *(continued)*

The PLCA RS

- **Success will require changes to the PLCA RS state diagrams to be minimal and as self-contained as possible.**
  - The state diagrams are critical as they are normative
    - Any text relating to the state diagrams is descriptive and informative
    - Where there is a discrepancy, the state diagrams are to be trusted

- **How was this accomplished when adding D-PLCA?**
  - Small updates to the PLCA Control and Data state diagrams
  - No changes to the PLCA Status state diagram
  - Addition of two new state diagrams for D-PLCA Control and Aging that are separate from the standard PLCA state diagrams.

Let's look at the D-PLCA changes

- **The following pages illustrate changes made in 802.3da to the PLCA state diagrams**
  - D-PLCA changes to existing PLCA state diagrams are highlighted in yellow
  - Fixes to the original PLCA state diagrams are highlighted in blue.

P. Beruto, "PLCA Corner-Case Fixes," Feb. 23, 2022.
https://www.ieee802.org/3/da/public/032322/beruto_3da_01_230222_plca_fixes.pdf

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PLCA Control State Diagram

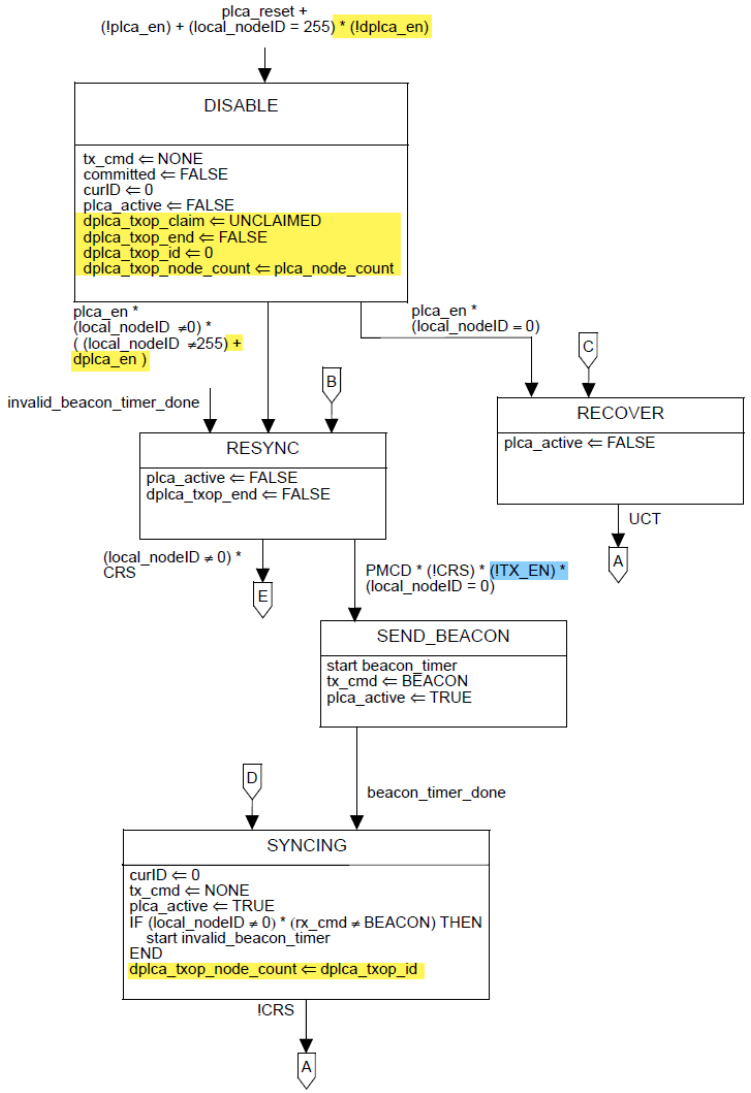


Figure 148–3—PLCA Control state diagram, part a

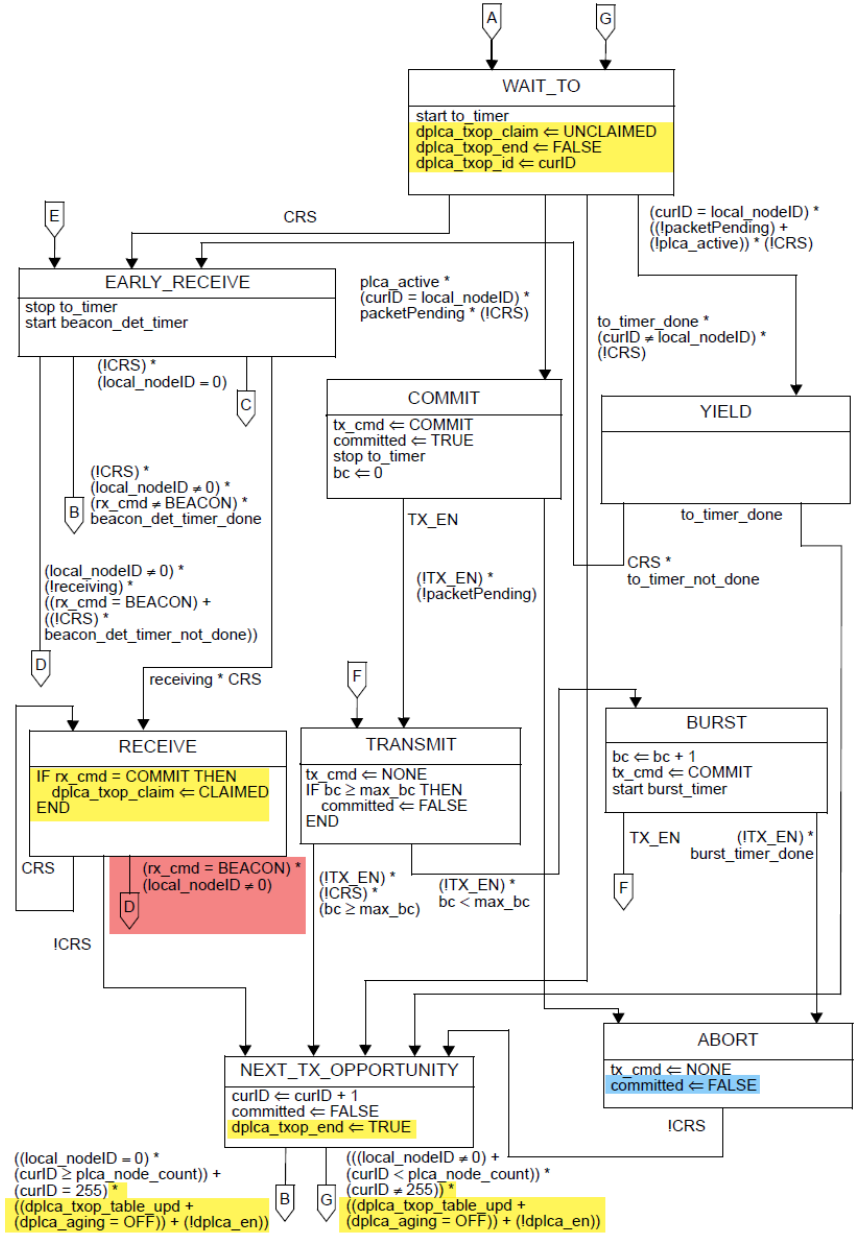


Figure 148–4—PLCA Control state diagram, part b

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PLCA Data State Diagram

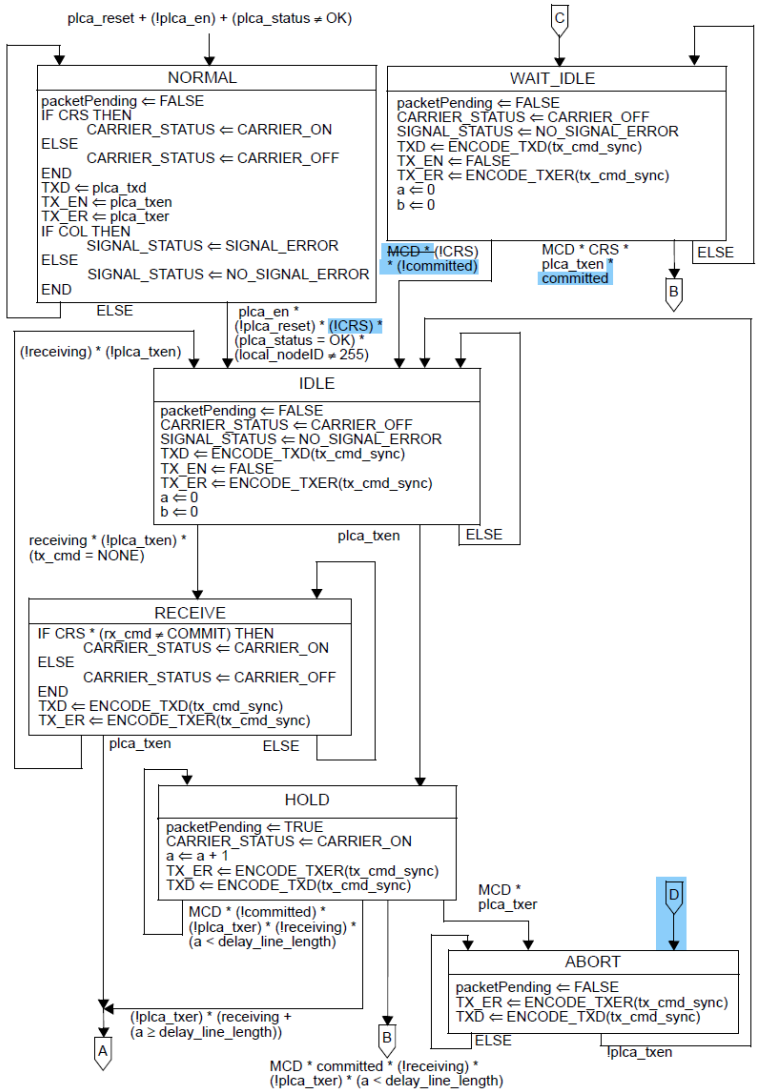


Figure 148–5—PLCA Data state diagram, part a

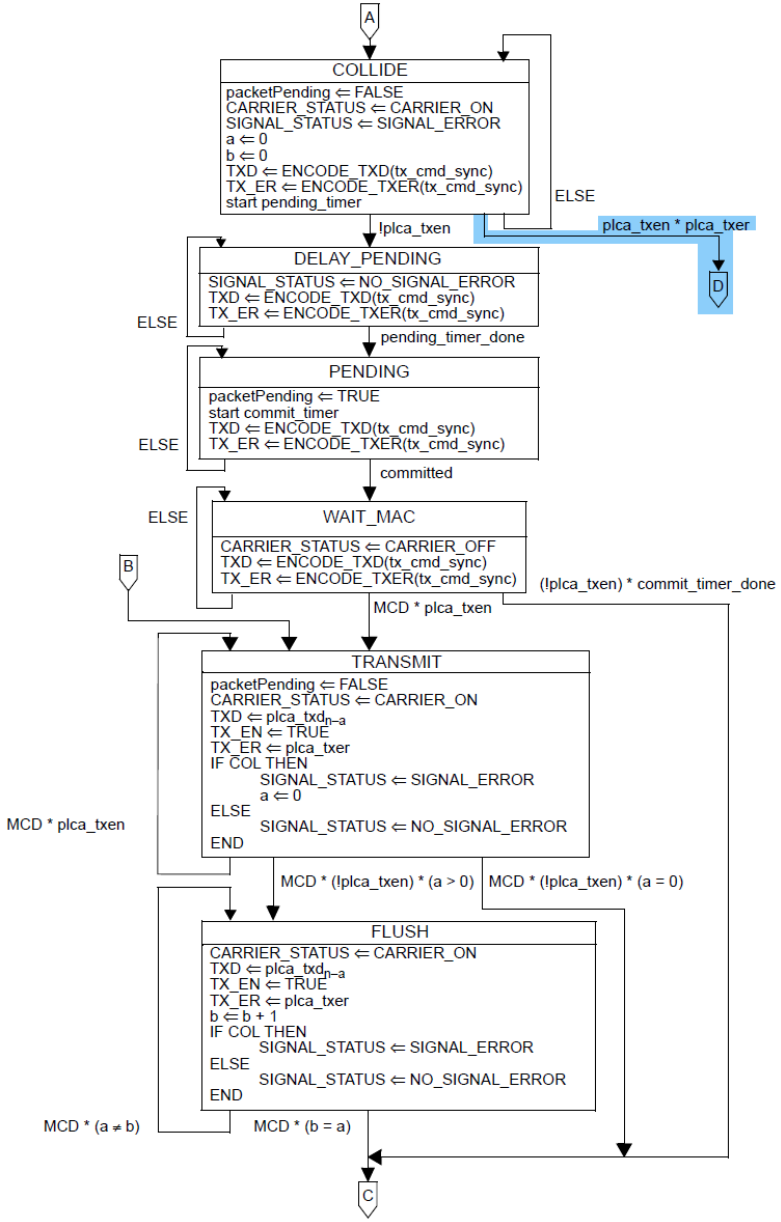


Figure 148–6—PLCA Data state diagram, part b

D-PLCA Aging State Diagram - New

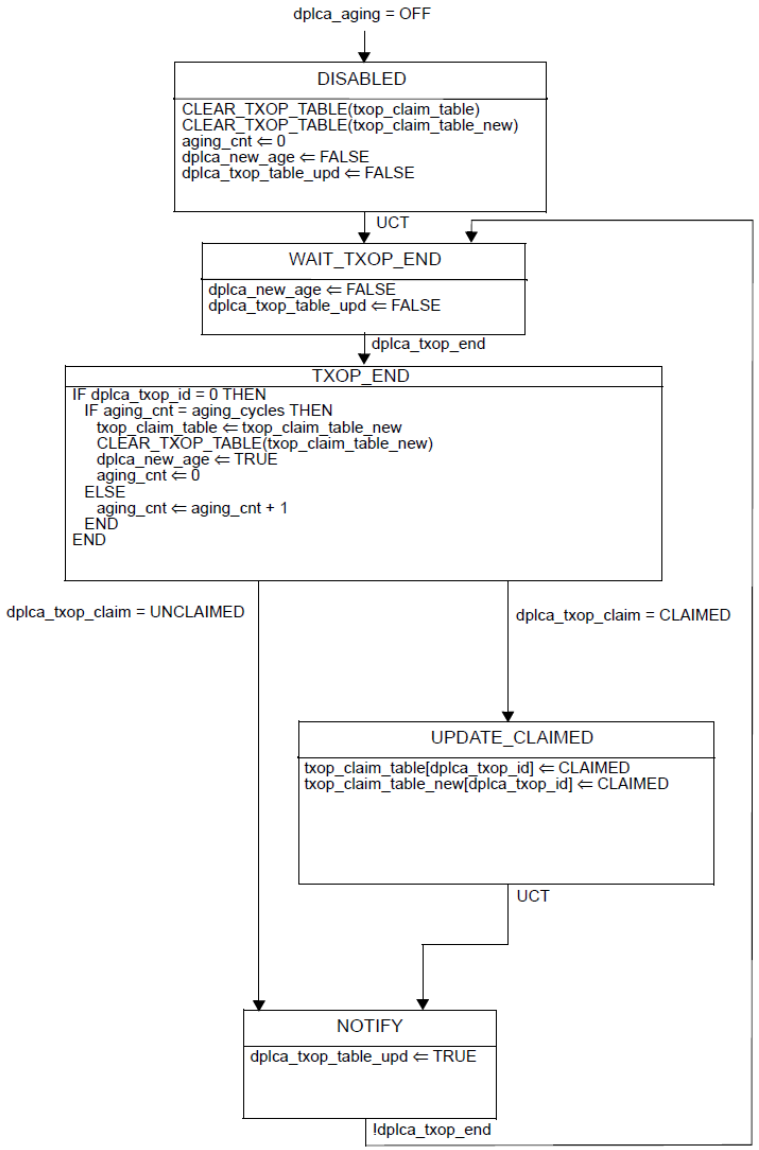


Figure 148–9—D-PLCA Aging state diagram

D-PLCA Control State Diagram - New

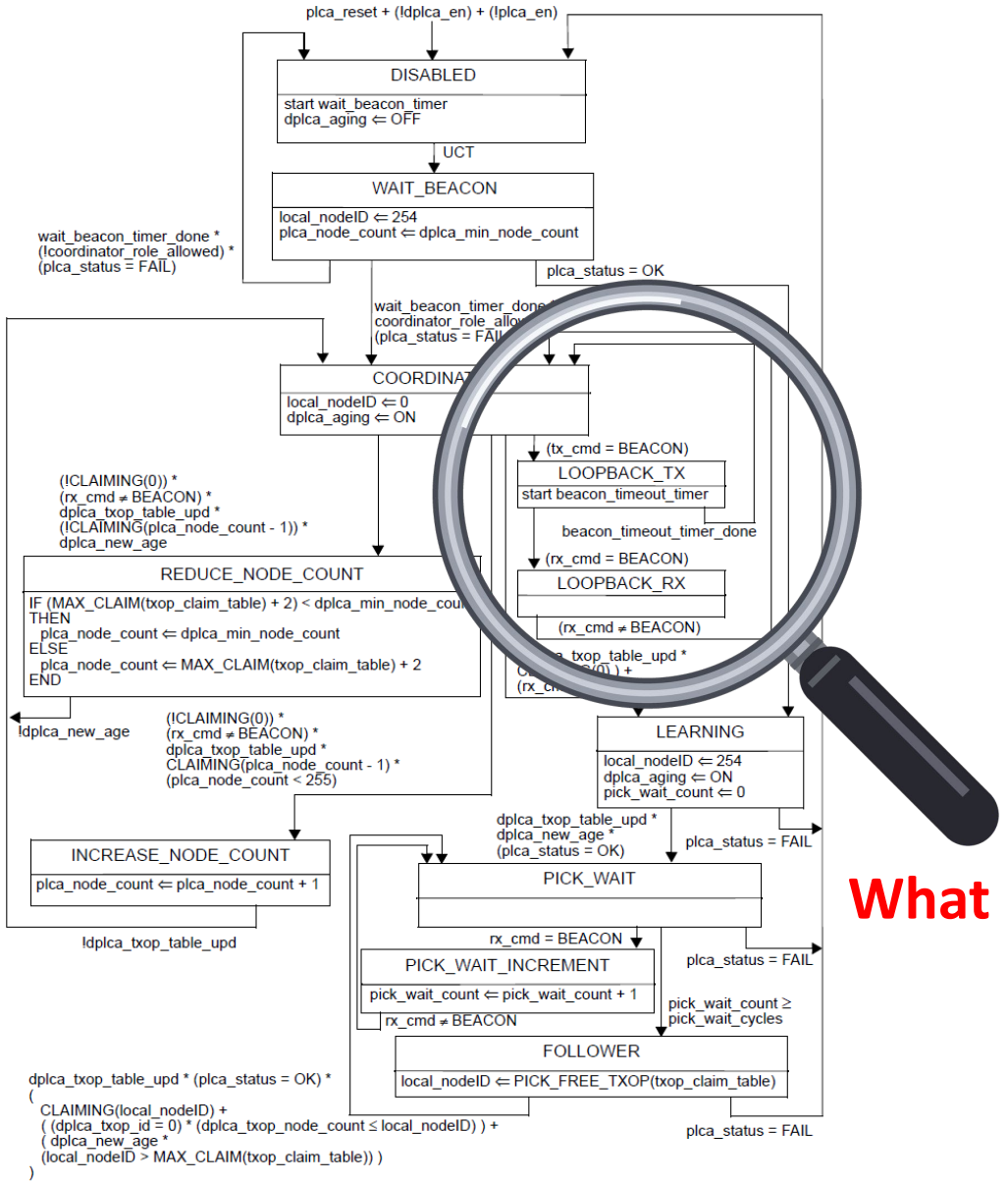


Figure 148–8—D-PLCA Control state diagram

What is all this in here?

D-PLCA Control State Diagram - Oddities

This portion of the state diagram works around the fact that the PHY receives the BEACONs that it transmits and we had to account for variable MII/PHY latency to resolve.

These MII/PHY timing corners are common in the PLCA state diagrams

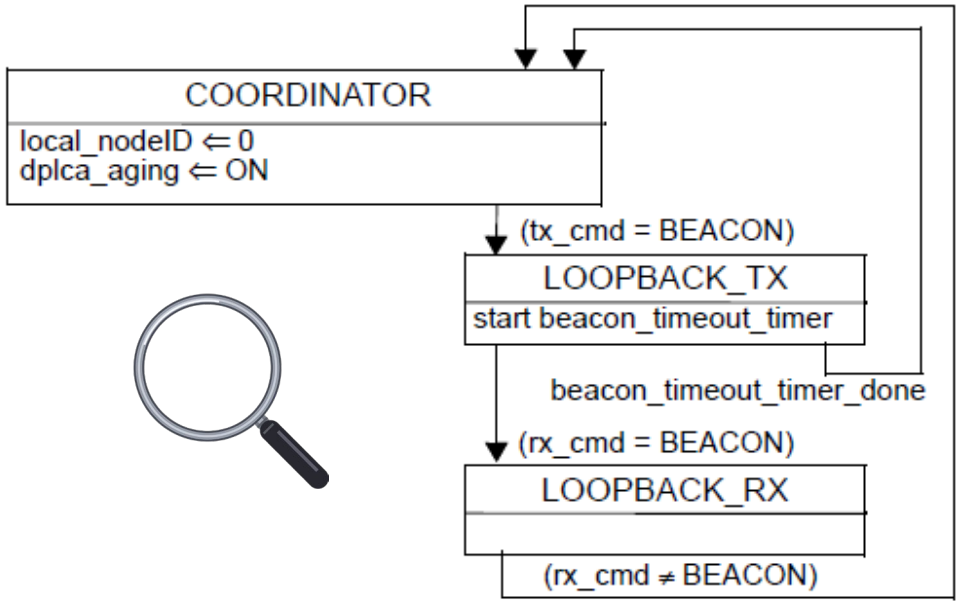
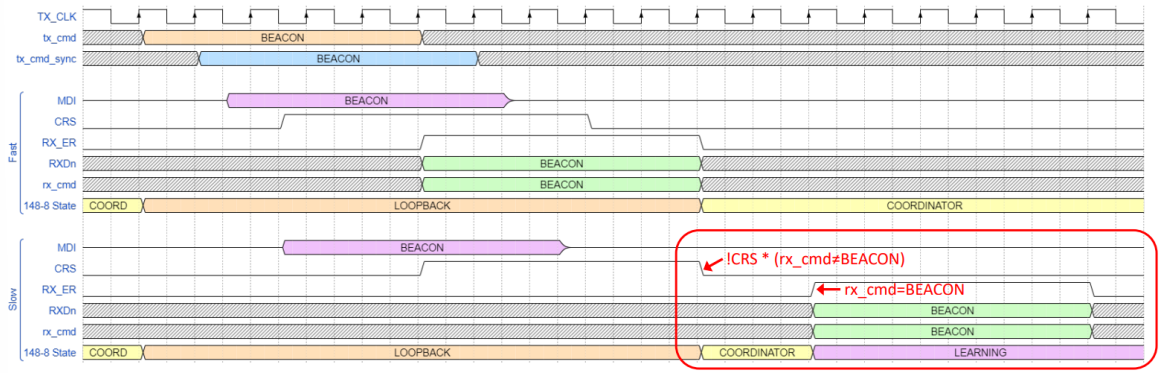
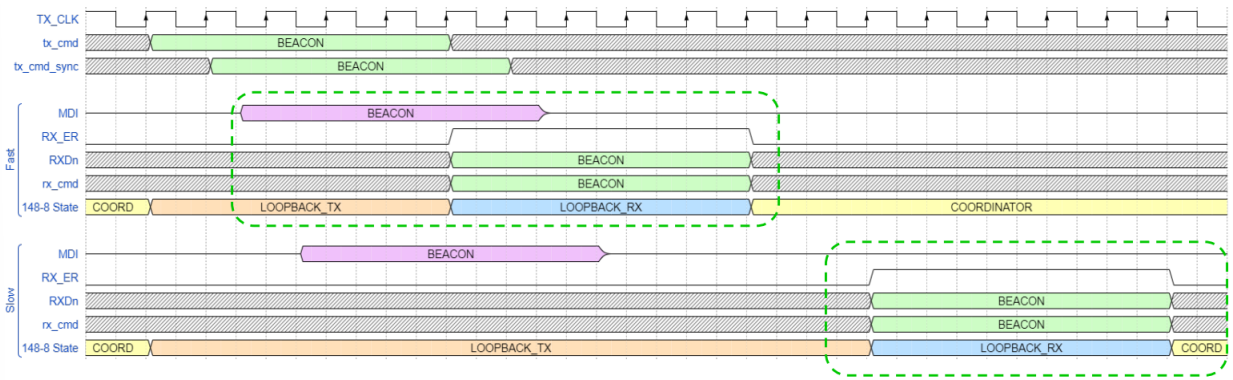


Figure 148–8—D-PLCA Control state diagram (excerpt)





https://www.ieee802.org/3/da/public/0525/Baggett_3da_Cmt47_DPLCA_Block_Own_BEACONs_v01.pdf

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Conclusions

- **Existing clause 147 and 188 PHY compatibility**
  - No changes, no new symbol encodings
  - No new PHYs in this task force
- **Constrain changes to Clause 148 (PLCA RS) and a service interface**
  - Don’t use MII to communicate priority class
  - Due to PLCA RS and MII/PHY timing complexity, we should follow the D-PLCA approach:
    - Keep changes to the existing PLCA state diagrams as minimal as possible.
    - Major changes should be kept as separate, new state diagrams.

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Thank You

Questions?