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Cyclic Traffic Requirements and the Time Axis in PLCA

Requirements, gap analysis, and existence proof
Contribution to the PAR, CSD and Objective discussion

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Three domains converge on the same requirement

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Three independent domains, three independent standards bodies, one shared property

- **The data is produced on a fixed period, and the payload is small**
  - None of these requirements is expressed as a priority.
  - All of them are expressed as a period.

Domain	Period	Payload per node per cycle
Automotive chassis control	1–100 ms, majority 2–100 ms	8–64 B (CAN / CAN FD heritage) → 64 B frame
Industrial isochronous control	1 μs – 1 ms range; 4 ms and 12 ms in cited use cases	bounded, constant per node per cycle
Robotics motion / tactile	1 ms; 125–250 μs recommended	30–200 B

Priority answers “who”. Periodicity asks “when”

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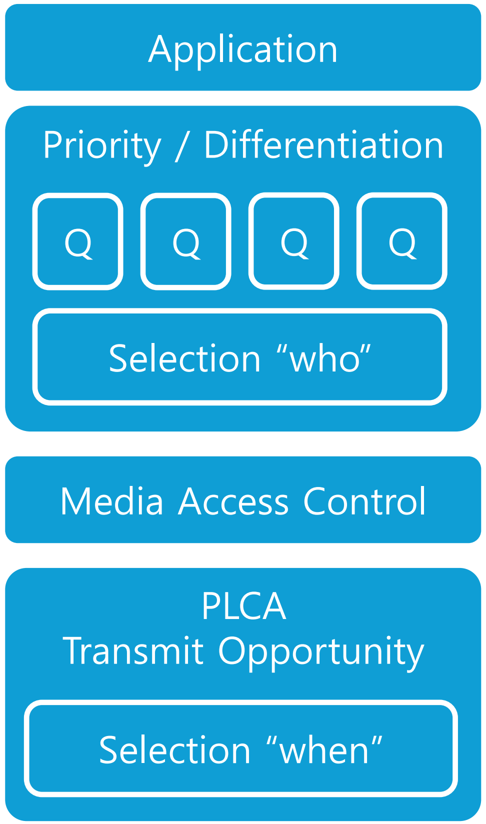
These are complementary requirements, not competing ones

- **Differentiation by class of service**
  - Reorders which pending frame is sent when an opportunity arrives
  - Effective for aperiodic, bursty contention
  - Addressed by the transmit-selection contributions already before this Study Group

- **Cyclic (periodic) traffic**
  - The frame is produced at a fixed phase; its value decays if the opportunity does not arrive near that phase
  - Raising a node's class of service does not move the instant its transmit opportunity arrives
  - That instant is a function of the node's position in the cycle and of the segment population

- **A frame at the highest class of service still waits for its position in the round robin**



The gap: the cycle length is the variable

The inter-BEACON interval varies with the number of transmitting nodes and with their frame sizes

- **Closed-form bounds**
  - 10BASE-T1S, $N = 8$, $R_b = 10$ Mb/s, $T_{beacon} = 2$ μs, $T_{commit} = 0.4$ μs, $O_{PHY} = 8$ B, $T_s = 3.2$ μs, $T_b = 10$ms

	L_max = 64 B standard PLCA	L_max = 64 B fixed period, m = 1	L_max = 1518 B standard PLCA	L_max = 1518 B fixed period, m = 1
Worst-case delay	0.524 ms	0.118 ms	10.99 ms	2.44 ms
Jitter bound	0.466 ms	0.055 ms	9.77 ms	1.218 ms

Standard PLCA worst case is a function of all N nodes. With a fixed period it is a function only of the m preceding nodes.

Consistent with figures already before this group: 8 stations / 1536 octets → 9.83 ms and 8 stations / 256 octets → 1.76 ms (CFI, slide 7)

A cycle count is not a time base

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An ordinal schedule inherits the variability of the cycle it counts

- **The approach already before this group**
  - Each node has parameters m_i and o_i, and may transmit when its TO is available and (cc_i + o_i) mod m_i = 0, where cc_i is a local cycle counter incremented on BEACON reception, with periodic reset by the coordinator
    - Jochim, Shazzad & Kim, IEEE 802.3 NEA Ad Hoc, 9 October 2025, slides 8 and 10

- **This establishes an ordinal axis. It does not by itself establish periodicity in time.**
  - The PLCA cycle length is not constant — it varies with transmitting nodes and frame sizes
  - Therefore "every m-th cycle" does not map to "every m × T seconds"
  - An application producing data every 1 ms is not synchronised to the cycle counter, so the phase between message release and grant instant continues to drift
  - Any add, move or change alters the mapping again — the concern the draft PAR raises in 5.5

- **A time reference is already present in this architecture — the draft objectives preserve the optional TSSI**

- **The ask is not a mechanism. It is that the objective state the target in units of time, so that any candidate can be measured against it.**

Existence proof, part 1: what is already on record

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The CFI presented four publicly available proprietary methods as existence proof

- **Three of the four operate on the time or repetition axis rather than on frame priority.** Feasibility of scheduled transmit opportunity assignment is therefore not in question before this Study Group — it is recorded in the CFI that opened it.
  - *Kim & Jochim, CFI Opening Report, IEEE 802.3 July 2026 Plenary, slides 28 and 39*

Method	Description recorded in the CFI	Axis
Modulo	Establishes a schedule that determines which PLCA ID can transmit in which cycle	repetition
Multi-ID	A node may hold several PLCA IDs and can therefore transmit more than once per cycle	repetition
Precedence	In each cycle only one PLCA ID transmits; the first ID that uses its TO ends the cycle	ordering
Skip-TO	A node can be configured to remain silent for n cycles once it has used a TO	repetition

Existence proof
part 2: analysis and simulation of a fixed time base

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Whether this axis can be quantified — data from one instance of the class the CFI recorded

- **Simulation setup**
  - OMNeT++ 6.2 with INET 4.5. Eight nodes, 10 Mb/s half-duplex multidrop. Two nodes carry 64-byte periodic control frames at 10 ms; six nodes carry 64-byte aperiodic background traffic with exponential inter-arrival. Offered background load 10 % to 80 %. 120 s per run, 10 runs per point.
- **Periodic control traffic, background load 10 % → 80 %**

Metric	CSMA/CD	standard PLCA	fixed period
Mean delay	0.207 → 144.2 ms	0.105 → 0.217 ms	0.089 ms, load-independent
Max delay	2.65 → 823.3 ms	0.270 → 0.469 ms	0.118 ms, load-independent
Mean jitter	0.160 → 17.01 ms	0.031 → 0.102 ms	0 measured
Max jitter	2.51 → 695.6 ms	0.195 → 0.381 ms	0 measured

Control overhead of the fixed-period initial phase, same parameters and a 10 ms period: 5.2 μs with all eight nodes active, 27.6 μs with all eight silent — roughly 0.05 % to 0.28 % of the cycle.

Analysis and simulation: Ahn & Park, Periodic PLCA: Deterministic and Bandwidth Efficient Medium Access for Ethernet Multidrop Networks, IEEE Access, 2026 [DOI.ORG/10.1109/ACCESS.2026.3732710]

Conclusion and Next Steps

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- **Conclusions**
  - Automotive chassis control, industrial automation and robotics each state their requirement as a period in time with small payloads. None of the three states it as a priority.
  - The PLCA cycle length is the variable, and an ordinal schedule built on the cycle counter inherits that variability.
  - Feasibility of time and repetition axis mechanisms is already recorded in the CFI, and the axis can be measured — load-independent within a stated sufficient condition, and a bound outside it.

- **What I am asking today**
  - Not for wording. Only that the group consider whether the time axis belongs in the objectives.

- **What we will do next**
  - Extend the evaluation to multi-rate periodic sources, mixed-criticality FIFOs within a node, and bursty arrivals — the cases where the property is a bound rather than a zero
  - Bring a node-count and period sweep to the deterministic-latency simulation work discussed in this group, so candidate mechanisms can be compared on a common basis
  - FPGA implementation and hardware-in-the-loop validation on 10BASE-T1S boards, including clock drift and guard-time behaviour

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" Thank you. "

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