Enhanced PLCA (EPLCA) – Technical Feasibility Study For Predictable Max Latency – Study3

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IEEE 802.3 PLCA Enhancements Study Group

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Feasibility Study-3

1. PCS Layer Change - 4B/5B encoding removal for data payload – ~25% Bandwidth/Latency gain
   – Keep the Beacon/Commit/Suspend/Wake and other special packets same
   – Keep the Data Frame starting/ending same and remove 4B/5B encoding for data payload alone
   – Provide additional Length information for fail safe parsing.
2. Setting Up EPLCA Latency Improvement Expectations
3. PLCA and CSMA/CD Interop Issue/Limitation

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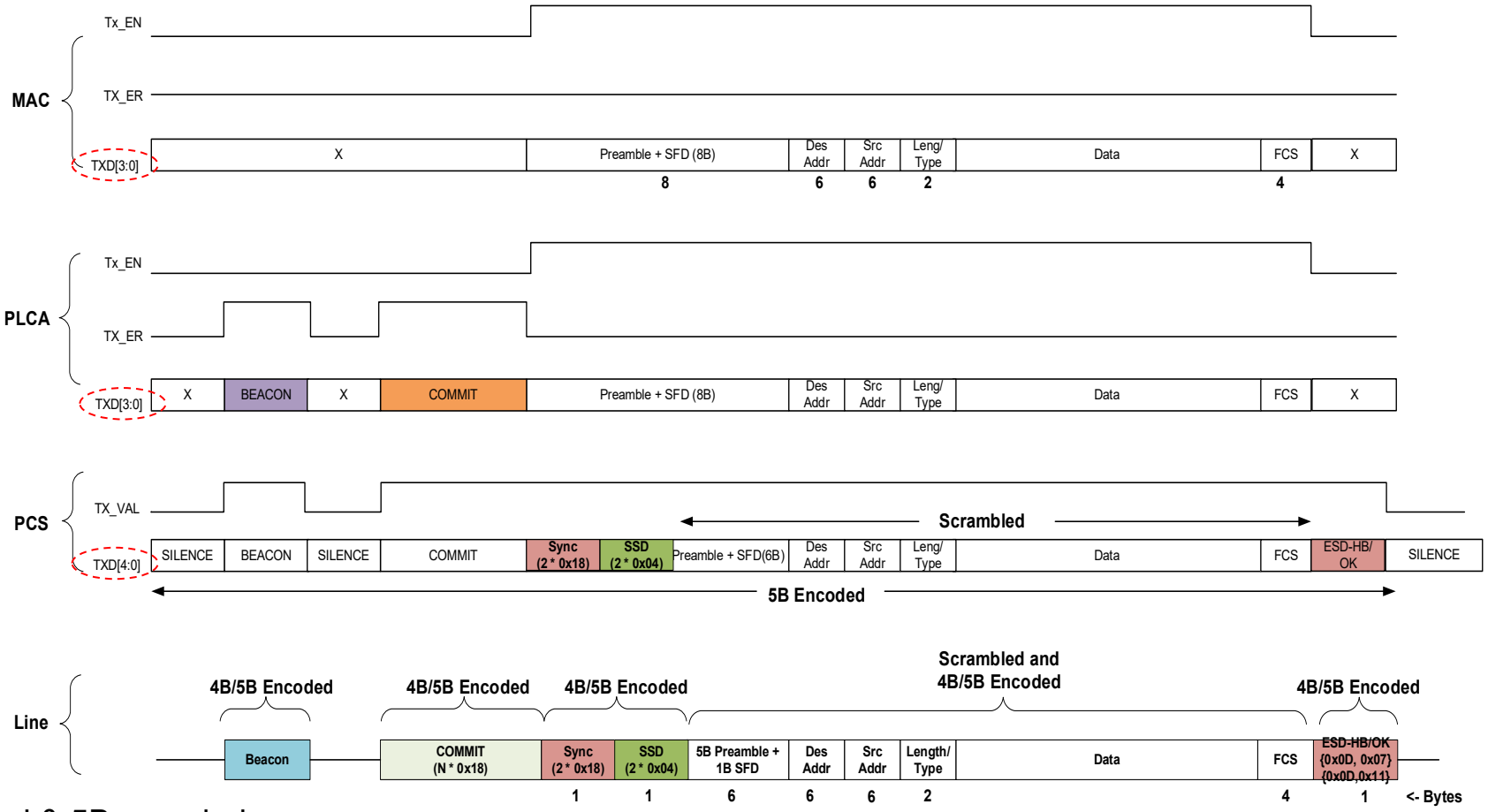
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Current Flow - MAC Data to PCS Output Data Conversion

- MAC: Preamble + Data:
  - 7 bytes of Preamble (7 * 0x55)
  - 1 byte of SFD (1 * 0xD5)
  - Data
- PLCA:
  - Adds Beacon + Commits
  - MAC's Preamble + Data
- PCS – 5B/Scramble
  - Sends Beacon
  - Sends Commit
  - Sends MAC's Preamble + Data
    - 1 byte SYNC (2 * 0x18) – 5B encoded
    - 1 byte SSD (2 * 0x04) – 5B encoded
    - Remaining 5 bytes Preamble – scrambled & 5B encoded
    - 1 bytes of SFD – Scrambled & 5B encoded
    - Data – Scramble & 5B encoded
    - 1-byte ESD-HR/OK/ERR ({0x07 * 0x07} or {0x0D, 0x07} or {0x0D, 0x11}) - 5B encoded



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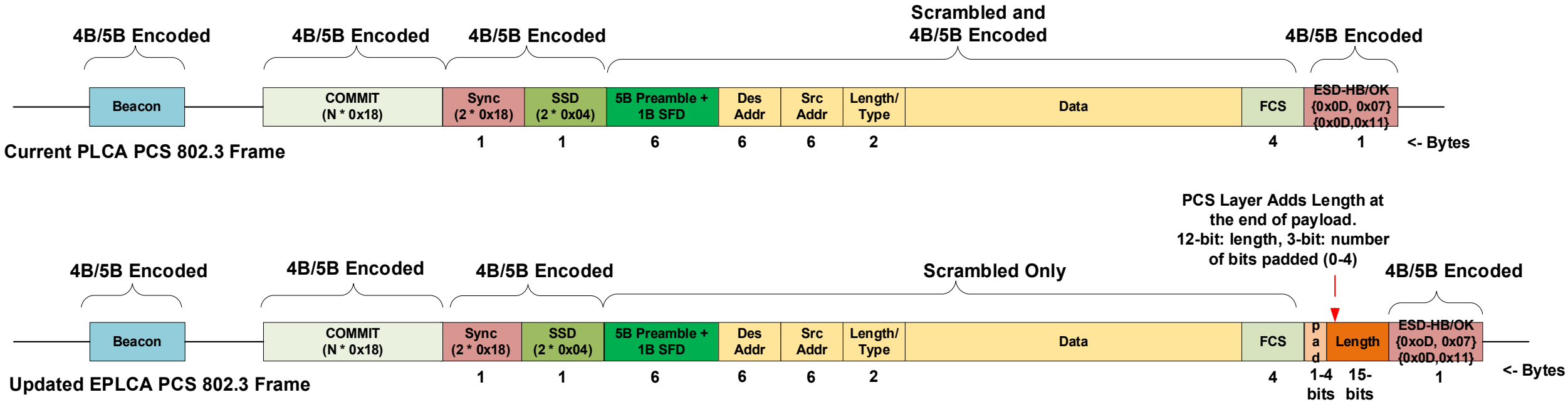
PCS Layer Change – 4B/5B encoding removal for data payload

- Currently the 4B/5B encoding adds 25% bandwidth overhead (We are getting only 10Mbps even though the PHY is running @12.5Mbps)
- NumPLCANodes indicates number of PLCA/CSMA-CD devices – Details in Feasibility Study-2 presentation (https://www.ieee802.org/3/EPLCA/public/261001/subramaniam_eplca_01c_261001.pdf)
  - Enable this feature only when NumPLCANodes=0
  - If all the devices in a Zone are EPLCA, then this feature is enabled to improve bandwidth/latency
- Unlike highspeed PHYs which are continually locked, the half-duplex 10BASET1S line goes idle between frames
  - Frame locking is requirement is less stringent with 10BASET1S than with high-speed SERDIES
  - Even if we miss a packet, locking to the next packet after IDLE is easier (~ed)?
  - Data payload is already scrambled for DC balancing/clock-recovery
- 4B/5B encoding removal for data payload alone solution is less disruptive than 64B/66B or 128B/132B encoding which are used in high speed always locked unidirectional PHYs.

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PCS Layer Change – 4B/5B encoding removal for data payload

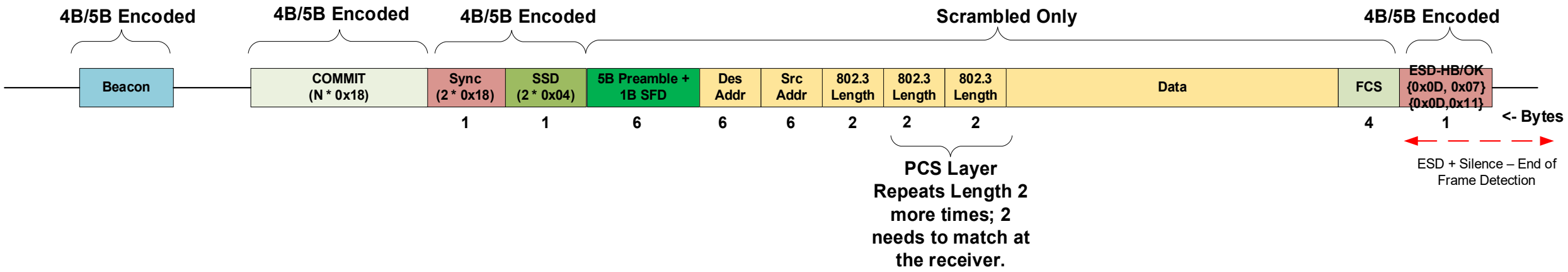
- Keep the Beacon/Commit/Silence/Suspend/Wake/SSD and other special packets and symbols same as in PLCA (4B/5B encoded and non scrambled)
- PCS Layer Addes “Length” information at the end of the Payload
- Scramble the data payload and Length and no 4B/5B encoding of data payload and length.
  - PCS receiver parser uses the “Length” and ESD to identify end of frame.
    - PCS can also check the additional FCS field for end of frame detection; makes it more robust.
- The PCS Receiver Layer will strip the Length fields



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PCS Layer Change – 4B/5B encoding removal for data payload

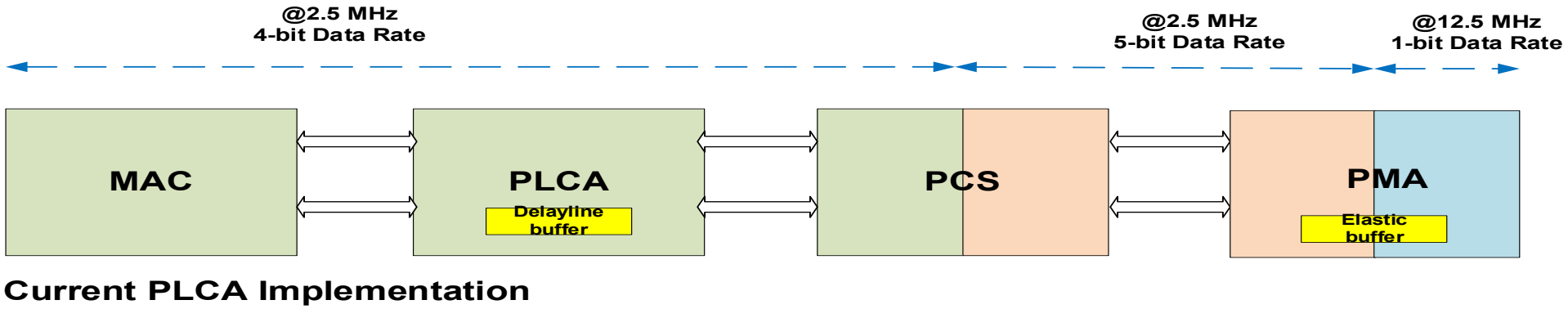
- Other options looked at to detect end of Frame – But less effective (Informative)
  - Use the length information in the 802.3/IP4/IP7/IEE1722 AVTP packets and count the bytes received to look for end of Frame. Also repeat the length 3 times for fail safe parsing
    - PCS Layer becomes more protocol dependent
    - The length information in the protocol may not be visible when encryption is used?
  - Since 10BASET1S is half duplex, we have IDLE/SILENCE at the end of frame, we can also use it to match the end of frame
    - We could stop supporting burst in EPLCA; also helps latency predictability

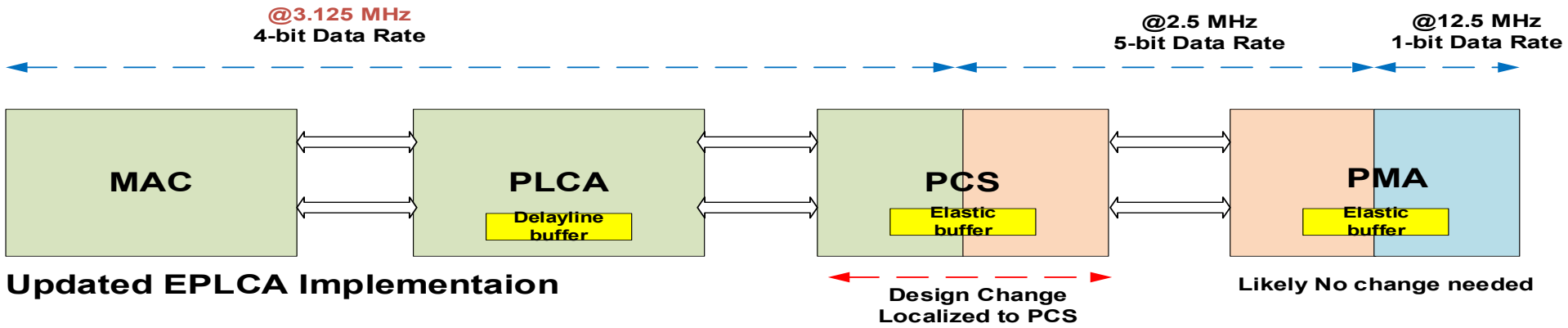


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PCS Layer Change – 4B/5B encoding removal for data payload

- The 4-bit Interface Data Rate is @3.125 MHz and the 5-bit Interface Data Rate is @2.5MHz
- Need to have a small FIFO/Elasticity-Buffer both in Tx/Rx direction in the PCS layer
  - Due to insertion/removal of Length information
  - Special 4B/5B encoded Packets/Framing symbols coming at 3.125 MHz
    - May have to drop extra COMITTs or handle it differently to avoid FIFO getting full.





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PCS Layer Change – 4B/5B encoding removal for data payload

- Pros
  - Changes are localized to PCS layer
  - No change in the PHY, MII interface, or other layers to support this; compared to using 64B/66B or 128B/132B
- Cons:
  - The bandwidth/latency improvement is disabled when interoperating with exiting PLCA devices.
  - Changing the MAC/PLCA MII clock from 2.5 MHz to 3.125MHz needs additional design changes and end of Frame detection is slightly more complex

- Additional Future Enhancement Request outside of PLCA:
  - The MII Interface can be enhanced to provide Length Information to make the future enhancements easier
  - The MII Interface can have Valid/Ready handshake for every data beat to make future enhancement easier.

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Setting Up Correct EPLCA Latency Improvement Expectation

- This video is already referring EPLCA; and the expectation is, EPLCA is to going to improve latency
  - https://www.youtube.com/watch?v=d4TPchoMA4A
- EPLCA expectation needs to be set correctly - Use case examples needs to be provided
  - The latency depends on the application, data rate, and data size
    - If one does bursts and large packet transfers, there is no latency improvements/predictability expected
    - EPLCA specification likely need to limit packet-size for latency predictability
  - PLCA Cycle period is not fixed, depends on the number of nodes – Example: USB/1394/Bluetooth/etc. Protocols have fixed time scheduling cycle
    - EPLCA specification likely need to limit maximum PLCA cycle period for latency predictability (for Non-Best-Effort Traffic)
  - Cyclic traffic definition will help to reduces the chances of multiple Nodes doing traffic all at the same time, there by improves latency
    - Does not improve latency if all the nodes need to transfer on every PLCA cycle or latency requirement is 1 PLCA cycle.
  - The data rate requirement for applications keeps increasing compared to traditional older CAN applications. 10BASET1S will not meet the new application requirements due to 10Mbps limit
    - Example: High-Definition (HD) Matrix Systems Headlights: Jumping from roughly 100 pixels to 65,536 individual micro-LEDs per vehicle; data rate requirement for Headlights is changing from 19.2 Kbps to 100+ Mbps
  - Interop: PLCA and DPLCA Interop will likely remove the EPLCA benefits

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PLCA and CSMA/CD Interop Issue/Limitation

- PLCA specification seems to have CSMA/CD interop limitation
  - PLCA Spec does not set Packet-Pending/CRS during CSMA/CD collision causing more retries
    - Fix: Set Packet-Pending/CRS during Media collision
  - PLCA Spec does not handle multiple MAC backoff retry scenarios
    - Fix: Extend Packet-Pending/CSR till maximum backoff retry time (52.8ms) and don't clear it on next PLCA cycle if there is no MAC Tx request
- Error Scenario Observed:
  1. The 1st Tx transfer in PLCA typically starts with collision and retry due to TO!=NodeID and FIFO getting full; Packet-Pending/CRS are set
  2. During 2nd retry, a CSMA/CD device also transmits and collides; Packet-Pending/CRS are not set during this collision.
  3. Since CRS was not set, the MAC retries 3rd time when TO!=NodeID and this causes FIFO-Full collision; Packet-Pending/CRS are set
  4. On the next PLCA cycle, when TO=NodeID, CRS is set to "0". Because of multiple retries, the MAC retry timer has increased and it does not request Tx transfer. Packet-Pending at the end of the TO is cleared and CRS is already cleared.
  5. The MAC retries again 4th time when TO!=NodeID, and this causes FIFO-Full collision; Packet-Pending/CRS are set,
  6. This can go on multiple times, and all the 15 MAC retries exhaust and transfer fails.

1.Delayline FIFO-Full Collision	2.CSMA/CD Device Collison	3.Delayline FIFO-Full Collision	4.No Tx Request As MAC Retry Timer is greater than PLCA cycle	5.Delayline FIFO-Full Collision
1st time Tx Request: TO != NodeID **Packet-Pending=1 CRS=1**	**Next PLCA Cycle TO = NodeID CRS=0;** **2nd time Tx Request:** **Collison Happens on Media Packet-Pending=0 CRS=0**	**3rd time Tx Request: TO != NodeID** **Packet-Pending=1 CRS=1**	**Next PLCA Cycle TO = NodeID CRS=0;** **No Tx Request from MAC as the retry timer is larger than PLCA cycle** **Packet-Pending=0 CRS=0**	**4th time Tx Request: TO != NodeID** **Packet-Pending=1 CRS=1**

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Backup



Reference Presentations

- RCP with 10BASE-T1S Latency Considerations – Colt Correa, Intrepid
  - https://www.youtube.com/watch?v=d4TPchoMA4A
- Microchip - AN1120 Ethernet Theory of Operation
  - https://ww1.microchip.com/downloads/en/AppNotes/01120a.pdf

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Backup – 4B/5B Encoding

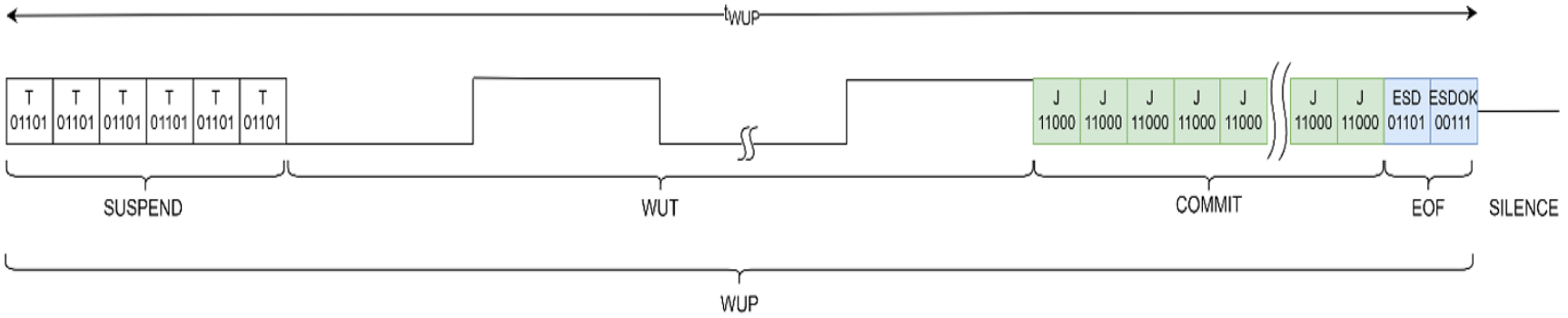


Table 23–1—MII interface signals

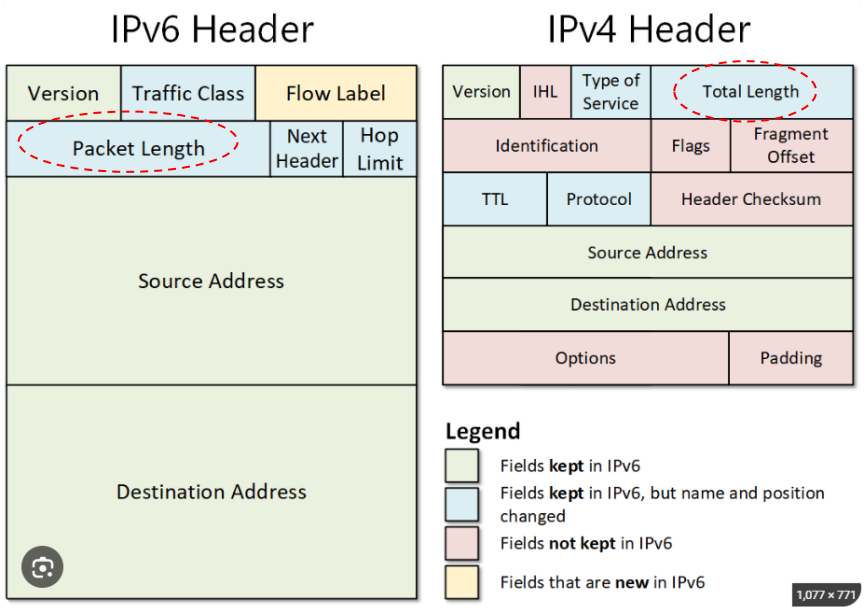
Signal name	Meaning
TX_CLK	Transmit Clock
TXD<3:0>	Transmit Data
TX_ER	Forces transmission of illegal code
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<3:0>	Receive Data
RX_DV	Frames Receive SFD and DATA
RX_ER	Receive Error Indication
MDC	Management Data Clock
MDIO	Management Data

Table 147–1—4B/5B Encoding

Name	4B	5B	Special function
0	0000	11110	—
1	0001	01001	—
2	0010	10100	—
3	0011	10101	—
4	0100	01010	—
5	0101	01011	—
6	0110	01110	—
7	0111	01111	—
8	1000	10010	—
9	1001	10011	—
A	1010	10110	—
B	1011	10111	—
C	1100	11010	—
D	1101	11011	—
E	1110	11100	—
F	1111	11101	—
I	N/A	11111	SILENCE
J	N/A	11000	SYNC / COMMIT
K	N/A	10001	ESDERR
T	N/A	01101	ESD / HB
R	N/A	00111	ESDOK / ESDBRS
H	N/A	00100	SSD
N	N/A	01000	BEACON
S	N/A	11001	ESDJAB

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Backup – Ethernet II Frame Length Information



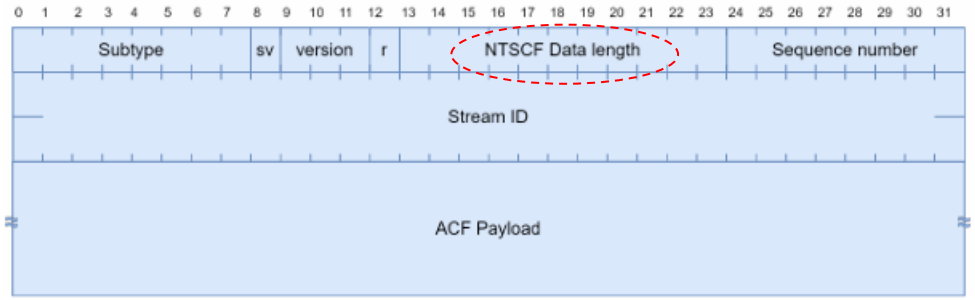


Fig. 2.7: Non-Time-Synchronous Control Format structure

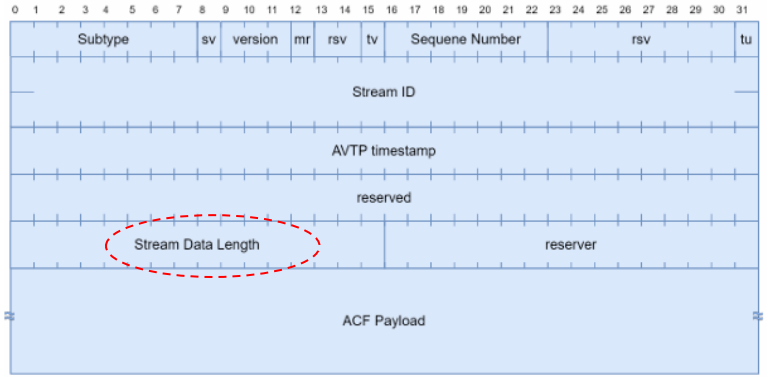
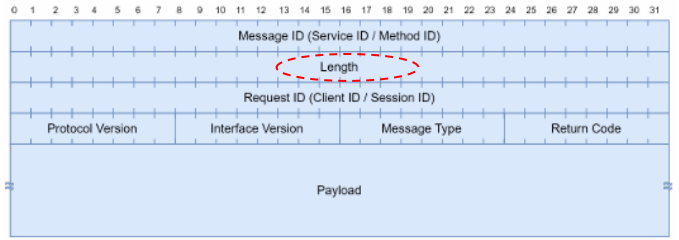
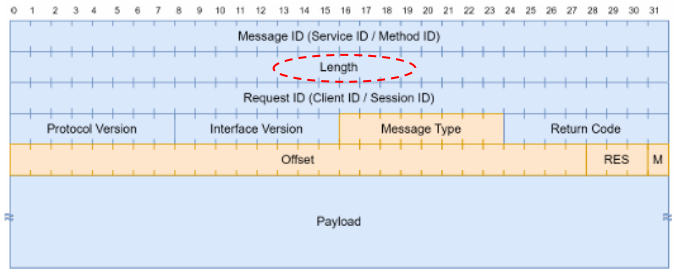


Fig. 2.8: Time-Synchronous Control Format structure



(a) Regular



(b) Transport Protocol

Fig. 2.13: SOME/IP header formats

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