Latency Objective for >10 Mb/s Long-reach SPE

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Purpose of this presentation

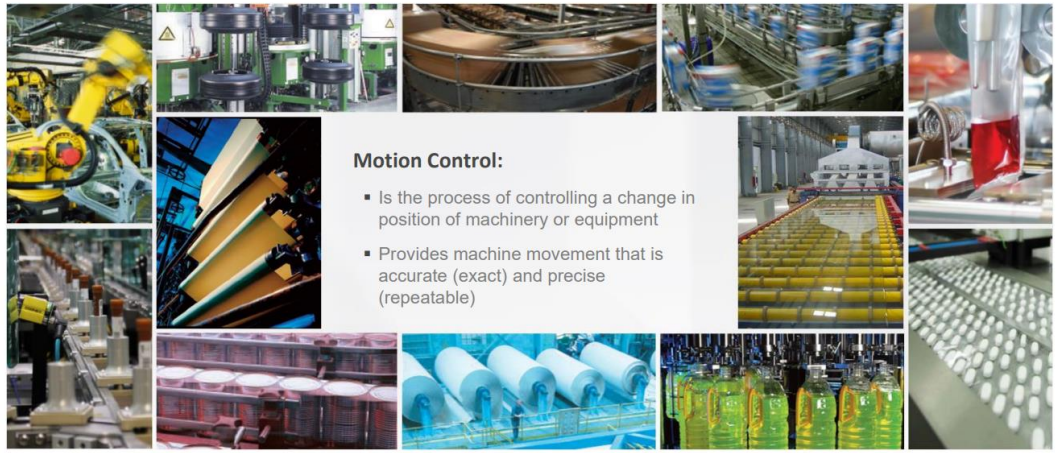
- Provide reasons why to specify the latency objective
- Propose the latency objective

Broad market potential

We should avoid the situation of excluding this big market potential of low latency industrial control applications because of no PHY latency objective

See more details in Dayin Xu's presentation: Use Case: Servo Drive Motor Communication

Motion Control Introduction



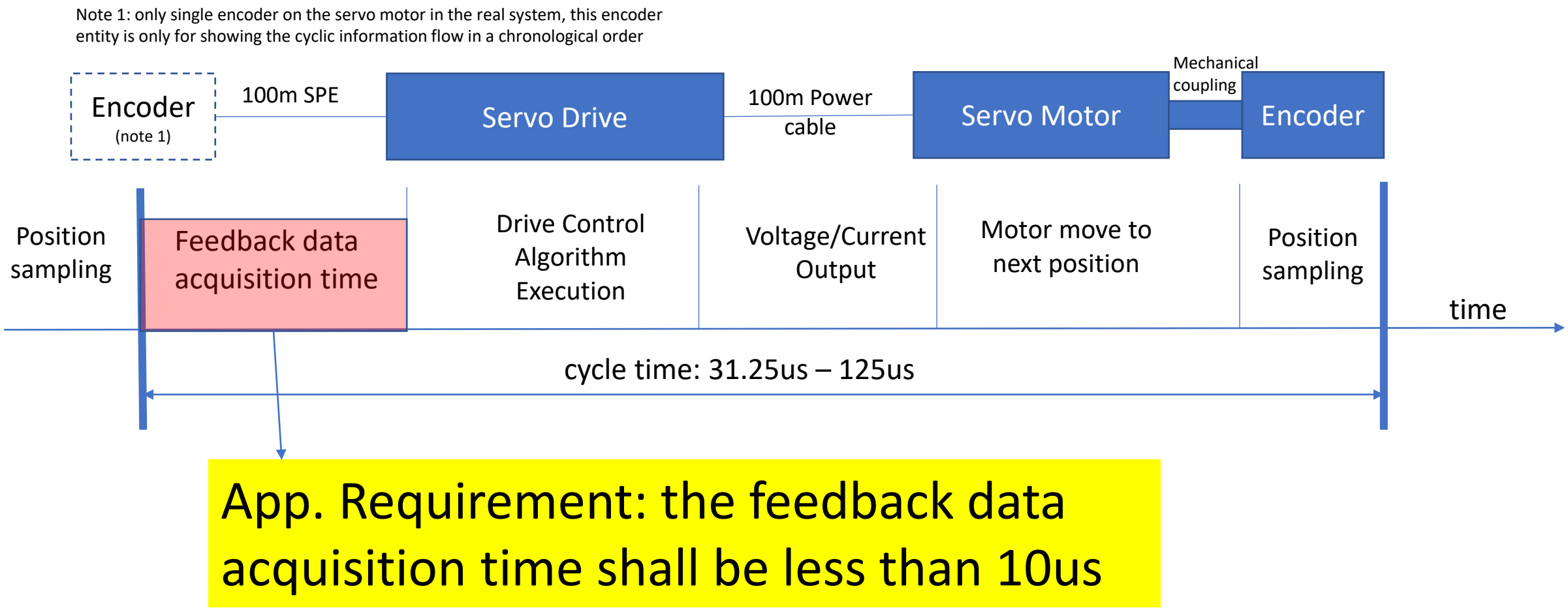
General Motion Control Market Size

- By Volume
  - General motion control servo drive: 2021 forecast unit shipment: 11,128,000
  - General motion control servo motor: 2021 forecast unit shipment: 14,054,000
- By Revenue
  - General motion control servo drive: 2021 forecast $4.1B
  - General motion control servo motor: 2021 forecast $4.5B

Src: IHS Markit, Motion Control Report - 2019

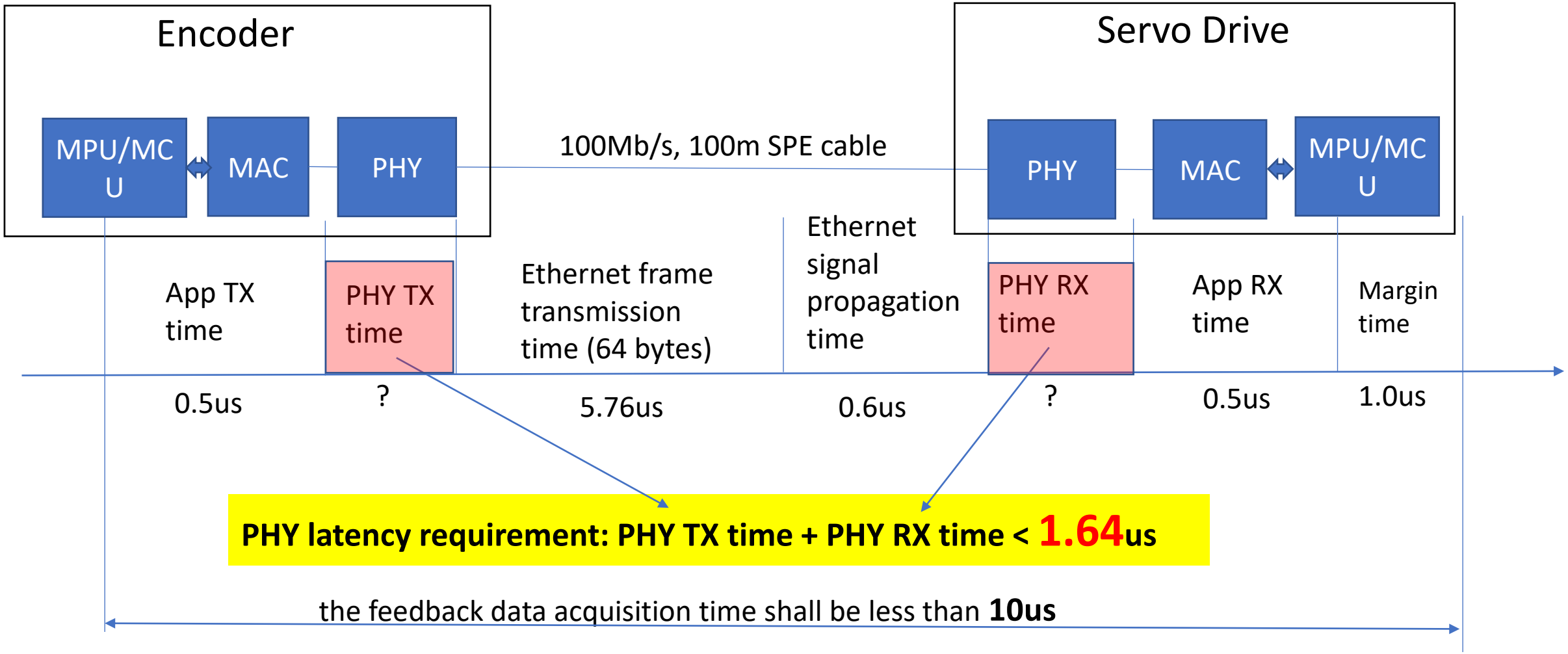
April 28, 2021 - D. XU IEEE 802.3 Pt-to-Pt SPE Enhancements Study Group 5

Servo motor control cycle time break-down



App. Requirement: the feedback data acquisition time shall be less than 10us

Feedback data acquisition time break-down



Specifying latency is not a new topic

- The latency has already been specified almost in all Ethernet PHY standards (e.g. 100BASE-T1 and 1000BASE-T1) , sometimes for a special purpose (e.g. MAC control PAUSE operation for 1000BASE-T1). It is not a new topic at all.

- High speed PHY (e.g. 1000BASE-T1, 10GBASE-T) has already shown the long latency issue because of using FEC, and therefore has lower throughput for close-loop applications. Attentions required since the study group is studying high speed PHY for industrial control applications!

96.10 Delay constraints 100BASE-T1

Every 100BASE-T1 PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than 360 ns. The delay for the receive path, from the MDI to the MII output, shall be less than 960 ns.

97.10 Delay constraints 1000BASE-T1

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 1000BASE-T1 PHY shall not exceed 7168 bit times (14 pause_quanta or 7168 ns). Transmit data delay is measured from the input of a given unit of data at the GMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the GMII.

Technical feasibility for “<=1.5us and 100m”

Latency spec in Dp83tc811 datasheet

		Min	Max	
TRANSMIT LATENCY TIMING				
T7.1	MII Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI	140	172	ns
	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI	304	372	ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI	322	382	ns
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI	134		ns
	Bit sequence 0b1101101000 to SSD symbol on MDI	401	440	ns
RECEIVE LATENCY TIMING				
T8.1	SSD symbol on MDI to MII Rising edge of RX_CLK with assertion of RX_DV	366	406	ns
	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV	434	513	ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV	438	525	ns
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL	385	417	ns
	SSD symbol on MDI to SFD (/S/) comprising bit sequence 0b1101101000	582	643	ns

897ns

895ns

RMII: Slave TX + Master RX = 897ns

RMII: Master TX + Slave RX = 895ns

100BASE-T1 PHY shows the technical feasibility of <1us TX+RX latency and 100m-200m reach with the shielded link segment under the industrial noisy environment.

One view of a path forward

- 100-200m short trunks and spurs with a reach extension to 100BASE-T1 (Cl 96) or similar technology
  - Minor modifications to existing standard
  - Consider needs of industrial, building & process automation vs. original target of automotive

SPE PHY : Measured Cable Reach with IEEE 802.3cg, IEEE 802.3bw PHYs

IEEE Standard	802.3bw 100Base-T1	802.3cg 10Base-T1L
Baud Rate	66.66MHz	7.5 MHz
Channel	1 pair UTP	Profibus Standard PA Cable
Modulation	PAM-3	PAM-3
Tx-PSD/VoD	Lower & Upper Mask	Lower & Upper Mask/Vod min/max limits 2.4V p2p/1V p2p
FEC	NA	NA
Equalization	Receiver Based	Receiver Based
Echo Canceller	Yes	Yes
IEEE Design Cable Reach	15m	1000m
Ethernet PHY	DP83TC811	DP83TD510E
Measured Cable Reach (Profibus PA Standard Cable)	100 meters+	2000 meters + (for both 2.4V p2p and 1V p2p)
TSN IEEE 802.3br SMD compliant	Yes	Yes

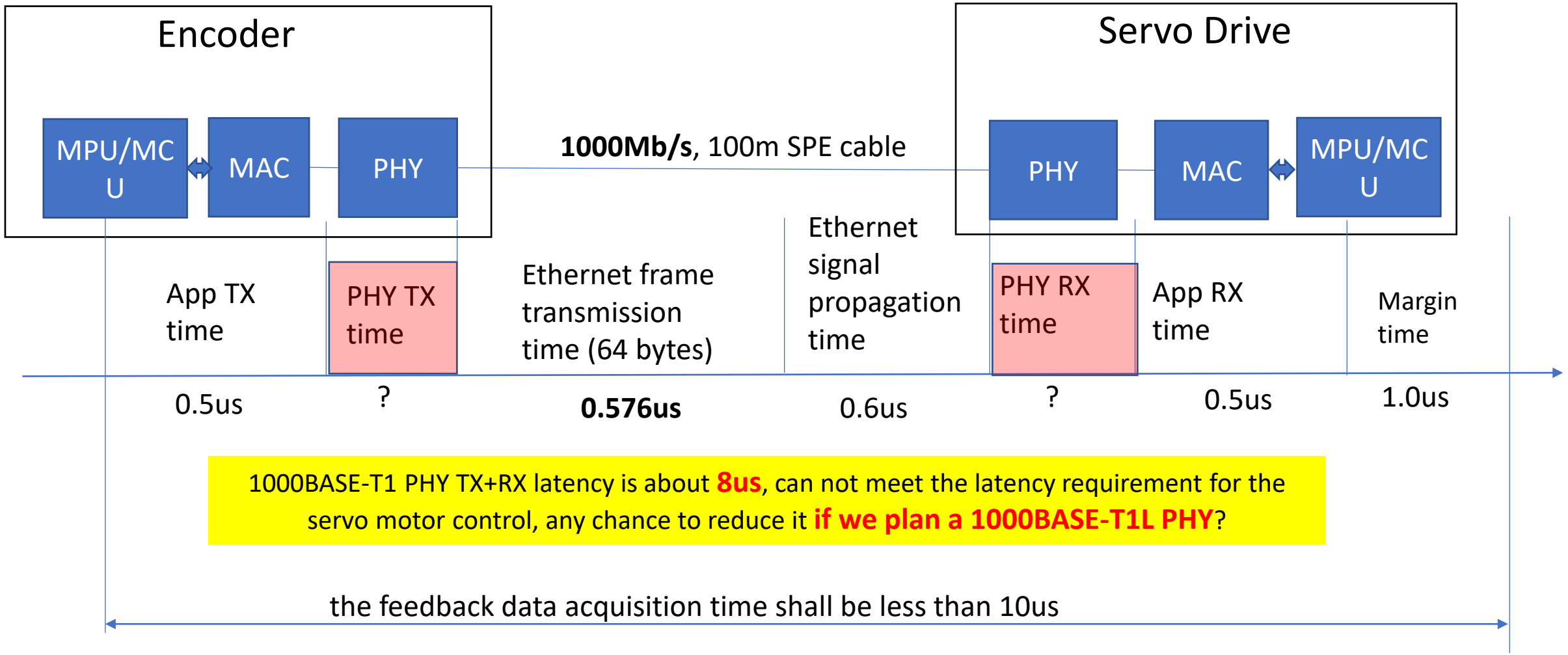
Technology exists with SPE PHY to reach the requirement of the long reach Industrial SPE 100M with appropriate noise and delay budgeting

Source: Geet Modi/Texas Instruments

3/9/2021 IEEE 802.3 Call for Interest Consensus Building 32

Src: IEEE 802.3 Single Pair Ethernet Enhancements Call for Interest Consensus Building

Is it technical feasible for 1000Mb/s?



The proposed latency objective for 100Mb/s

- **Do not preclude operation with latency (TX+RX) <= 1.5us when the reach is <=100m**

- With this objective, the 100Mb/s long reach PHY could be used for
  - Reasonable reach (e.g. 100m), low latency applications (e.g. servo motor control)
  - Long reach (e.g. 500m), higher latency applications (e.g. process automation trunk)

- The 100Mb/s PHY could be implemented with a configuration bit to disable FEC for low latency applications and enable FEC for long reach applications

Summary

- Propose the latency objective as **“Do not preclude operation with latency (TX+RX) <= 1.5us when the reach is <= 100m”** for 100Mb/s long-reach PHY

- Specifying latency properly will enable the broad market potential for those low latency industrial control use cases (e.g. Servo motor control)
- Specifying latency is not a new topic
- <=1.5us latency and 100m reach 100Mb/s SPE PHY is technically feasible according to the specification and test on the available 100BASE-T1 PHY

Thank You