Specification Gaps and Improvement of MDC/ MDIO Interface for Automotive Applications

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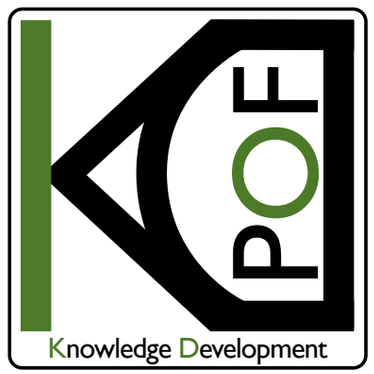
Supporters

- Seeking for supporters for interim meeting on May 2017



MDC/MDIO interface specification in 802.3

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Current specifications per 802.3 (I)

- Legacy MDIO interface speed is limited to 2.5 MHz (the minimum high and low times for MDC are 160 ns each, and the minimum period for MDC is 400 ns, per subclause 22.2.2.13)
- When MDIO is sourced by the STA, 10 ns of minimum setup and hold time referenced to the rising edge of MDC are defined in IEEE 802.3 subclause 22.3.4

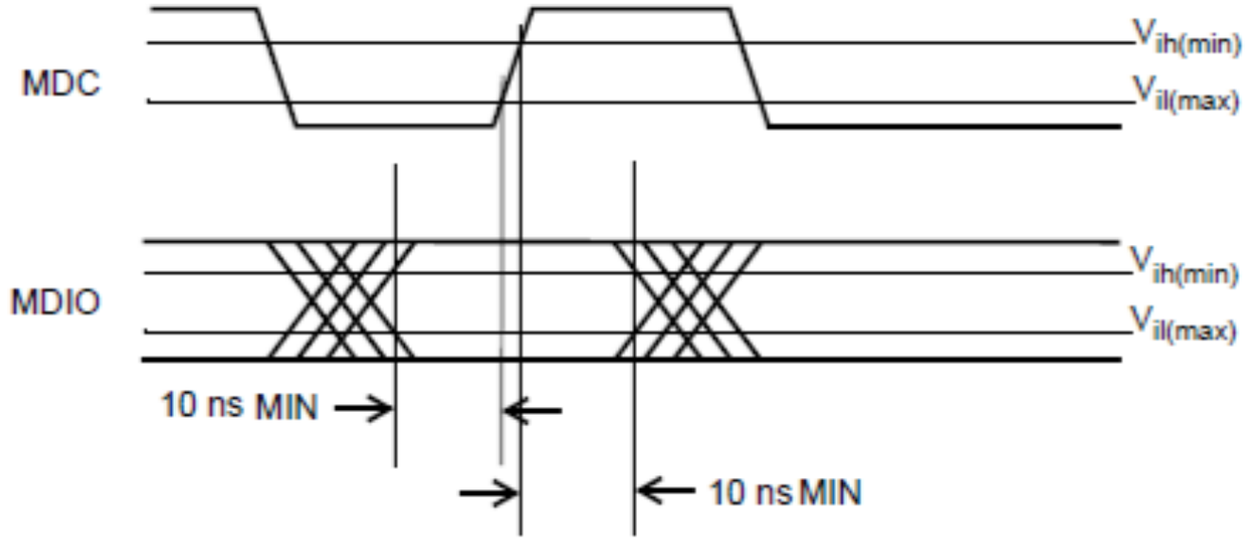

Figure 22–18—MDIO sourced by STA

- When MDIO is sourced by the PHY, a maximum clock to output delay of 300 ns is defined in IEEE 802.3 subclause 22.3.4

Current specifications per 802.3 (II)

- MDIO electrical interface specified in IEEE 802.3 subclause 45.4.1 is limited to devices operating at nominal supply voltage of 1.2 V, giving the following table for input and output high and low voltages and capacitance:

Table 45–223—MDIO electrical interface characteristics

Symbol	Parameter	Condition	Min.	Max.
V_{IH}	Input high voltage		0.84 V	1.5 V
V_{IL}	Input low voltage		–0.3 V	0.36 V
V_{OH}	Output high voltage	I_{OH} = –100 uA	1.0 V	1.5 V
V_{OL}	Output low voltage	I_{OL} = 100 uA	–0.3 V	0.2 V
I_{OH}[a]	Output high current	V_{OH} = 1.0 V		–4 mA
I_{OL}	Output low current	V_{OL} = 0.2 V	+4 mA	
C_i	Input capacitance			10 pF
C_L	Total capacitive load			470 pF

[a]I_{OH} parameter is not applicable to open drain drivers.

Industry implementations

Industry implementations

IC	Type	MDIO role	MDC typ freq (MHz)	MDC max freq (MHz)	Supported VDDIO (V)
Broadcom BCM8953x	Switch	Master	2.5	2.5	3.3
Broadcom BCM8953x	Switch	Slave		12.5	3.3
Broadcom BCM54612E	Phy	Slave		12.5	3.3, 2.5
Marvell 88E151x	Phy	Slave		12.0	3.3, 2.5, 1.8
Marvell 88E154x	Phy	Slave		12.5	3.3, 2.5, 1.8
Marvell 88E6131	Switch	Master	4.16	8.33	3.3, 2.5
Marvell 88E6131	Switch	Slave		8.33	3.3, 2.5
Marvell 88E6141	Switch	Master	(Not reported)	20.833	3.3, 2.5, 1.8
Marvell 88E6141	Switch	Slave		20.833	3.3, 2.5, 1.8
Marvell 88E6165	Switch	Master	4.16	8.33	2.5, 1.8
Marvell 88E6165	Switch	Slave		8.33	2.5, 1.8
Marvell 88E6171	Switch	Master	4.16	8.33	3.3, 2.5, 1.8
Marvell 88E6171	Switch	Slave		8.33	3.3, 2.5, 1.8
Marvell 88E6185	Switch	Master	4.16	8.33	2.5
Marvell 88E6185	Switch	Slave		8.33	2.5
Marvell 88E6320	Switch	Master	4.16	8.33	3.3, 2.5, 1.8
Marvell 88E6320	Switch	Slave		8.33	3.3, 2.5, 1.8
Microchip LAN8820	Phy	Slave		6.25	2.5
NXP SJA1105	Phy	SPI instead of MDIO			
Qualcomm AR8035	Phy	Slave		25	3.3, 2.5
Realtek RTL8211F	Phy	Slave		12.5	3.3, 2.5, 1.8, 1.5
Microsemi VSC8211	Phy	Slave		12.5	3.3, 2.5
Microsemi VSC8501	Phy	Slave		12.5	3.3, 2.5, 1.2

Misalignment between 802.3 and implementations

- There are many PHY implementations supporting MDC frequency > 2.5 MHz, which in principle is not an interoperability problem from 802.3 point of view
- There are Switch implementations supporting MDC frequency ≤ 2.5 MHz, which is 802.3 compliant
- There are Switch implementations that work with MDC in frequency ranges much larger than 2.5 MHz: this may be a potential interoperability issue from the point of view that in general any Switch implementation wants to be able to be connected to any PHY implementation
- For (at least) automotive applications where MDC/MDIO interface is implemented, the timing should be clearly standardized by the implementors of the different involved Ethernet ICs in an ECU
- The questions that should be answered are:
  - Is the timing of IEEE 802.3 Clause 22 (i.e. max 2.5 MHz) valid for the Automotive applications?
  - If higher frequency than 2.5 MHz is required, what is the maximum one?

Misalignment between 802.3 and implementations

- Switch and PHY implementations typically support VDDIO of 3.3 V and 2.5 V, and 1.8 V starts to be more common in more recent implementations
- Switch and PHY ICs cannot be connected if at least one common VDDIO level configuration is supported by both
- VDDIO of 1.2 V is not typically supported because same VDDIO is shared with high speed interfaces (e.g. RGMII) to reduce pin count. Larger voltage levels than 1.2 V are needed due to RGMII implementation
- The MDC/MDIO interface needs to be improved to be aligned with the real practices of the industry

Proposal

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Proposal (to solve the misalignment)

- To standardize high speed MDIO, if demanded by OEMs:
  - To speed up the MDIO interface by an integer factor of 5, preserving current specifications on minimum setup and hold time when MDIO is sourced by the STA
  - The factor of 5 is just an example that is also consistent with many implementations, however it may be considered different
  - If no high speed MDIO is decided to be standardized, all the Ethernet components to be used in an ECU should support MDC frequency of 2.5 MHz
- To support additional voltage levels:
  - Support of JEDEC JESD8C (3.3 V)
  - Support of JEDEC JESD8-5A (2.5 V)
  - Support of JEDEC JESD8-7A (1.8 V)

Proposal and affected 802.3 clauses (I)

- Subclause 22.2.2.13: MDC (management data clock)

22.2.2.13 MDC (management data clock)

MDC is sourced by the station management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

- Change MDC minimum period from 400 ns to 80 ns (reduction by a factor of 5)
- Change minimum high and low times for MDC from 160 ns to 32 ns (reduction by a factor of 5)
- That means a change in subclause 22.8.3.2 MII Signal functional specifications items SF34 and SF35.

Proposal and affected 802.3 clauses (II)

- Subclause 22.3.4: MDIO timing relationship to MDC

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the MII connector, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 22–19.

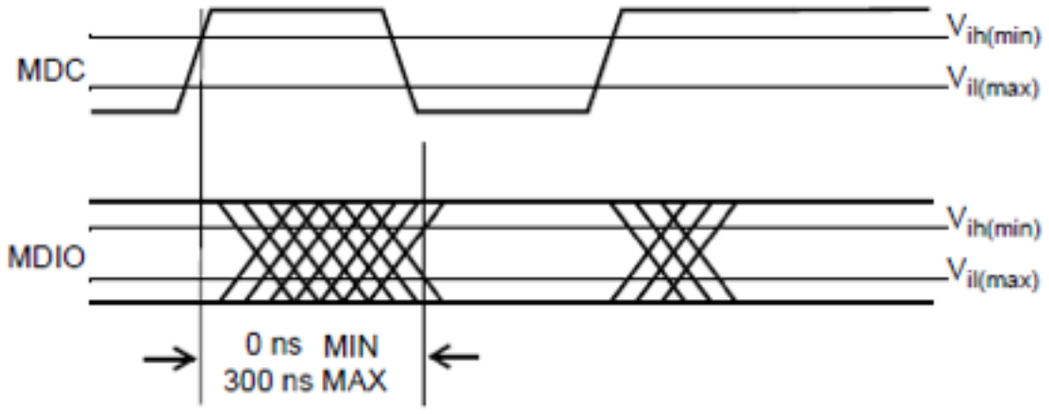

Figure 22–19—MDIO sourced by PHY

- Change clock to output delay from the PHY maximum from 300 ns to 60 ns (reduction by a factor of 5)
- That means a change in subclause 22.8.3.2 MII signal timing constraints item ST6

Proposal and affected 802.3 clauses (III)

- Subclause 45.4.2: Timing specification

When the MDIO signal is sourced by the MMD, it is sampled by the STA synchronously with respect to the beginning of the rising edge of MDC. The clock to output delay from the MMD, as measured at the STA, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 45–4.

The timing specification for the MDC signal is given in 22.2.2.13.

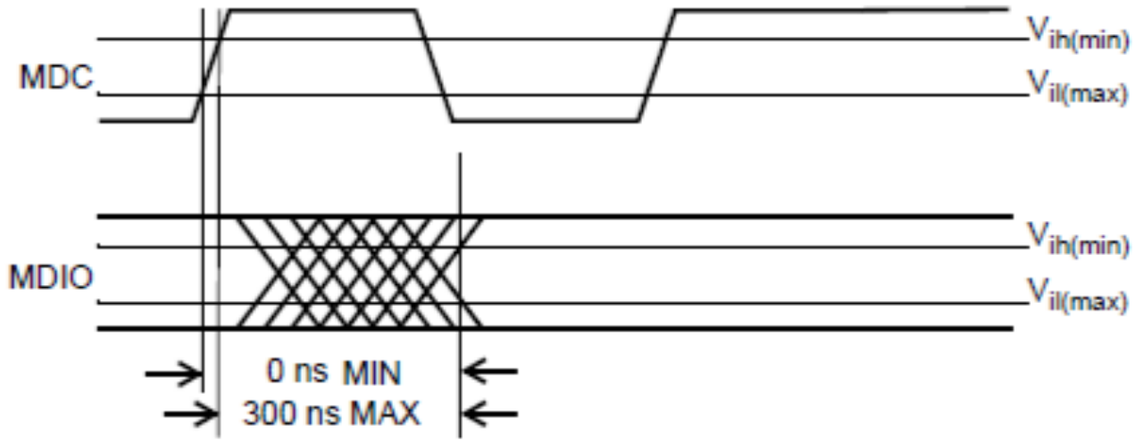

Figure 45–4—MDIO sourced by MMD

- Change the maximum clock to output delay from the MMD from 300 ns to 60 ns (reduction by a factor of 5)
- That means a change in subclause 45.5.3.20 Signal timing characteristics items ST2, ST3 and ST4.
- Minimum setup and hold time when MDIO sourced by STA does not change

Proposal and affected 802.3 clauses (IV)

- Subclause 45.4.1: Electrical specification

Table 45–223—MDIO electrical interface characteristics

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V_{IH}	Input high voltage		0.84 V	1.5 V
V_{IL}	Input low voltage		–0.3 V	0.36 V
V_{OH}	Output high voltage	I_{OH} = –100 uA	1.0 V	1.5 V
V_{OL}	Output low voltage	I_{OL} = 100 uA	–0.3 V	0.2 V
I_{OH}[a]	Output high current	V_{OH} = 1.0 V		–4 mA
I_{OL}	Output low current	V_{OL} = 0.2 V	+4 mA	
C_i	Input capacitance			10 pF
C_L	Total capacitive load			470 pF

[a]I_{OH} parameter is not applicable to open drain drivers.

- Add three new subclauses with the voltage and current values from JEDC JESD8C, JESD8-5A and JESD8-7A
- Change the input capacitance to 5pF to cope with new high speed MDIO (if agreed).
- Change total capacitive load to 165 pF to cope with new high speed MDIO (if agreed).
- That means to add in subclause 45.5.3.21 Electrical characteristics items and change items EC5 and EC6
- Add voltage translators extensions described in 45A.3 and 45A.4

Summary

- A summary of MDC/MDIO interface specification per 802.3 has been provided
- Some examples of industry implementations are also summarized and the misalignment with 802.3 specification highlighted
- Some interoperability issues that can arise if the MDC/MDIO interface specification is not improved are also explained
- A proposal to improve MDC/MDIO interface is given, consisting on:
  - To standardize a high speed MDC/MDIO, if higher speeds than 2.5 MHz are needed
  - To support additional voltage levels