NG-EPON Architecture
Initial Thoughts

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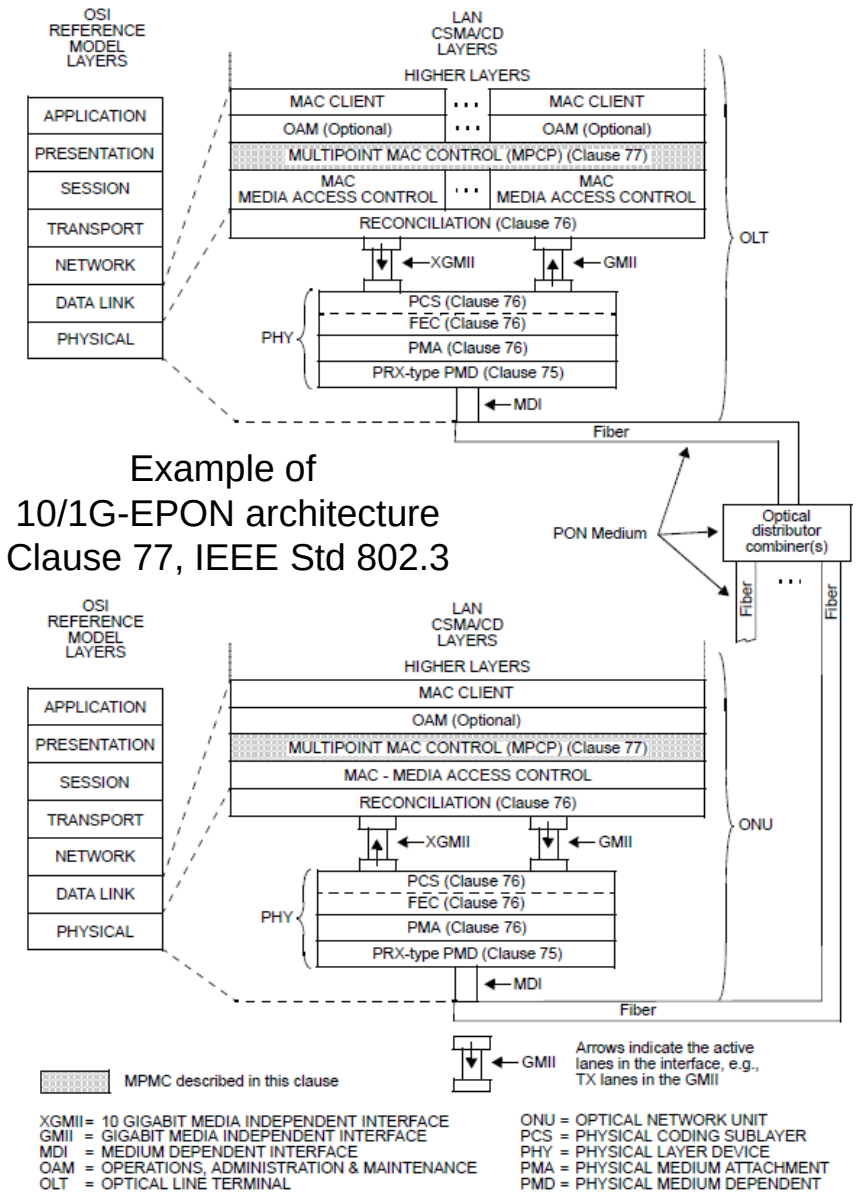
Architecture of EPON (today)



Example of 10/1G-EPON architecture Clause 77, IEEE Std 802.3

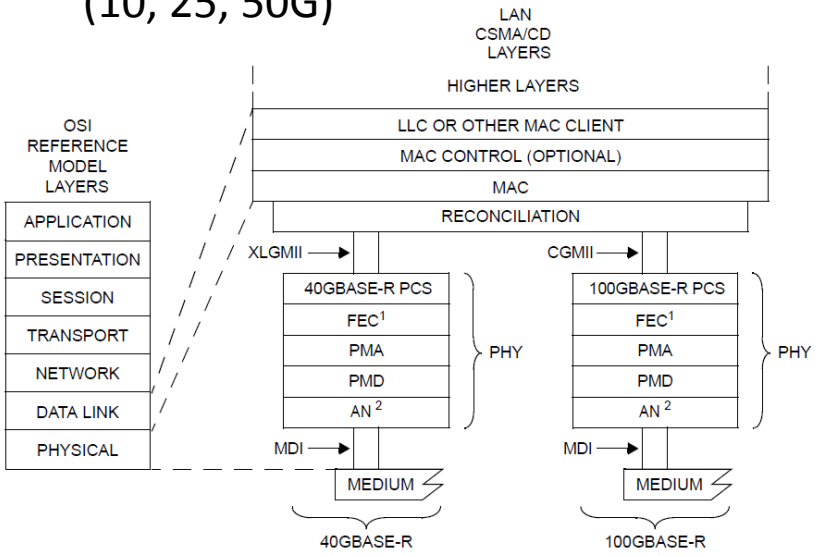
- Multi Point Control Protocol (MPCP) defined in Clause 77 (10G) / 64 (1G)
- Physical Coding Sublayer (PCS) defined in Clause 76 (10G) / 65 (1G)
- Physical Medium Dependent (PMD) defined in Clause 75 (10G) / 60 (1G), including MDI and ODN requirements
- Extensions to Reconciliation Sublayer (RS) to support P2MP defined in Clause 76 (10G) / 65 (1G)
- (X)GMII, MAC, OAM, and higher layers defined in other Clauses in 802.3/802.1
- Details on dual-rate OLT receiver architecture in Annex 75A

Architecture of NG-EPON

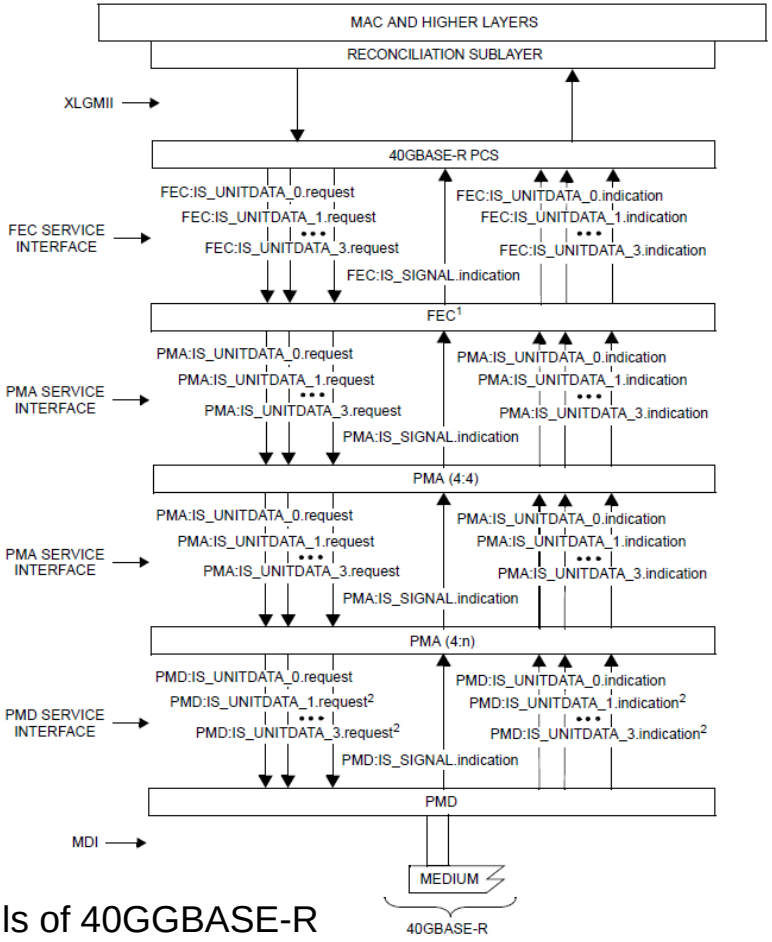
- The main building blocks for NG-EPON will remain the same:
  - MPCP in control of station discovery, registration, timing, ranging, and bandwidth allocation
  - MAC responsible for serialization / deserialization of data and framing
  - RS responsible for P2P emulation over P2MP medium
  - PCS responsible for coding data from MAC into medium-specific format
  - PMD responsible for delivering encoded data across medium (fiber)
- There will be some changes as well, depending on technical choices taken by the future Task Force:
  - MPCP might need to support multiple wavelengths (wavelength allocation, bandwidth allocation across different lanes, etc.)
  - PCS might need to support data striping across multiple lanes, insert alignment markers, encode data for non-OOK modulation, etc.
  - PMD might need to support multiple data lanes (wavelengths) across a single MDI, etc.

Example of multi-lane architecture

- 802.3ba (40GE/100GE) introduced the concept of multi-lane system, with “extensible architecture”
  - The primary building blocks are the same as in EPON (less MPCP)
  - PCS, PMA, and PMD are designed around the concept of data lanes. The number of data lanes depends on aggregate data rate (40/100G) and data rate per lane (10, 25, 50G)



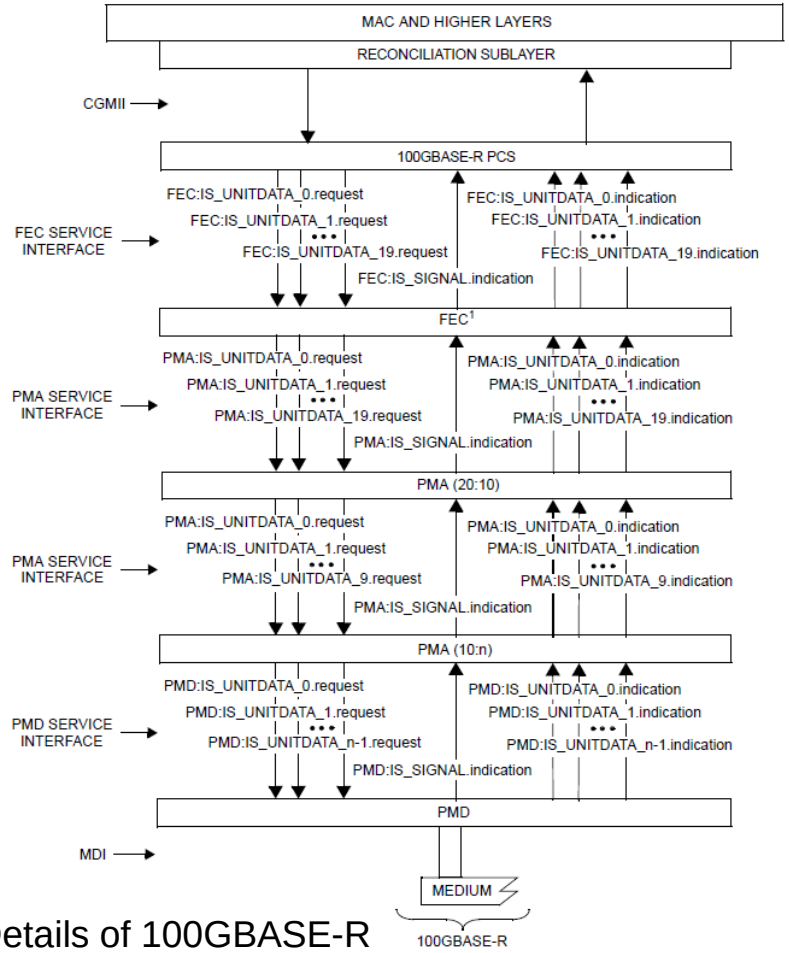
40G/100GBASE-R architecture



Details of 40GGBASE-R with focus on 4x10G lanes

100GBASE-R

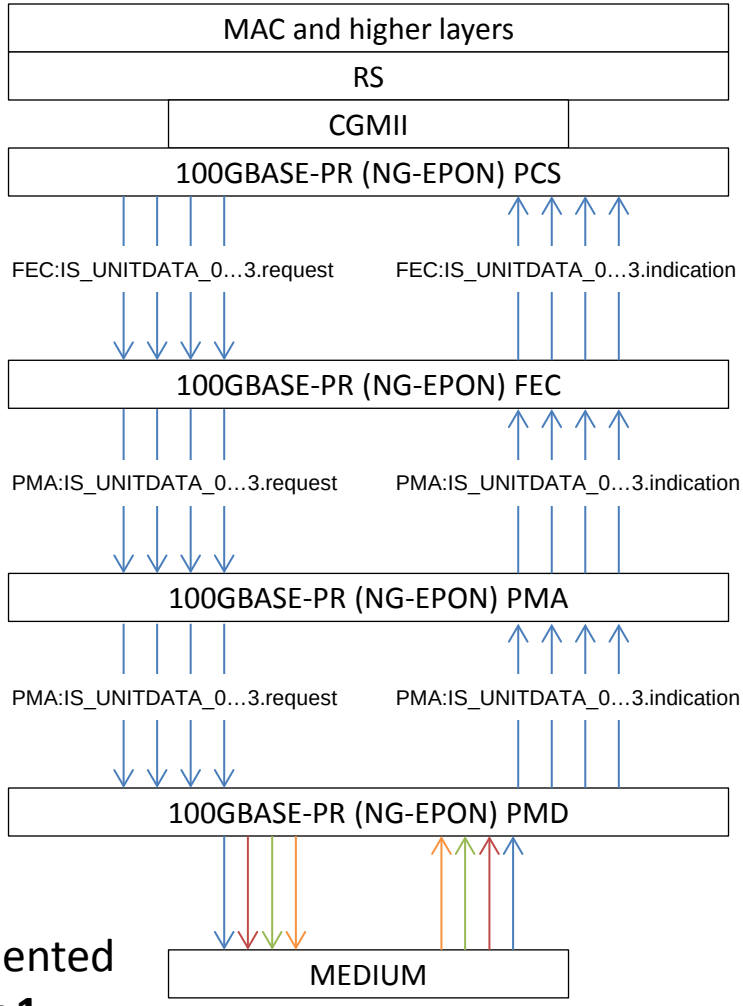
- 100GBASE-R supports multiple lane counts: 10x10, 4x25, etc.
  - PCS and FEC sublayers operate on 20x5G parallel data streams
  - PMA-PMA (CAUI) interface performs gearbox of 20x50G to 10x10G streams
  - 10x10G streams are then converted into n×kG streams, where number (n) and data rate (kG) per stream depend on specific PMD
- The same design approach is used for 400GE (P802.3bs), underway today
- Similar architecture could be used in NG-EPON to support data rates up to 100Gbps (or more, if needed)
  - Scalability is limited only by number of parallel lanes used in the architecture and implementation challenges



Details of 100GBASE-R with focus on n×kG lanes

100GBASE-PR (NG-EPON)

- Provided that 25GBASE-PR becomes available under NG-EPON project (single lane, operating at 25G)
  - 25GBASE-PR PCS could be extended to use the same approach as in 100GBASE-R
  - Up to 100G of data (in 25G increments) is received from MAC across CGMII
  - PCS encodes received data into 1, 2, 3, or 4 parallel 25G streams (depending on target aggregate data rate)
  - PMA performs any gearboxing needed
  - PMD delivers resulting streams across MDI and onto the medium
- A single architecture could support data rates from 25G to 100G
  - Individual lanes could be disabled, if needed
  - Drawback – the whole PHY has to be implemented **<u>to support the maximum data rate from day 1</u>**



100GBASE-PR specification

- STEP 1: design 1-lane 25G EPON PHY, including
  - Extensions (as needed) to MPCP, new PCS, PMA, and PMD
- STEP 2: design multi-lane 100GBASE-PR architecture and reuse as much of IEEE Std 802.3ba as possible:
  - CGMII per Clause 81
  - PCS derived from Clause 82 / 76
  - PMA derived from Clause 83 / 76
  - PMD derived from Clause 84 / 75
  - Extend MPCP from STEP 1 to support multi-lane architecture
  - Control for disabling individual lanes
  - Requirements for discovery of ONU capabilities, number of supported data lanes, data striping, etc.
- Work on STEP 1 and STEP 2 could be done in parallel
  - STEP 1 done by 25G PHY group
  - STEP 2 done by 100G Architecture group

100GBASE-PR caveats

- The OLT PHY will be complex from day 1, supporting data rates from 25G to 100G, depending on number of enabled lanes
- ONU complexity depends on number of lanes that it needs to support (listen to / transmit on)
- No way to support 1-lane and 4-lane ONUs on the same ODN:
  - all ONUs have to support the same number of lanes to work correctly (lowest common denominator)
  - ONUs can be equipped with fixed number of lanes and need to be replaced every time aggregate data rate is increased per PON **or** support multiple lanes from day 1 and disable some of them.
- No way to selectively stripe data, e.g., one packet is striped on 1 lane, and next packet is striped on 4 lanes.
  - Packet destination information loses relevance once it is passed across CGMII into PCS/PMA/PMD. All packets are treated equal beneath MAC

THANK YOU!