



50 Gb/s PAM4 transmission with InGaAs 25G VCSEL

Rubén Pérez-Aranda
rubenpda@kdpof.com

Introduction



- This contribution shows experimental results of 50 Gb/s transmission using PAM4 scheme with InGaAs 25G VCSEL (TRUMPF VCSEL-ULM850-25-TT-V03), between -40°C and $+125^{\circ}\text{C}$, for technical feasibility assessment
- This contribution is NOT a technical proposal for using PAM4 scheme for 50 Gb/s
 - Other different transmission schemes can also be feasible for same data-rate
- This contribution does NOT pursue including 50 Gb/s within the OMEGA project objectives
 - Use cases demanding 50 Gb/s should be presented by OEMs also including WHEN they are expected
- VCSEL devices with different oxide aperture diameters have been tested for several substrate temperatures (-40 , $+25$, and $+125^{\circ}\text{C}$)
 - See “perezaranda_OMEGA_02c_1119_InGaAs_25G_VCSEL.pdf”
- Based on Shannon’s capacity analysis and simulation models, the receiver sensitivity and the link budget have been calculated and are presented
 - See “perezaranda_OMEGA_04a_1119_LinkBudget.pdf” for reference
 - Link budget is only reported in the worst case: $T_s = +125^{\circ}\text{C}$ (substrate)
- Comparison between 25 Gb/s and 50 Gb/s in terms of VCSEL current density, RIN requirement and link budget is provided



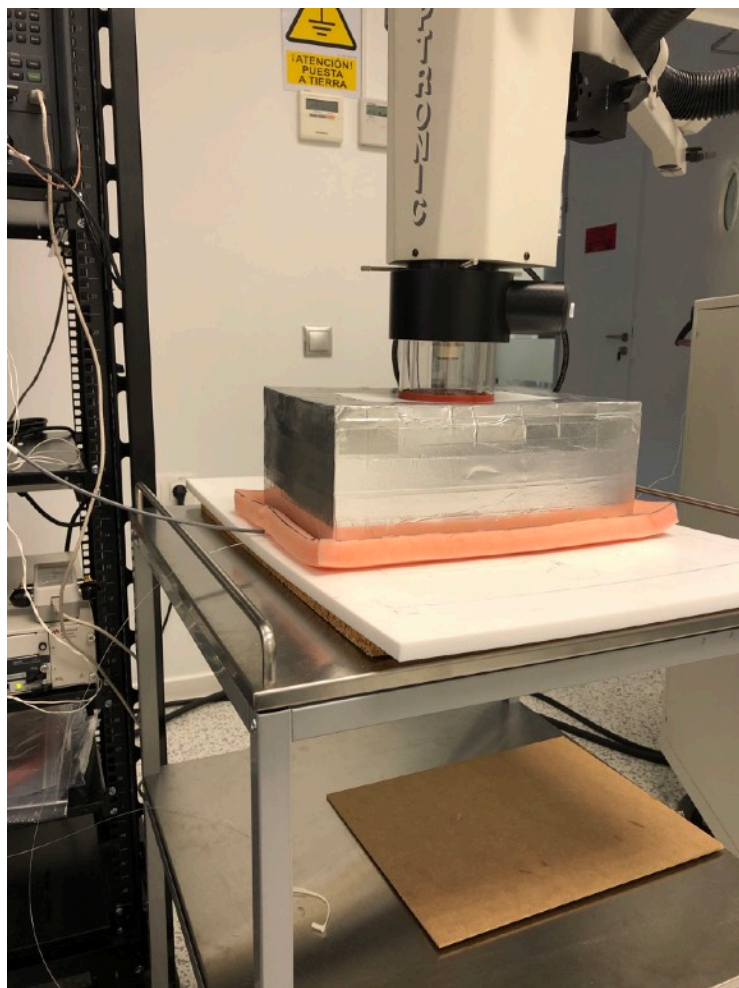
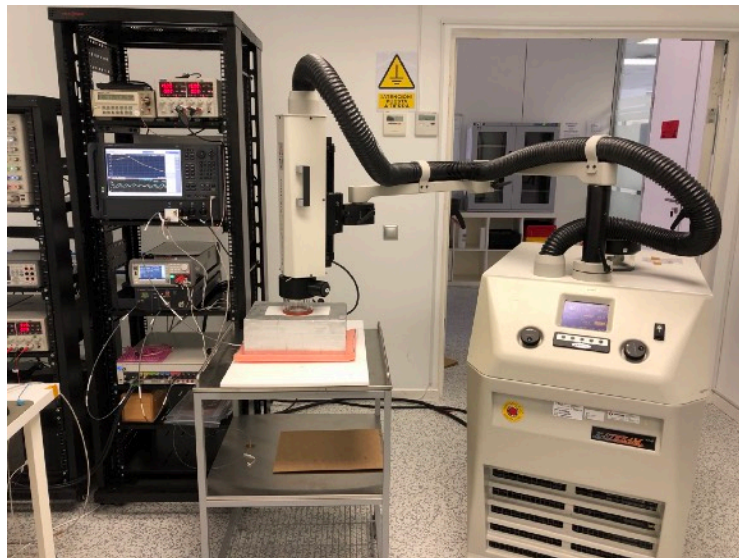
50 Gb/s transmission experiments

Equipment & Software



- Marki Microwave BTN-0040 bias tee (40 kHz to 40 GHz)
 - Used to combine bias current with RF signal from VNA or AWG
- Minicircuits TMP40-3FT-KMKM+, temperature stable 2.92mm cable, 40.0 GHz
 - Used to connect bias tee output to the DUT
- Keysight B2901A Precision Source/Measure Unit
 - Bias current to VCSEL
 - Voltage drop measurement (V-I curve)
- OFS HCU-MF050T 50/200/230 GiHCS fiber, 2 meters
 - Used for AC and time-domain characterization
- Keysight M8195A 65 GSa/s, 25 GHz, Arbitrary Waveform Generator
 - Used to generate time-domain RF signal that drives the VCSEL
 - Capability of real-time digital signal processing with 8 bits DAC
 - Used to provide symbol clock to oscilloscope
- Keysight N1092C DCA-M Sampling Oscilloscope (one optical and two electrical channels)
 - Used to make the time-domain characterization with periodic arbitrary signal generated by VCSEL
- Keysight N1010A FlexDCA Sampling Oscilloscope Software, R&D package
- Matlab 2018a:
 - Test automation
 - Signal processing
 - Model extraction
 - User operator extensions for N1010A

Tests setups

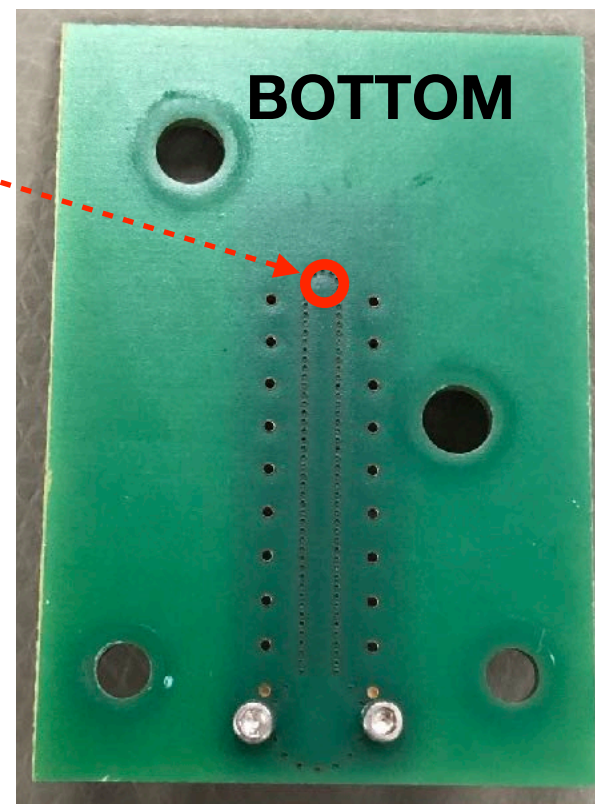


DUT

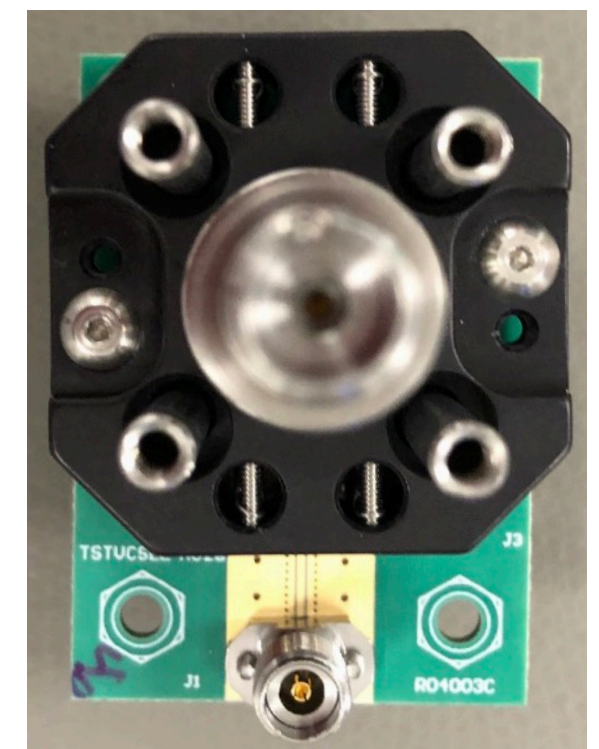
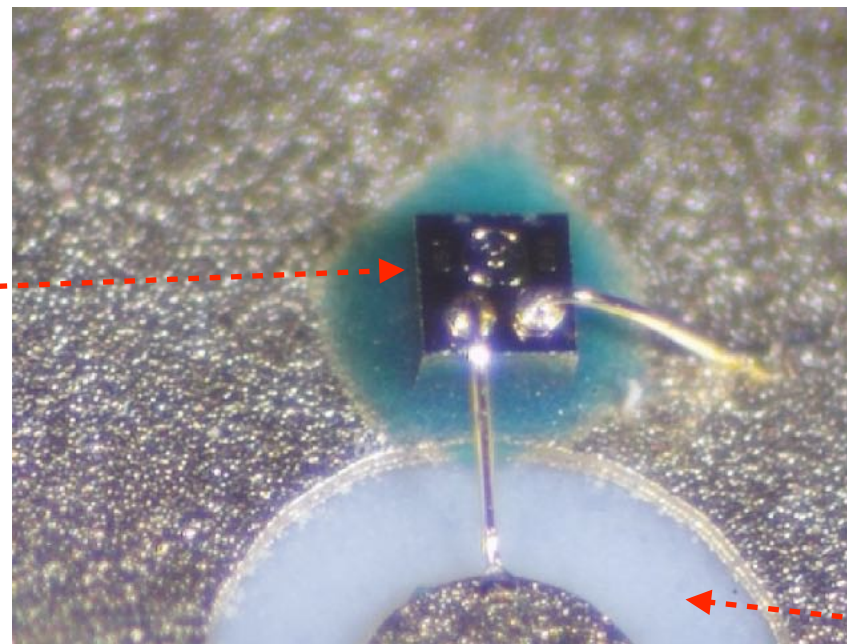
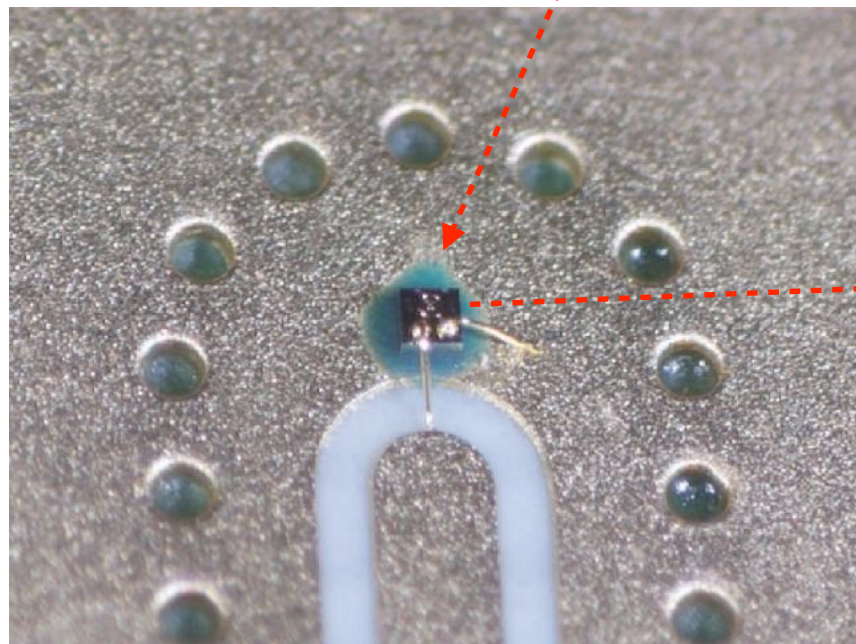


Thermo-couple
attachment point

VCSEL



X-Y adjustable
collimator with FC
connector



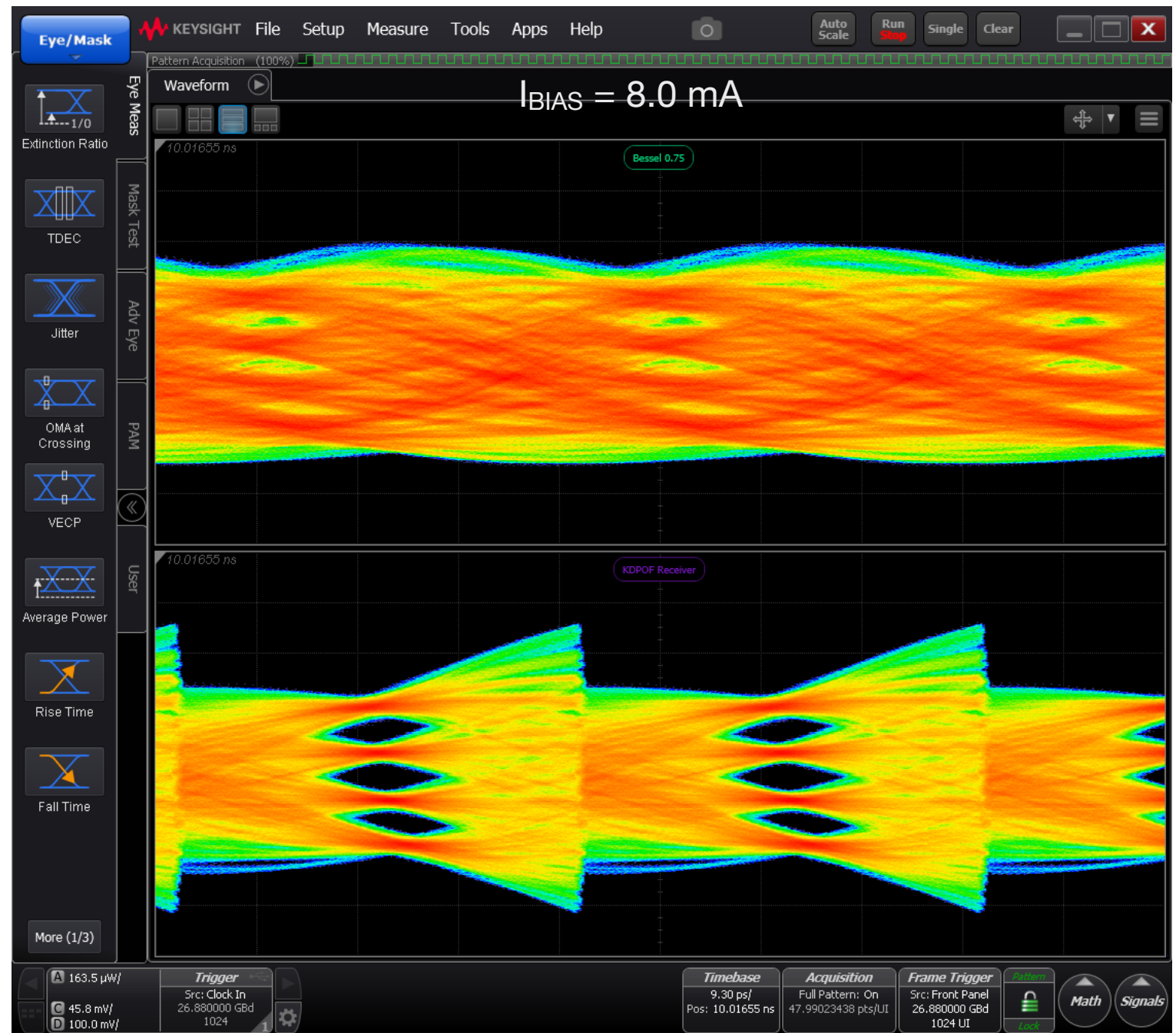
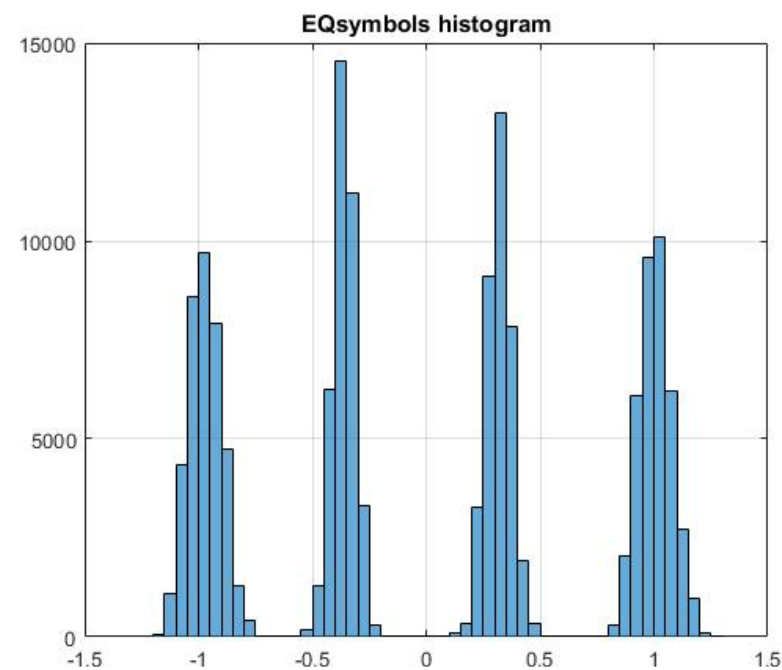
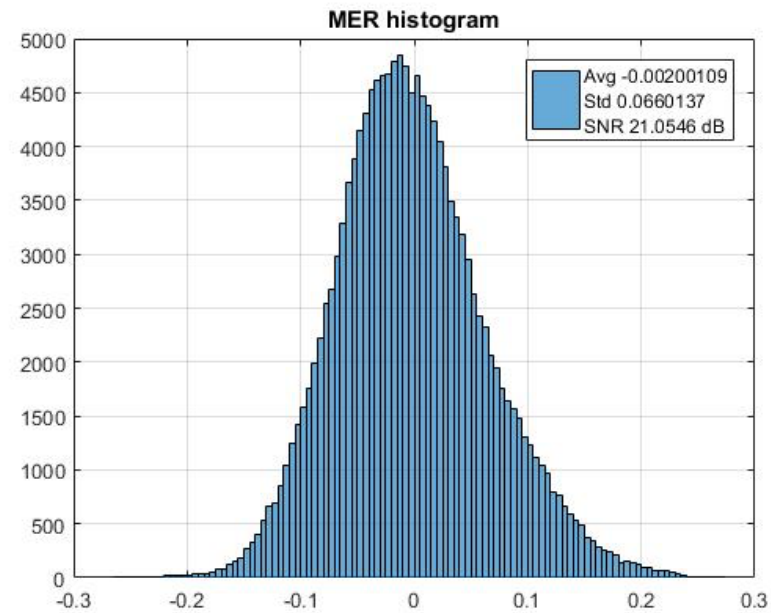
Rogers dielectric

Eye diagram, 50 Gbps

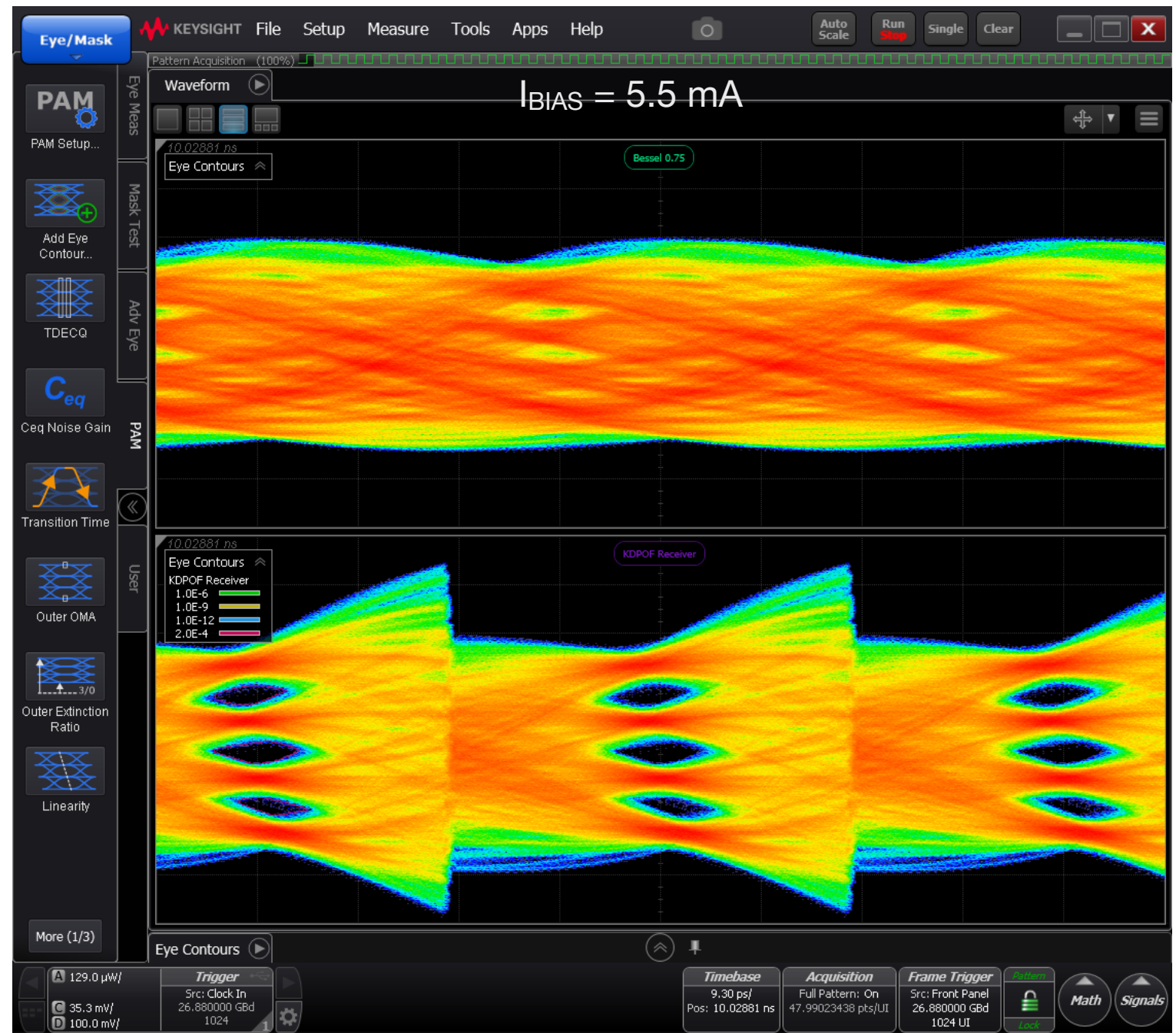
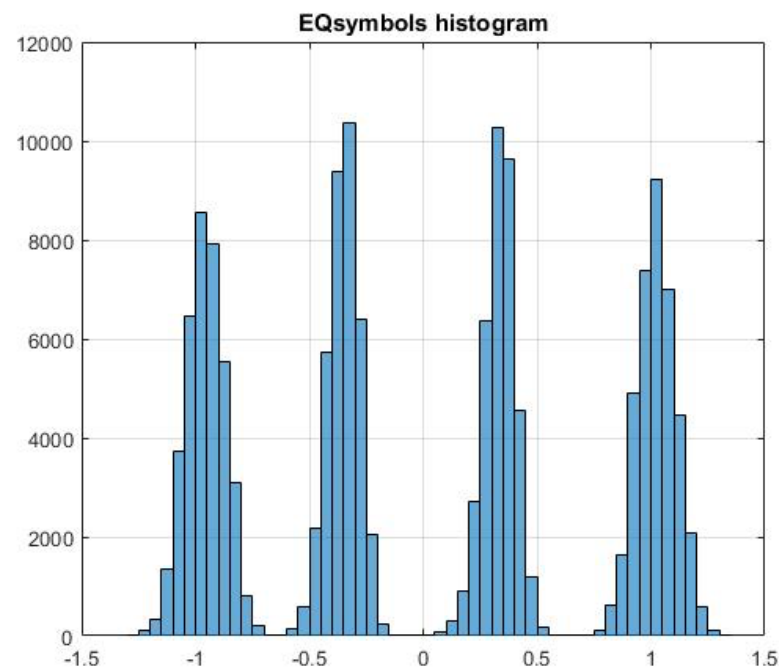
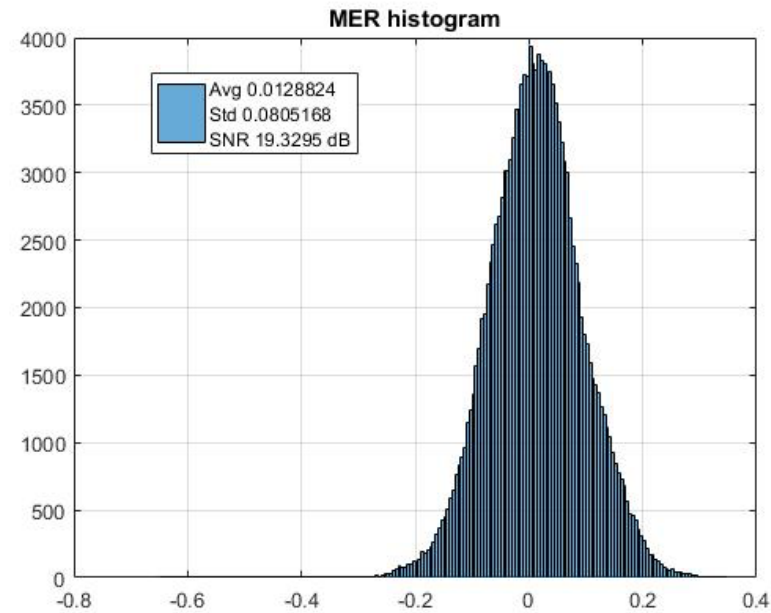


- Signal type: PAM4
- Baud-rate: 26.88 GBd (selected according to the AWG clock configuration capabilities)
- ER (current): 3 dB (expected worst case)
- Current densities at $T_s = 125^\circ\text{C}$ are limited to $< 13 \text{ kA/cm}^2$
 - See “perezaranda_OMEGA_05a_1119_VCSEL_Reliability.pdf”
- AWG is configured with response correction calibrated from factory to avoid additional driving bandwidth limitations
- DCA configuration:
 - Receiver input filter is Bessel $\text{BW}_{-3\text{dB}} = 39.8 \text{ GHz}$ (SIRC)
 - Trace 1: signal is filtered with Bessel 4th with $\text{BW}_{-3\text{dB}} = 0.75 \times \text{BR}$ (20.16 GHz)
 - Used to observe the eye diagram as usual
 - Trace 2: user operator that implements golden (KDPOF) receiver
 - Timing recovery for optimum symbol sampling
 - Adaptive equalizer coefficients calculation
 - Signal sampling and equalization processing
 - Implemented to demonstrate technical feasibility and to correlate with simulation system

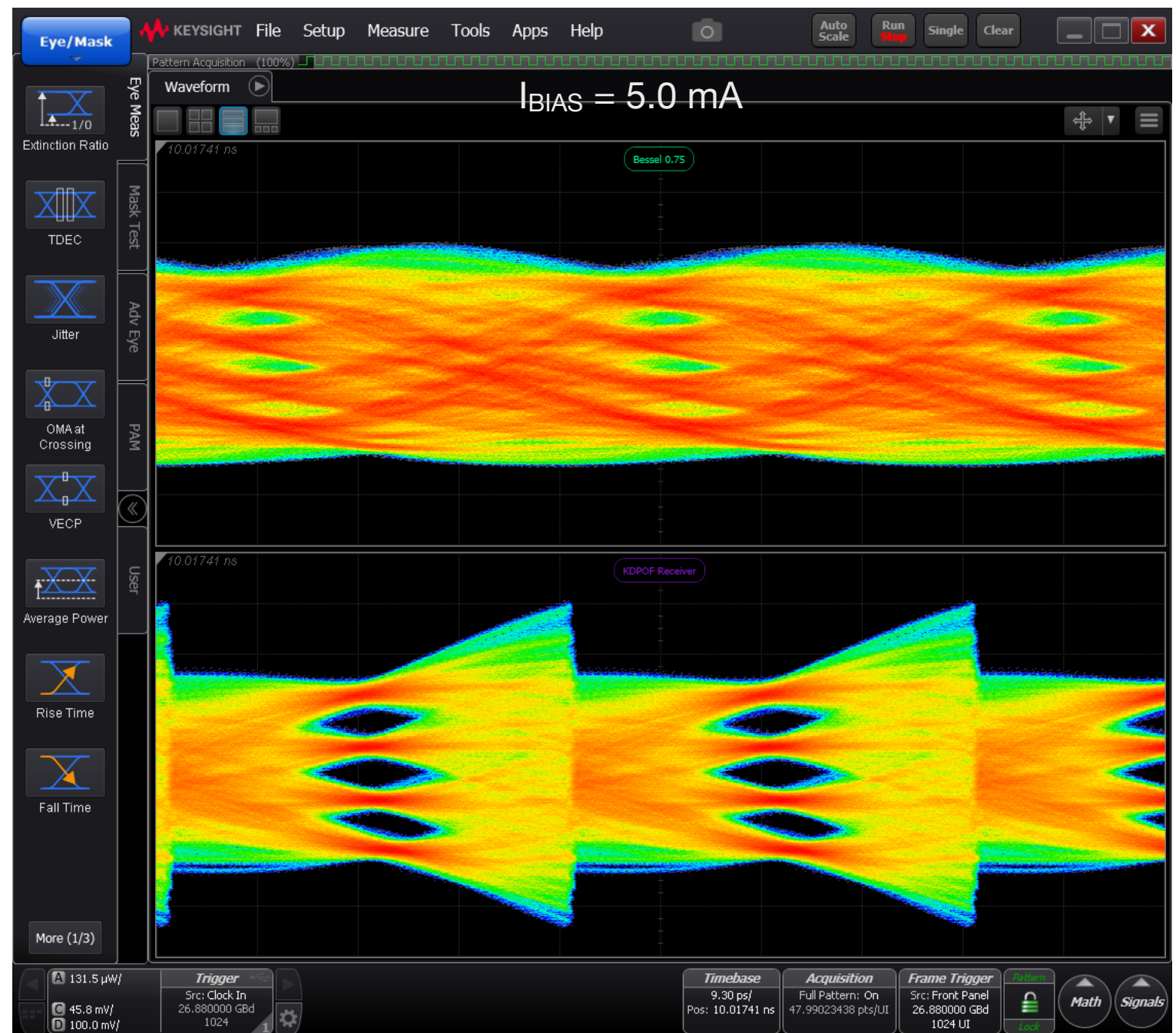
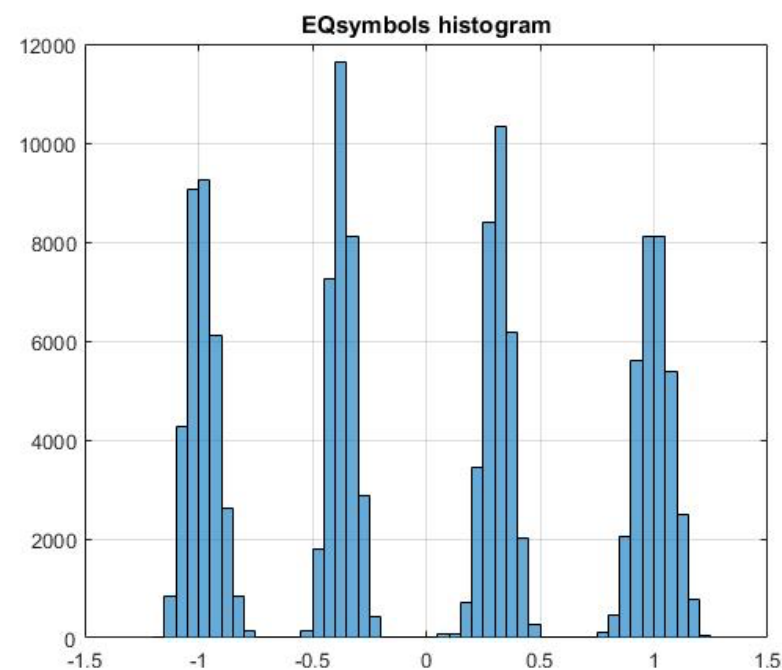
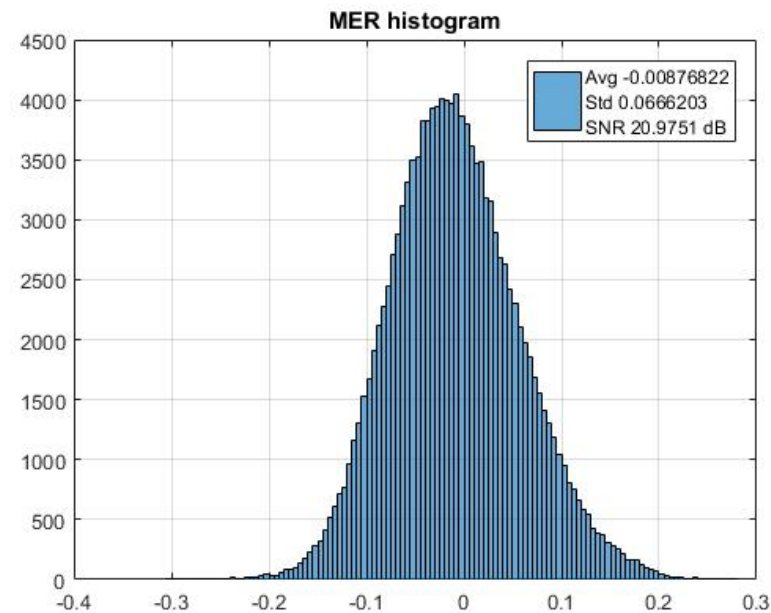
Eye diagram, -40 °C, 7.5 um, ID #235116



Eye diagram, -40 °C, 6.5 um, ID #152150



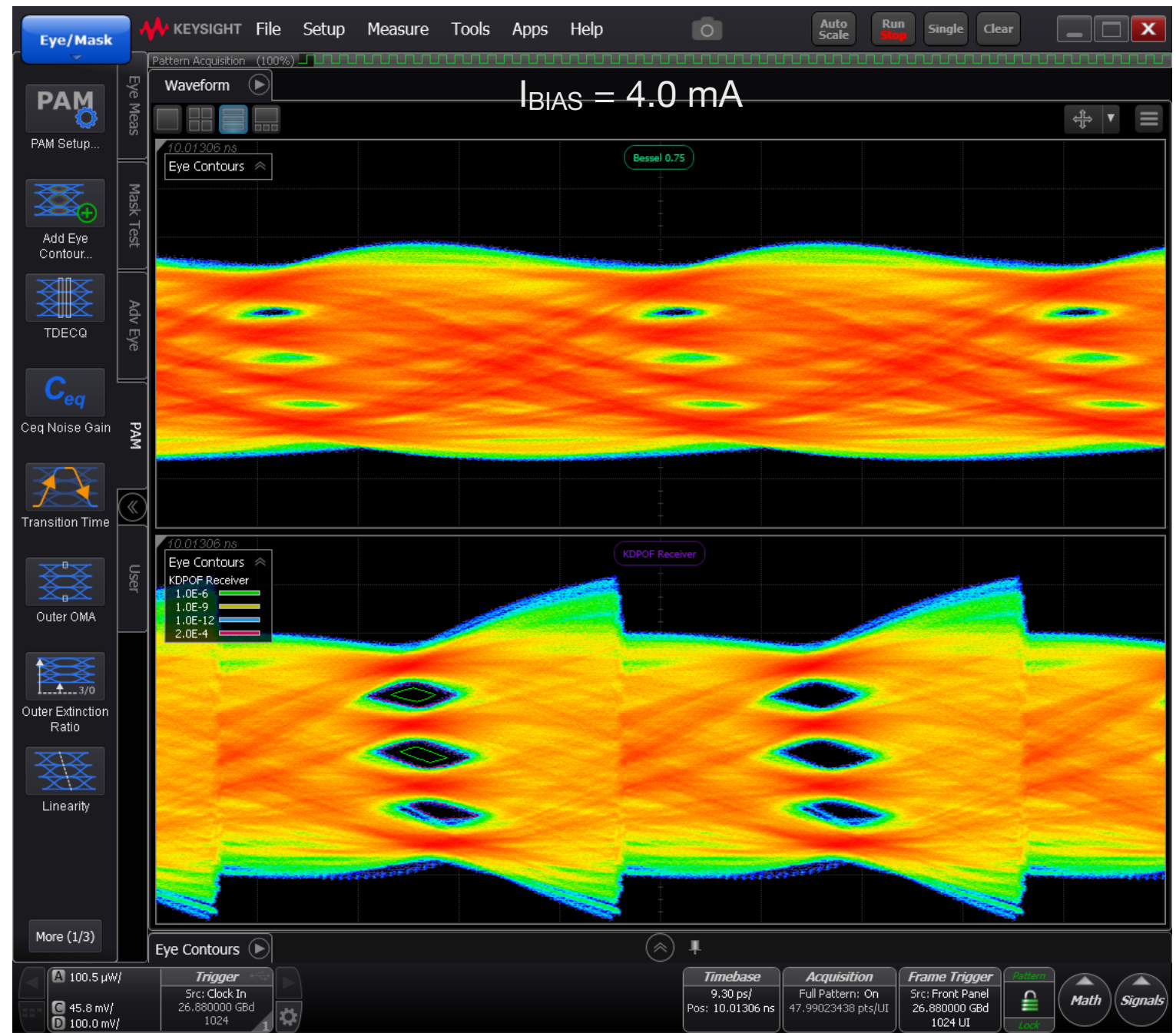
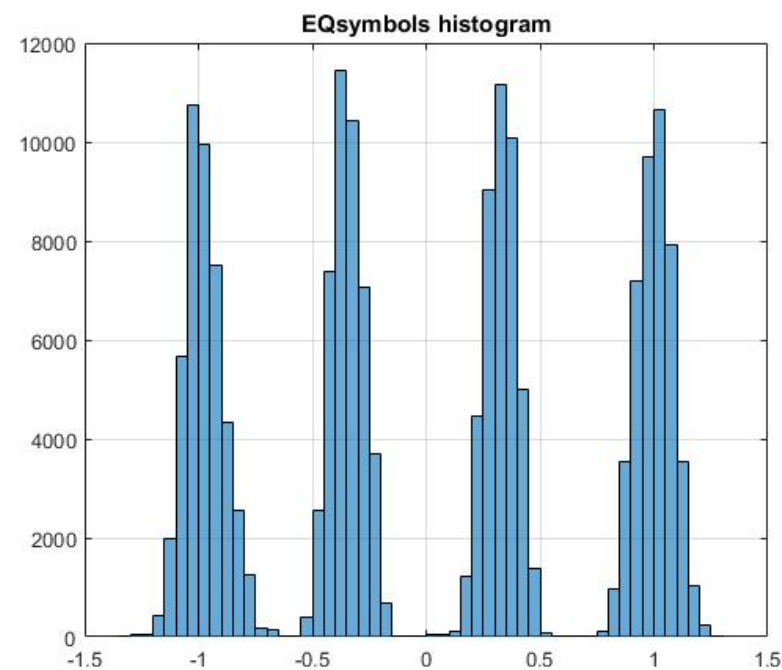
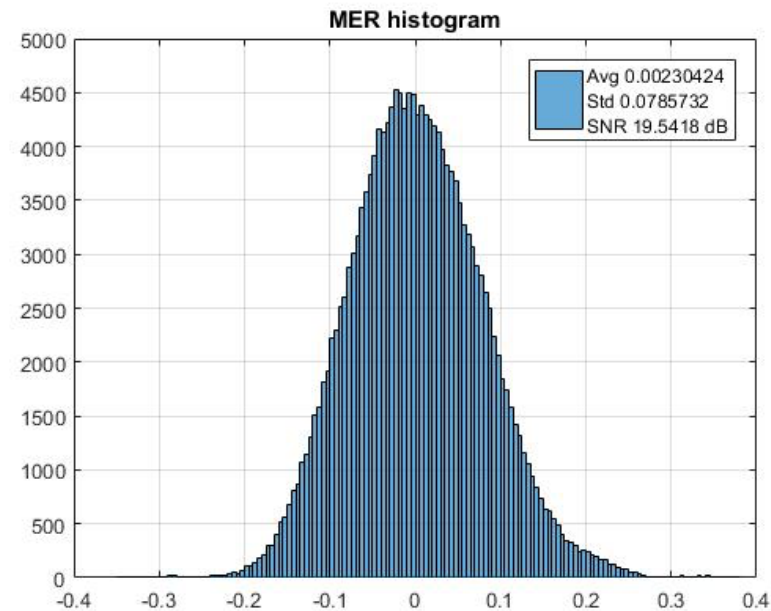
Eye diagram, 25°C, 7.5 um, ID #235116



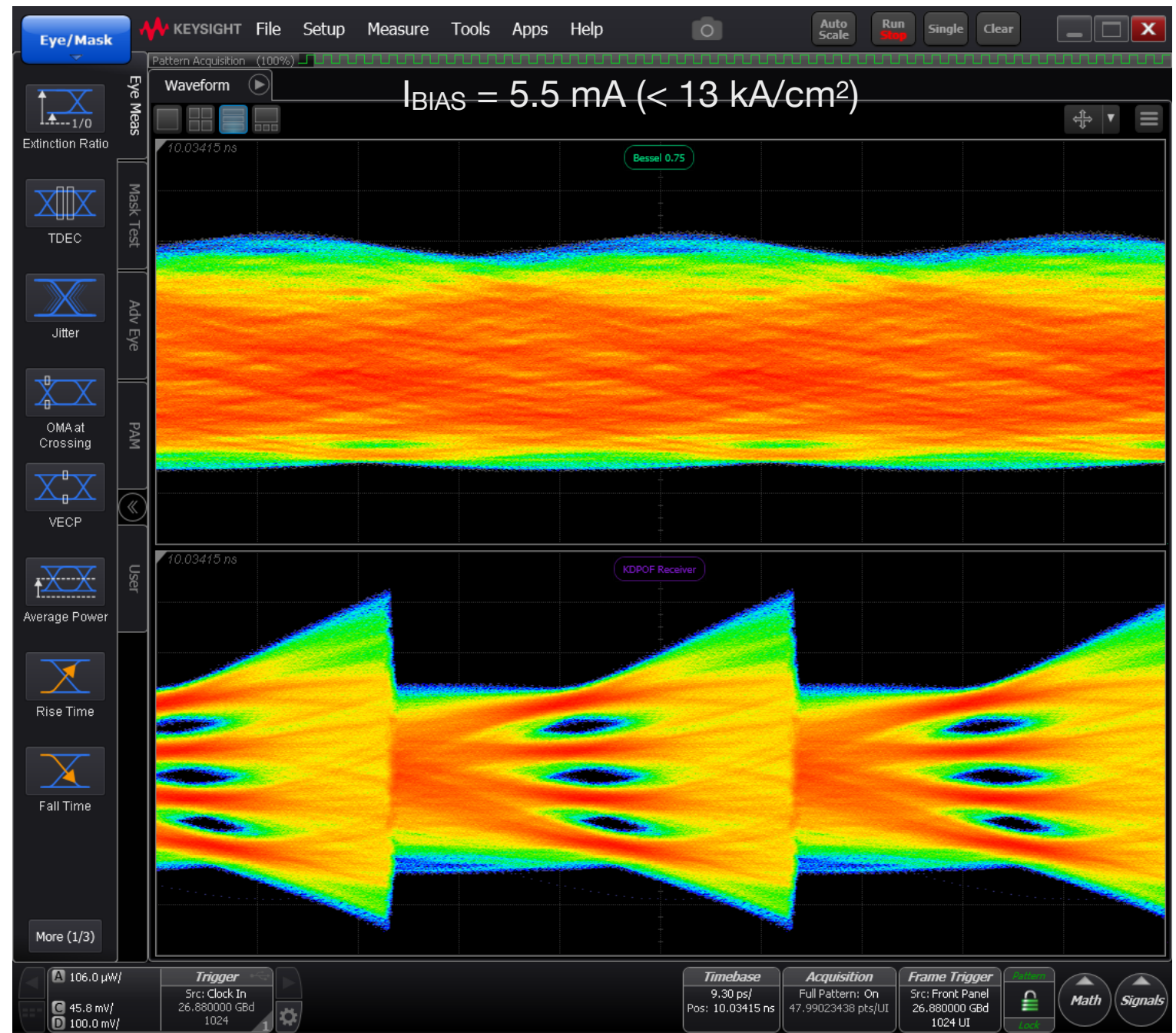
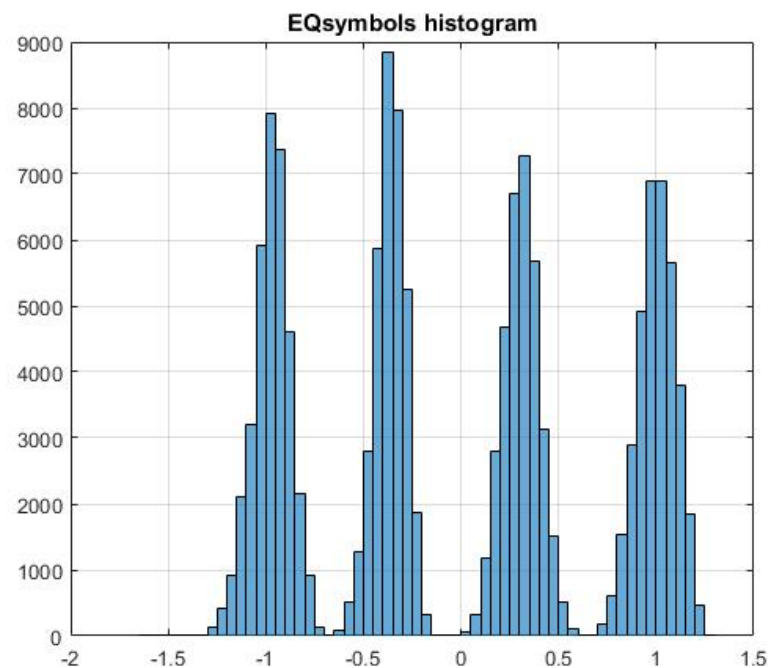
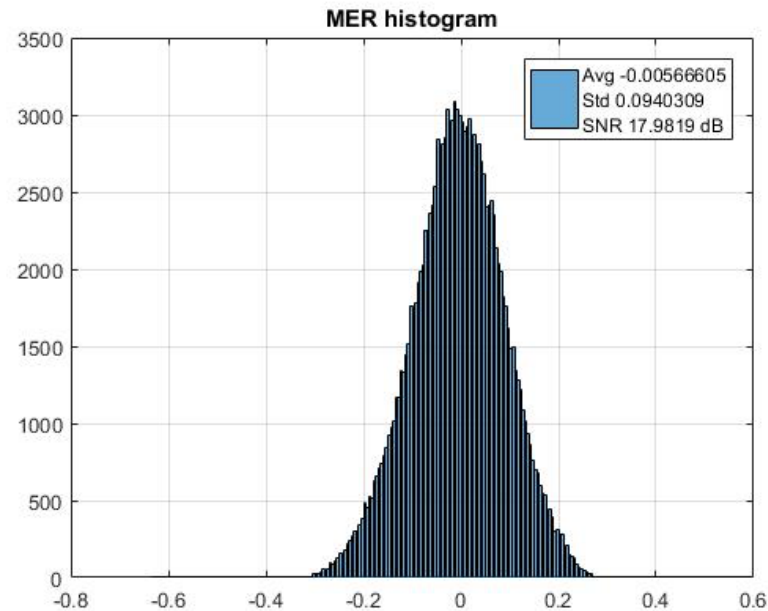
Bessel 0.75

Golden RX

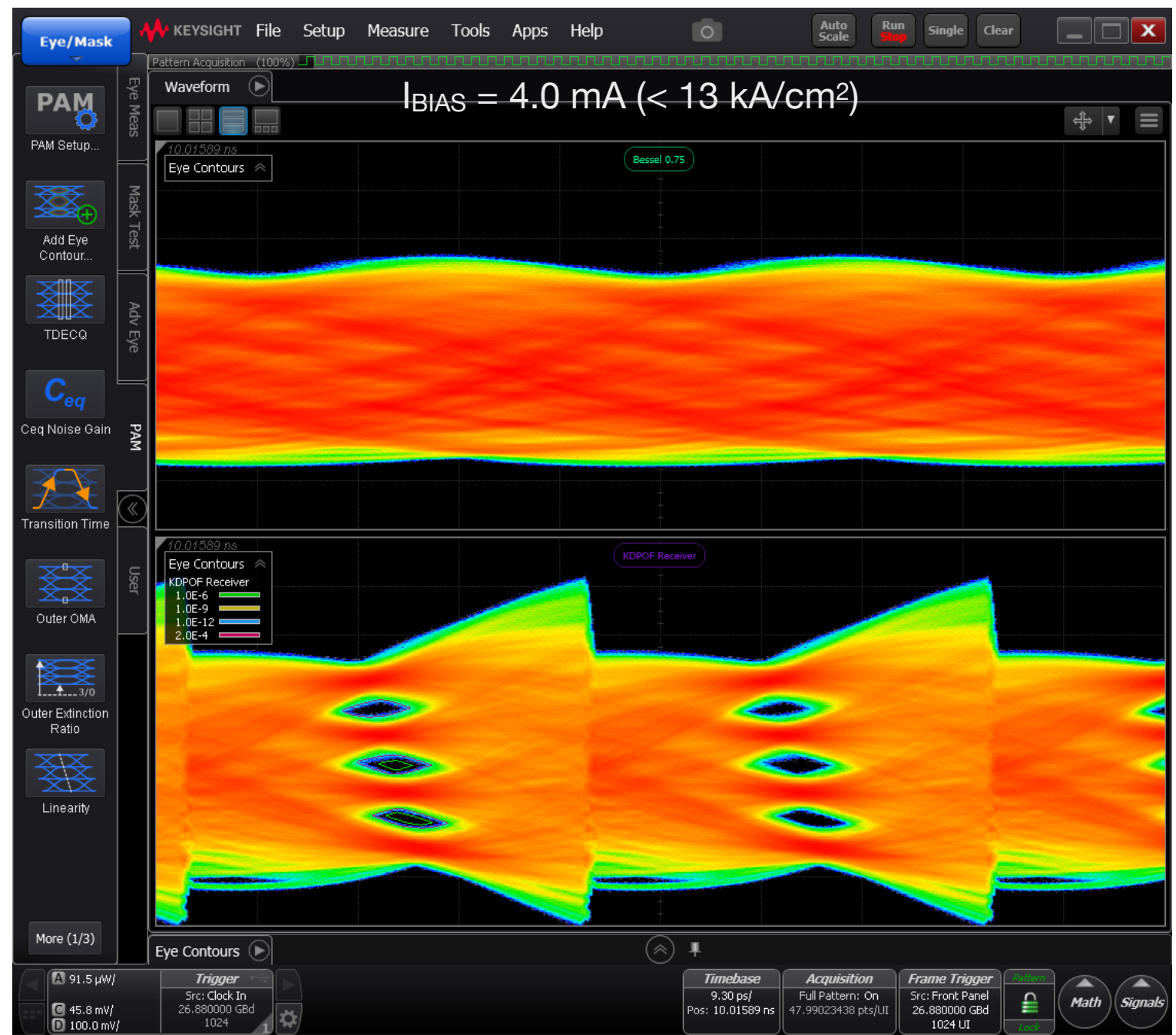
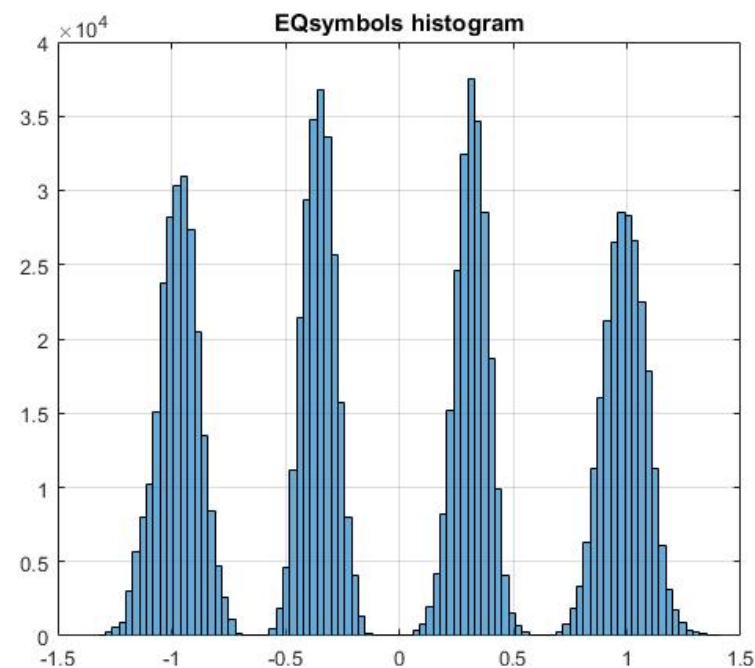
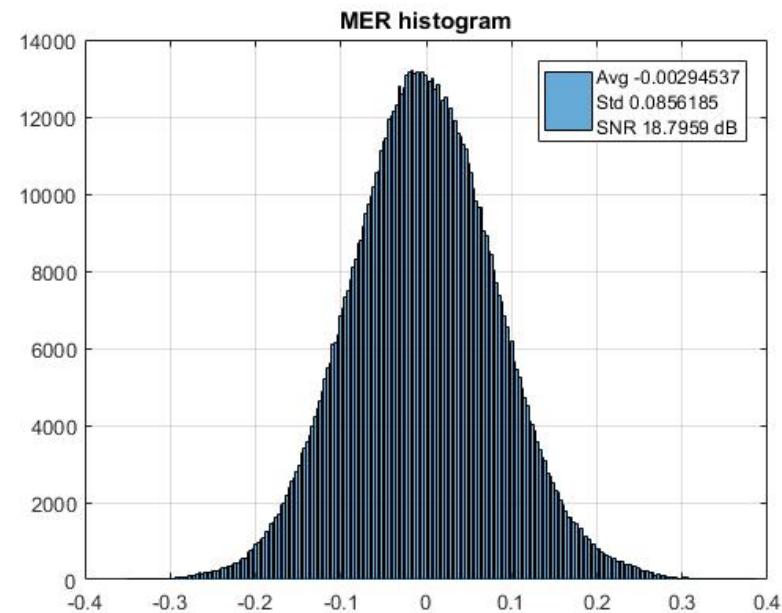
Eye diagram, 25°C, 6.5 um, ID #152150



Eye diagram, 125°C, 7.5 um, ID #235116



Eye diagram, 125°C, 6.5 um, ID #152150





50 Gb/s Link budget analysis

VCSEL parameters

Configuration	C	D	E	F
Target speed / scheme	25 Gb/s NRZ		50 Gb/s PAM4	
VCSEL T substrate (°C)	125	125	125	125
VCSEL Wavelength (nm)	850	850	850	850
VCSEL Oxide apperture, max (μm)	6.5	7.5	6.5	7.5
VCSEL Slope efficiency (mW/mA), min	0.285	0.265	0.285	0.265
VCSEL Threshold current (mA), max	0.95	1.36	0.95	1.36
VCSEL Bias current (mA), max	3.0	4.0	4.0	5.5
VCSEL Current density (kA/cm ²), max	9.05	9.06	12.06	12.46
VCSEL ER (dB), min	3	3	3	3
VCSEL ER (lin), min	2.00	2.00	2.00	2.00
VCSEL Current modulation amplitude (mApp), min	1.36	1.75	2.03	2.75
VCSEL AOP (mW), min	0.59	0.70	0.87	1.10
VCSEL AOP (dBm), min	-2.33	-1.55	-0.60	0.40
VCSEL OMA (mW), min	0.39	0.46	0.58	0.73
VCSEL OMA (dBm), min	-4.10	-3.33	-2.38	-1.37
VCSEL SE dispersion (dB), max	1.0	1.0	1.0	1.0
VCSEL Aging factor (dB), max	1.0	1.0	1.0	1.0
VCSEL OMA (dBm) with aging, min	-6.10	-5.33	-4.38	-3.37
VCSEL Relaxation Resonance Frequency (GHz)	9.3	7.9	10.4	9.1
VCSEL Damping factor (GHz)	30.5	24.8	37.3	32.2
VCSEL Extrinsic Fp (GHz), min	7.0	8.6	7.4	10.1
VCSEL BW (GHz), min	11.0	10.2	13.5	13.0
VCSEL RIN _{OMA} (dB/Hz), max spec, assumption	-124.0	-124.0	-128.0	-128.0
VCSEL RIN delta (dB) due to ER	9.6	9.6	9.6	9.6
VCSEL RIN (dB/Hz), max	-133.6	-133.6	-137.6	-137.6
VCSEL AC Coupling, max (MHz)	0.1	0.1	0.1	0.1

PD, TIA and optical connectivity parameters



PD Parameters

PD Material	GaAs
PD Tj (°C)	125
PD Wavelength (nm)	850
PD responsivity (A/W), min	0.6
PD diameter (um), max	55
PD capacitance (fF), max	180
PD pad cap (fF), max	10
PD series resistance (Ohm), max	20
PD bandwidth (GHz), min	12

TIA parameters

TIA Tj (°C)	125
TIA corner process	SLOW
TIA Tech node	CMOS 28 nm
TIA Gamma, max	1.5
TIA Gm + Gmb (mS), min	120
TIA Cgate (fF), max	165
TIA Cpad (fF), max	70

Optical connectivity parameters

Grade 0	VCSEL to TP2 IL _{MAX} (dB)	1.0
	TP3 to PD IL _{MAX} (dB)	1.0
	IC Att. Max (dB) (w/c, dust, aging)	1.0
	Macrobend IL _{MAX} (dB)	0.2
	Microbend IL _{MAX} (dB)	0.0
	Bend IL _{MAX} (dB)	0.2
Grade 1	VCSEL to TP2 IL _{MAX} (dB)	1.6
	TP3 to PD IL _{MAX} (dB)	1.6
	IC Att. Max (dB) (w/c, dust, aging)	1.7
	Macrobend IL _{MAX} (dB)	0.2
	Microbend IL _{MAX} (dB)	0.0
	Bend IL _{MAX} (dB)	0.2

< 1.0
< 1.0
< 0.75
< 0.1
< 1.0
< 1.0
< 0.75
< 0.1

Worst/case in datacenter applications

- Link budget is reduced for 50 Gb/s wrt. 25 Gb/s
- 2 grades of connectivity need to be defined.
- Expected different tolerances and relative costs.

Sensitivity and link budget



xMII DR (Gb/s)	PAM	Phase Jitter PLL _{tx,rx} (ps RMS)	VCSEL CFG	VCSEL Pre-emphasis	BLP (MHz·km)	Fiber att. (dB/km)	Length (m)	Conn. grade	OMA _{VCSEL} (dBm)	OMA _{TP2} (dBm)	OMA _{PD} (dBm) BER < 10 ⁻¹²	OMA _{TP3} (dBm)	VCSEL to PD link budget (dB)	TP2 to TP3 link budget (dB)	Allocation for connectors & bending
50	4	0.3	F	1	2000	3.0	15	0	-3.37	-4.37	-10.66	-9.66	7.29	5.29	5.24
50	4	0.3	F	1	2000	3.0	40	0	-3.37	-4.37	-10.58	-9.58	7.21	5.21	5.09
50	4	0.3	E	1	2000	3.0	15	0	-4.38	-5.38	-10.79	-9.79	6.41	4.41	4.37
50	4	0.3	E	1	2000	3.0	40	0	-4.38	-5.38	-10.72	-9.72	6.34	4.34	4.22
25	2	0.8	D	1	2000	3.0	15	1	-5.33	-6.93	-16.60	-15.00	11.27	8.07	8.03
25	2	0.8	D	1	2000	3.0	40	1	-5.33	-6.93	-16.55	-14.95	11.22	8.02	7.90
25	2	0.8	C	1	2000	3.0	15	1	-6.10	-7.70	-16.64	-15.04	10.54	7.34	7.29
25	2	0.8	C	1	2000	3.0	40	1	-6.10	-7.70	-16.59	-14.99	10.49	7.29	7.17

xMII DR (Gb/s)	PAM	Phase Jitter PLL _{tx,rx} (ps RMS)	VCSEL CFG	VCSEL Pre-emphasis	BLP (MHz·km)	Fiber att. (dB/km)	Length (m)	Conn. grade	Link Margin (dB)	Link Margin (dB)	Link Margin (dB)	Link Margin (dB)	Link Margin (dB)
									4 Inliners	3 Inliners	2 inliners	1 inliner	0 inliners
50	4	0.3	F	1	2000	3.0	15	0	1.04	2.04	3.04	4.04	5.04
50	4	0.3	F	1	2000	3.0	40	0	0.89	1.89	2.89	3.89	4.89
50	4	0.3	E	1	2000	3.0	15	0	0.17	1.17	2.17	3.17	4.17
50	4	0.3	E	1	2000	3.0	40	0	0.02	1.02	2.02	3.02	4.02
25	2	0.8	D	1	2000	3.0	15	1	1.03	2.73	4.43	6.13	7.83
25	2	0.8	D	1	2000	3.0	40	1	0.90	2.60	4.30	6.00	7.70
25	2	0.8	C	1	2000	3.0	15	1	0.29	1.99	3.69	5.39	7.09
25	2	0.8	C	1	2000	3.0	40	1	0.17	1.87	3.57	5.27	6.97

Conclusions



- Real 50 Gb/s PAM4 transmission has been demonstrated between $-40\text{ }^{\circ}\text{C}$ and $+125\text{ }^{\circ}\text{C}$, based on InGaAs 25G VCSEL
- VCSEL current density needs to be increased from 9 kA/cm^2 to 12.5 kA/cm^2 to make feasible 50 Gb/s transmission
 - Important RIN reduction (4 dB)
 - Slight bandwidth improvement ($\sim 2\text{ GHz}$)
 - AOP at TP2 increase ($\sim 2\text{ dB}$)
 - VCSEL reliability can be a problem depending on the device design
- Despite these counter measurements, the VCSEL-to-PD link budget is reduced $\sim 4\text{ dB}$ to get double data-rate
 - Required better optical coupling quality in TP2 and TP3
 - Required smaller insertion loss per inline connection
- PAM4 requires almost 7 dB additional SNR: better linearity and resolution is demanded to electronics
 - Bigger area
 - Higher power consumption



Thank you