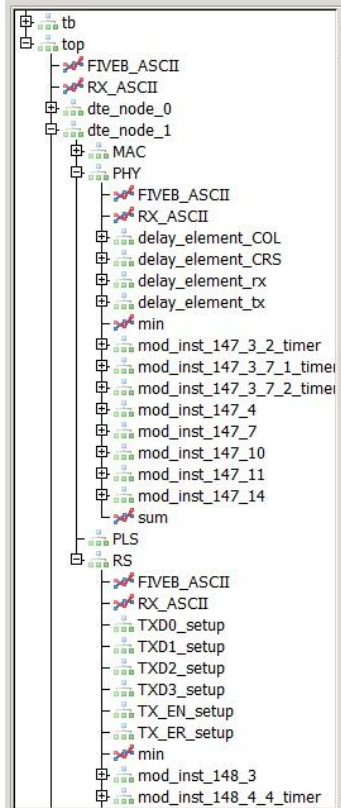


SST



Type Signals

reg mod_148_5_state_ASCII[103:0]
 reg plca_status_ASCII[31:0]
 reg rx_cmd_ASCII[47:0]
 reg tx_cmd_ASCII[47:0]
 reg tx_cmd_sync_ASCII[47:0]

Filter: ascii

Append Insert Replace

Signals

```

Time
top.dte_node_2.RS.mod_inst_148_3.mod_148_3_state_ASCII[151:0]=
top.dte_node_2.RS.mod_inst_148_3.curID[7:0]=
top.dte_node_2.RS.mod_inst_148_3.rx_cmd_ASCII[47:0]=

top.dte_node_0.TX_EN=
top.dte_node_1.TX_ER=
top.dte_node_1.TX_EN=
top.dte_node_2.TX_ER=
top.dte_node_2.TX_EN=
top.dte_node_3.TX_ER=
top.dte_node_3.TX_EN=

top.dte_node_0.RS.local_nodeID[7:0]=
top.dte_node_1.RS.local_nodeID[7:0]=
top.dte_node_2.RS.local_nodeID[7:0]=
top.dte_node_3.RS.local_nodeID[7:0]=

top.dte_node_0.RS.mod_inst_148_3.mod_148_3_state_ASCII[151:0]=
top.dte_node_1.RS.mod_inst_148_3.mod_148_3_state_ASCII[151:0]=
top.dte_node_2.RS.mod_inst_148_3.mod_148_3_state_ASCII[151:0]=
top.dte_node_3.RS.mod_inst_148_3.mod_148_3_state_ASCII[151:0]=

top.dte_node_0.RS.mod_inst_148_3.curID[7:0]=
top.dte_node_1.RS.mod_inst_148_3.curID[7:0]=
top.dte_node_2.RS.mod_inst_148_3.curID[7:0]=
top.dte_node_3.RS.mod_inst_148_3.curID[7:0]=

top.dte_node_3.RS.CRS=
top.dte_node_3.RS.RX_DV=
top.dte_node_3.RS.receiving=
top.dte_node_3.RS.RX_ER=
top.dte_node_3.RS.rx_cmd_ASCII[103:0]=

top.dte_node_0.RS.mod_inst_148_5.mod_148_5_state_ASCII[103:0]=
top.dte_node_1.RS.mod_inst_148_5.mod_148_5_state_ASCII[103:0]=
top.dte_node_2.RS.mod_inst_148_5.mod_148_5_state_ASCII[103:0]=
top.dte_node_3.RS.mod_inst_148_5.mod_148_5_state_ASCII[103:0]=

top.dte_node_0.RS.plca_active=
top.dte_node_1.RS.plca_active=
top.dte_node_2.RS.plca_active=
top.dte_node_3.RS.plca_active=

top.dte_node_0.RS.packetPending=
top.dte_node_1.RS.packetPending=
    
```

Waves

