Next Generation IO Enabling 400Gbps C2M and CR Channels

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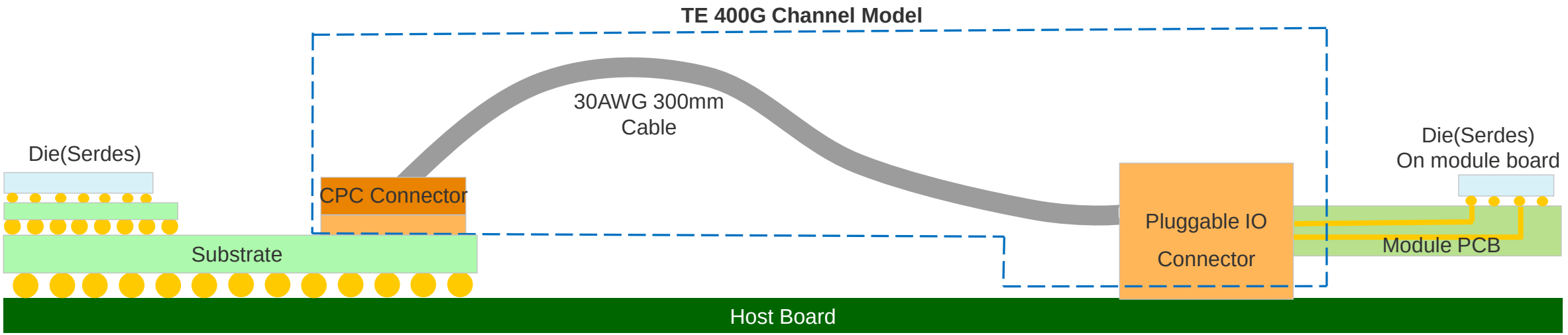
EVERY CONNECTION COUNTS

400 Gbps Next Generation Pluggable IO

- **A new generation of face plate pluggable interconnect is proposed with an optimized stub-less interface**
- Based on this new face plate pluggable IO interconnect, two channels have been simulated:
  - C2M (Chip to Module): **tracy_efai_02a_250430**
  - CR (passive copper cable assembly): **tracy_efai_03a_250430**
- S-parameter channels are included with this contribution for IEEE attendee analysis regarding architecture, modulation and equalization tradeoffs for the IEEE 802.3 NEA “Ethernet for AI” Assessment activity
- This interconnect development and related channels are an on-going body of work and further progress will be contributed

C2M Channel (tracy_efai_02a_250430)



CPC Connector

- Includes connection to substrate (device package) and internal cable termination.
- Does not include substrate footprint and breakout.

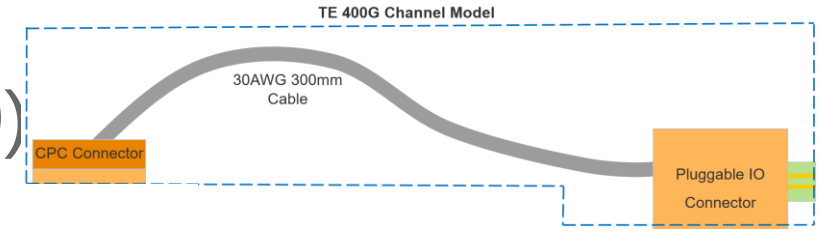
Pluggable IO Connector

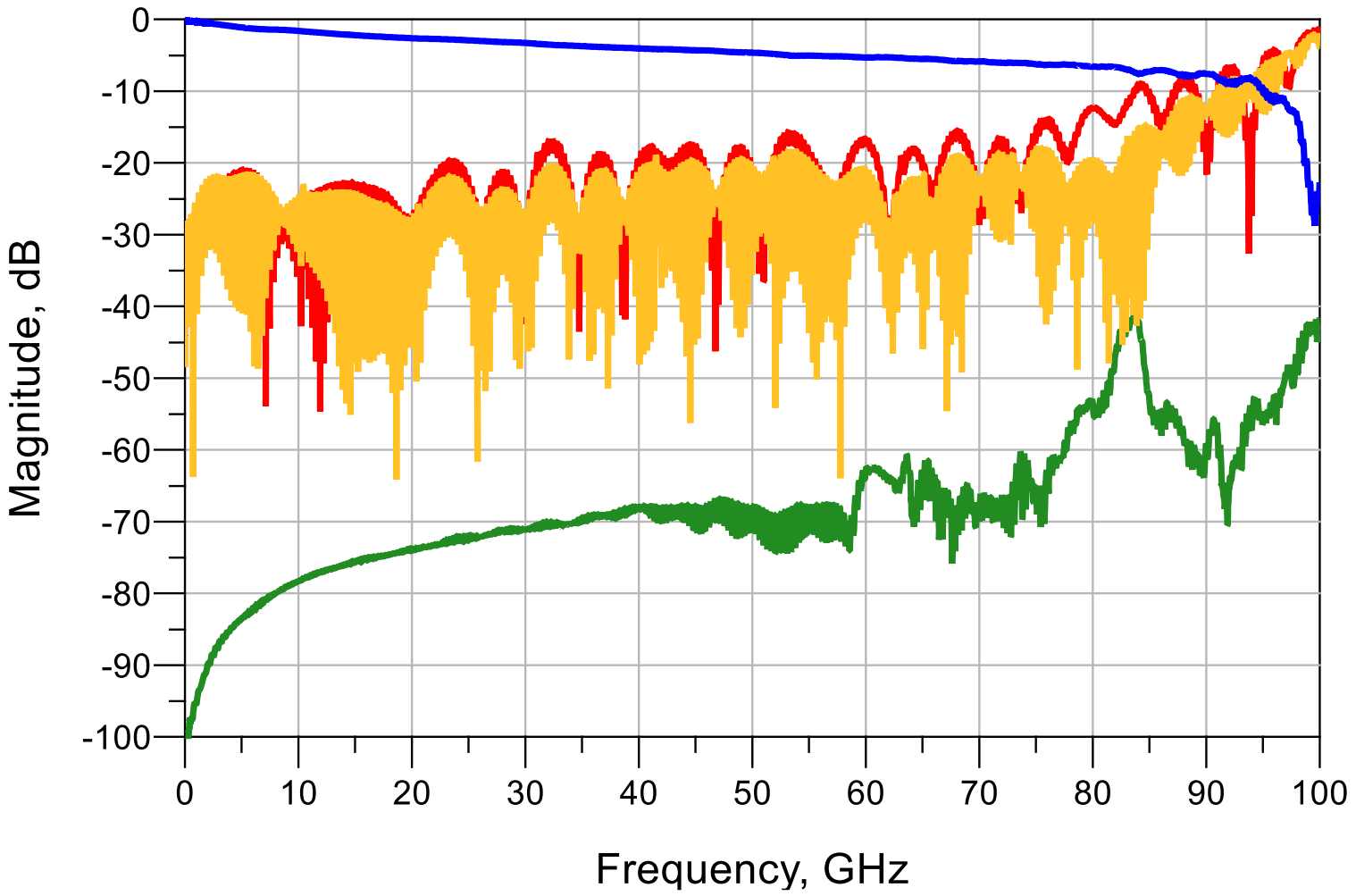
- Includes: internal cable termination and short module trace.
- Does not include full trace routing on module board.

Channel File Name: tracy_efai_02a_250430

Models are preliminary and under development.

C2M Channel (tracy_efai_02a_250430)



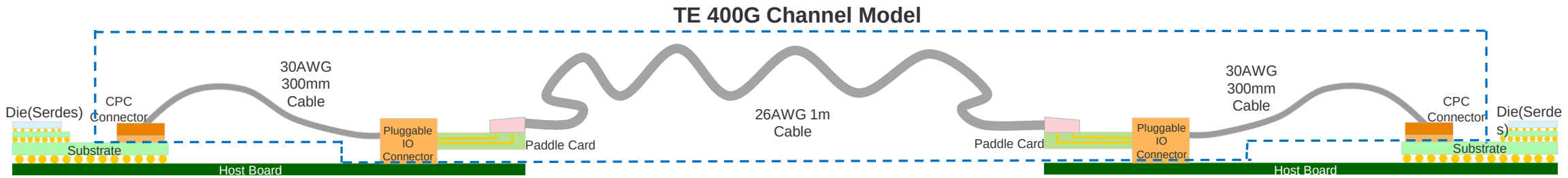


Insertion Loss
Return Loss, Module side
Return Loss, Host side
PowerSum Crosstalk

Crosstalk includes 3 FEXT and 4 NEXT aggressors, module side.

Models are preliminary and under development.

Direct Attach Copper Cable Channel (tracy_efai_03a_250430)



CPC Connector

- Includes connection to substrate and internal cable termination.
- Does not include substrate footprint and breakout.

Pluggable IO Connector

- Includes internal cable termination.

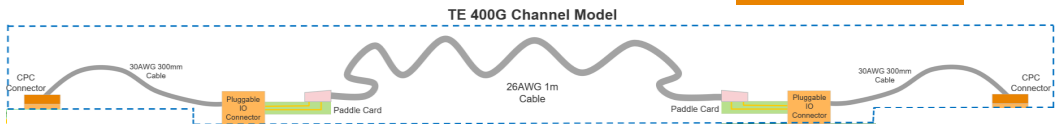
Paddle Card

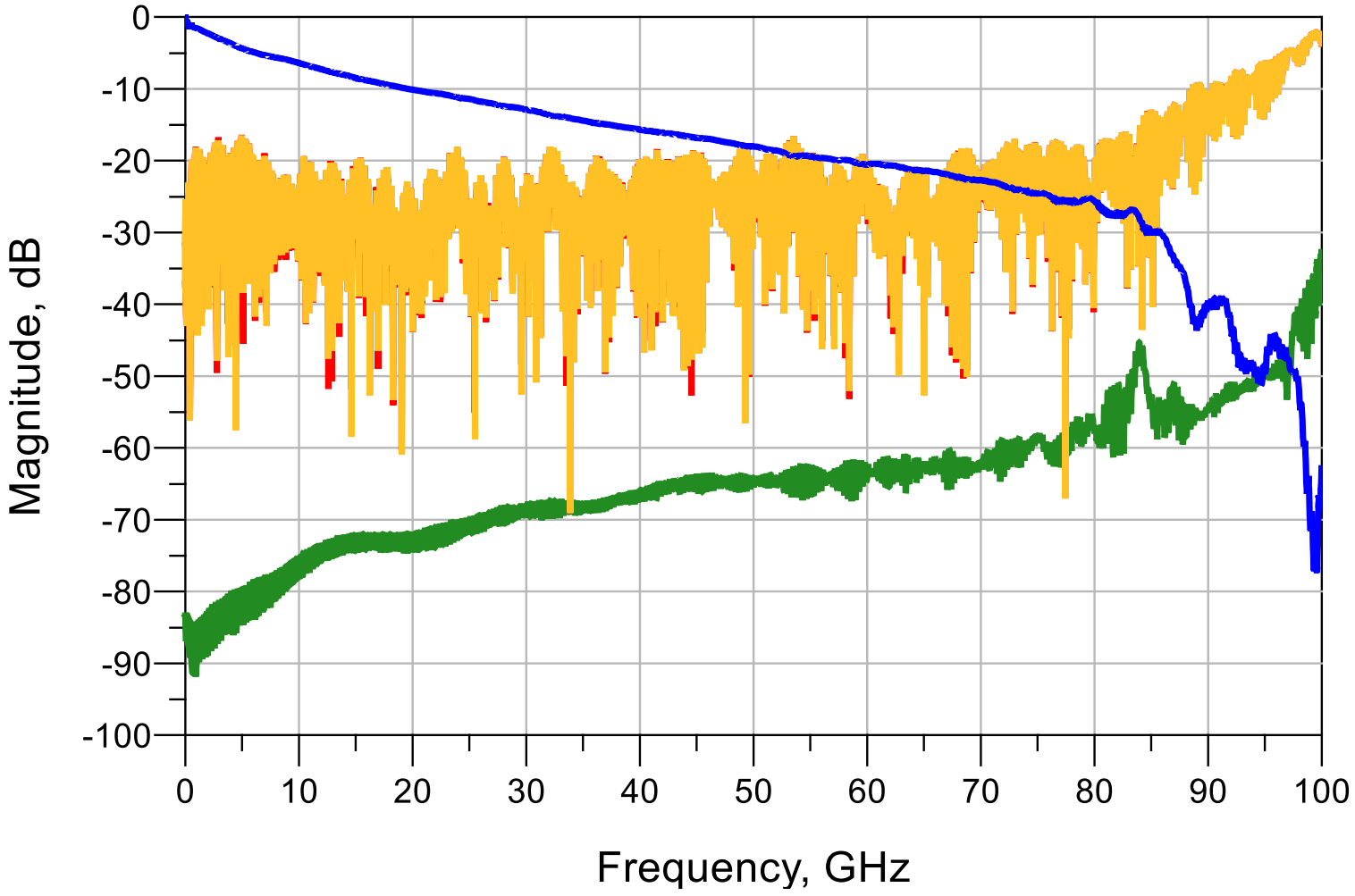
- Includes external cable termination and paddle card routing and bulk cable

Channel File Name: tracy_efai_03a_250430.

Models are preliminary and under development.

DAC Channel (tracy_efai_03a_250430)





Insertion Loss
Return Loss
PowerSum Crosstalk

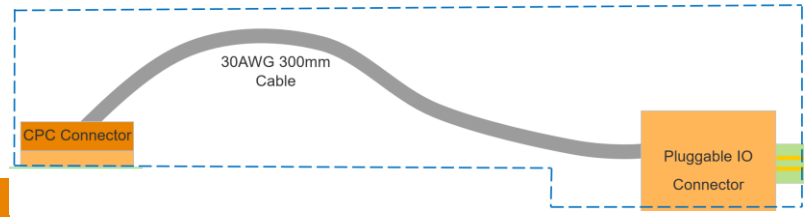
Crosstalk includes 3 FEXT, 4 NEXT

Models are preliminary and under development.

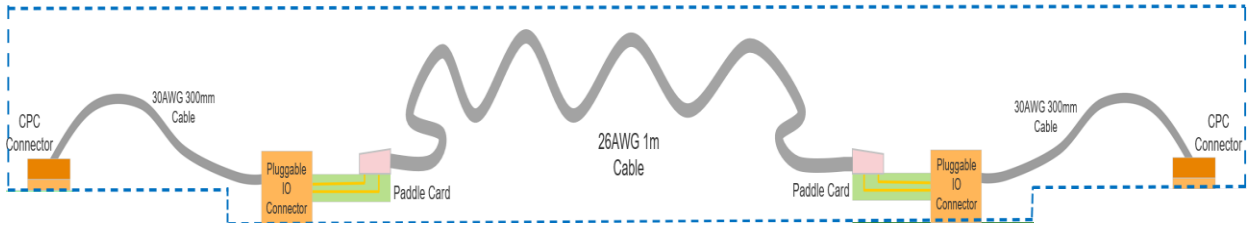
400 Gbps Imperatives

- New pluggable interconnect is required, eliminate transmission line stubs for optimal impedance management
- Insertion Loss: PCB, Substrate trace loss is challenging at these candidate Nyquist frequencies and densities. Twinax cable-based architectures are a viable alternative.
- Return Loss: Relentless drive for optimized transitions to minimize reflections is critical. Interconnect mating interfaces and leadframes are streamlined
- Crosstalk: Interconnect design and PCB/Substrate escapes are highly shielded to minimize near and far end crosstalk. This is especially critical at the densities required.

TE 400G C2M Channel Model



TE 400G CR Channel Model



Summary

- Transition to 400G/lane drives addressable challenges along all SI vectors: loss, crosstalk, reflections
- A new pluggable IO connector is proposed as opposed to ‘band-aiding’ existing interfaces
- Addressing the SI challenges in the accelerated adoption time frame demands an optimized approach to channel development
- The authors are providing early simulation-based 400G C2M (tracy_efai_02a_250430) and CR (tracy_efai_03a_250430) channels for IEEE attendee evaluation and analysis
- Face plate pluggable module and passive copper cable-based architectures are promising realities at 400 Gbps
- This interconnect development and related channels are an on-going body of work and further progress will be contributed