PAMXmY with LDPC Modulation Proposal for 448G

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Overview

- Background
- LDPC Overview
- PAMXmY LDPC System
- LLR Mapping
- SER Performance
- Summary

448G Soft FEC

- **Entangle the DFE channel with a soft FEC**
- **Target is to reduce the Pre-KP FEC Symbol Error Rate (SER) by two or more decades**
- **Latency target**
  - KP FEC is 5440 bits + t15 RS decoding
  - Previous discussions permitted 2x and even 12x interleaving of KP FEC
  - Set soft FEC target latency at (0.5 to 4.0) x 5440 bits
- **Gates are efficient**
  - 3 nm or lower geometry
  - Gates/unit area continues to scale favorably
  - Try not to use SRAM as this does not scale well
- **Ideally cooperates well with following KP FEC**
- **Follow receiver progression**
  - Analog sampler based DFE → ADC + DSP → ADC + DSP + SoftFEC

*Note: Latency targets increased from previous work

PAMXmY Modulation

- **PAMXmY Modulation**
  - X represents the Baud rate PAM levels
    - Number of levels required to represent information
  - Y represents the actual levels used
    - Additional levels from PAMY used by soft FEC

- **PAM6m8**
  - 2 Symbols of PAM6 give 5 information bits
  - 2 Symbols of PAM8 give 6 coded bits
  - Supports a FEC code rate of 5/6

- **Use the extra levels to form a more complex trellis with an LDPC code**

LDPC Overview

- **Low-Density-Parity-Check (LDPC)**

- **LDPC Pros**
  - Capacity approaching error correction performance
  - Best performance for soft input decoding
  - Parallel structure scales well for operation at any speed
  - Broadly adopted correction method for many standards and applications

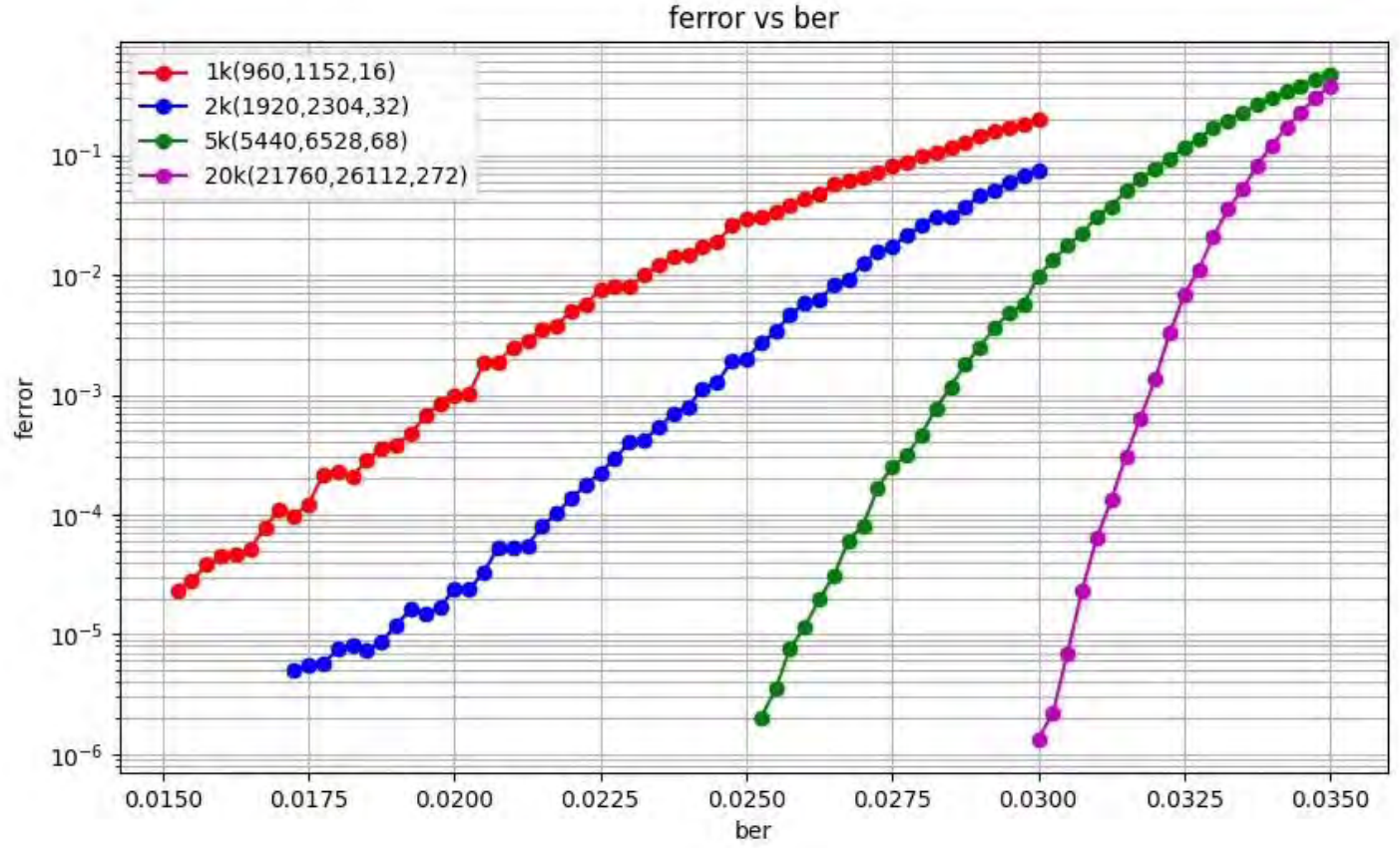
- **LDPC Cons**
  - Iterative decoding structure
    - Different FEC blocks at the same bit error point will require different decoding times
  - Not well-suited to burst-error susceptible systems
    - Input patterns have high bit error rates
    - LDPC does not inherently correct burst errors
  - LDPC decode failures often result in randomly placed bit errors
    - Not ideal for interoperation with KP-FEC

LDPC Overview : Continued

- **LDPC Input**
  - Log-Likleyhood-Ratio (LLR)
    - Efficient number format for doing probability calculations
  - LLR = Log (P0/P1)
    - P0 is the probability that a bit is a 0
- **LDPC Codes**
  - (N,K,EF)
  - N is the number of data bits in a FEC block
  - K is the total number of bits in a FEC block
  - EF is the Expansion Factor for the Quasi-cyclic H-Matrix
    - 4 Reference codes
      - 1k(960,1152,16)
      - 2k(1920,2304,32)
      - 5k(5440,6528,68)
      - 20k(21760,26112,272)

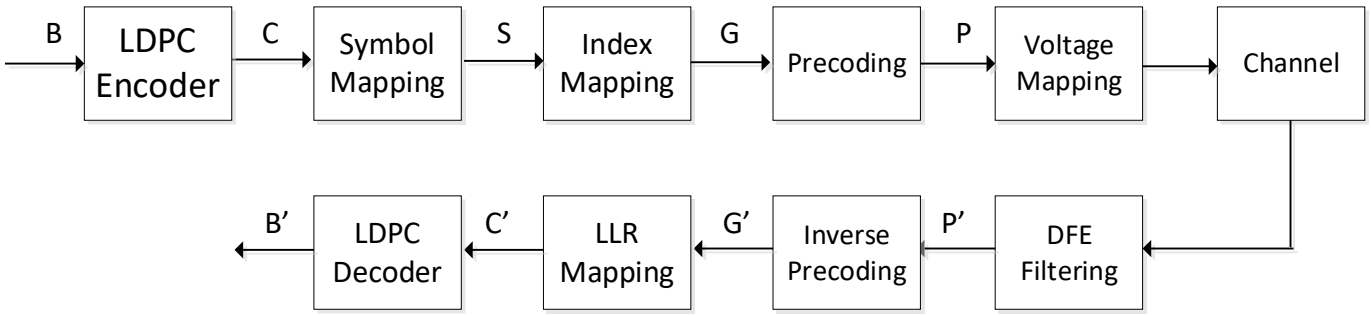
LDPC Overview (Reference Curves)

- **Background**
  - Custom codes
  - Generic fixed-precision layered LDPC decoder
- **Reference Performance**
  - AWGN Channel
  - Frame Error is a failed LDPC Decode
  - BER is Bit-Error-Rate
- **Focus on 5k code for subsequent analysis**
  - Good Waterfall in AWGN



PAMXmY LDPC System

- **Transmit path requires the following steps**
  - LDPC encoding
  - Symbol mapping
  - Index mapping
  - Precoding
  - TX Voltage mapping
- **Receive path requires**
  - DFE decoding
  - Reverse precoding
  - LLR mapping
  - LDPC decoding
- **Channel is TX(n)+D*TX(n-1)+noise**
  - Represents full DSP receiver after the FFE filter in a Serdes receiver



PAMXmY LDPC System

- **LDPC Encoder**
  - 5440 input bits, 6528 output bits
  - 2176 Symbols
  - Note 5440/2.5 (PAM6) = 6528/3 = 2176 (PAM6m8)
- **Symbol Mapping**
  - 3 bits mapped to each symbol
- **Index Mapping**
  - Label each level with an index between 0 and 7
  - Grey-mapping when connecting bits to indices
- **Precoding to remove burst errors**

PAMXmY LDPC System

- **Grey Coding**
  - For PAM8 we have 8 different levels of transmission, representing 3 bits of information
  - The mapping of these 3 bits to 8 levels is such that an error of 1 level only causes an error in a single bit

- **PAM8 Levels**
  - Indices {0, 1, 2, 3, 4, 5, 6, 7}
  - TX Output levels{-7, -5, -3, -1, 1, 3, 5, 7} (Scaled to 1V Peak to Peak)

- **Precoding (TX)**
  - The transmitter sends the difference between the new symbol B(n) and the last symbol that was sent (TX(n-1))
  - A commonly used technique to mitigate burst errors
  - A DFE error burst is converted to two errors, one at the front of the burst and one at the end of a burst
  - TX(n) = (B(n) – TX(n-1) + 8) % 8 (For PAM8)

Grey, Index and TX Levels, PAM8

b2b1b0	TX Index	TX Precode	TX Level
000	0	0	-7
001	1	1	-5
011	2	2	-3
010	3	3	-1
110	4	4	1
111	5	5	3
101	6	6	5
100	7	7	7

PAMXmY LDPC System

- **1-tap DFE Channel and Receiver**
  - RX(n) = TX(n)+D*TX(n-1)+Noise
    - D is typically 0.5 to 0.875
  - P(n) = Slice (Rx(n) – D * P(n-1))
    - Received symbol is current RX value – D*previous symbol sliced to 8 levels
    - D=0.875 used for this work

- **Precoding (RX)**
  - Undo the precoding performed at the transmitter to obtain the original symbol
  - G’(n) = (P’(n)+P’(n-1))%8

- **LDPC Codes**
  - Low-Density Parity Check (LDPC) is a capacity approaching error correction code
  - Focus is on 5440 / 6528 code (CR=5/6 for PAM6m8)
    - Code is 80 data columns with 96 total columns and Expansion Factor=68

- **Log-Likelihood Ratio (LLR)**
  - A value representing the probability that bit is a 1 or a zero
  - Larger magnitude indicates greater confidence
  - Positive LLRs are 0s and negative LLRs are 1s

LLR Mapping

- **Incorporate key properties of DFE channels and precoding**
- **G' may differ from G by 1 level**
  - A received value of 5 at G' may have been a 4 or a 6 in the transmitter
- **Based on this property we find that 1 of the 3 bits in any Symbol are +-Infinity**
  - Large LLR values are used for these bits
- **Simple LLR mapping for the other 2 bits is**

$$LLR = log\left(\frac{(1-p)+p/2}{p/2}\right) = log\left(\frac{2-p}{p}\right)$$

  - Where p is the symbol error rate at G'
    - a fixed value of p=3% can be used

Map1 : PAM8 LLR Mapping Table

Index	b2	b1	b0	LLR2	LLR1	LLR0
0	0	0	0	4.1	Inf	4.1
1	0	0	1	Inf	4.1	-4.1
2	0	1	1	Inf	-4.1	-4.1
3	0	1	0	4.1	(-Inf)	4.1
4	1	1	0	-4.1	(-Inf)	4.1
5	1	1	1	(-Inf)	-4.1	-4.1
6	1	0	1	(-Inf)	4.1	-4.1
7	1	0	0	-4.1	Inf	4.1

b2 is a 1 for 4,5 and 6

Note :Negative LLRs are 1's and positive LLRs are 0's

LLR Mapping : continued

- **Add the slicer levels to the table**
  - Even levels
  - {-6, -4, -2, 0, 2, 4, 6}
  - Maximum uncertainty about one of the bits
- **Considering Index 5.5 (level 4)**
  - b2 is a very strong 1
  - At level 4 we find b1 to be at its decision point (LLR 0)
  - At level 4 we find b0 to be at the center of its distribution, or a strong 1
- **Error in one bit means more confidence is another bit**

Level	Index	b2	b1	b0
-7	0	0	0	0
-6	0.5	0	0	0 or 1
-5	1	0	0	1
-4	1.5	0	0 or 1	1
-3	2	0	1	1
-2	2.5	0	1	0 or 1
-1	3	0	1	0
0	3.5	0 or 1	1	0
1	4	1	1	0
2	4.5	1	1	0 or 1
3	5	1	1	1
4	5.5	1	0 or 1	1
5	6	1	0	1
6	6.5	1	0	0 or 1
7	7	1	0	0
		Very strong 1	LLR0	strong 1

LLR Mapping : Improved Mapping

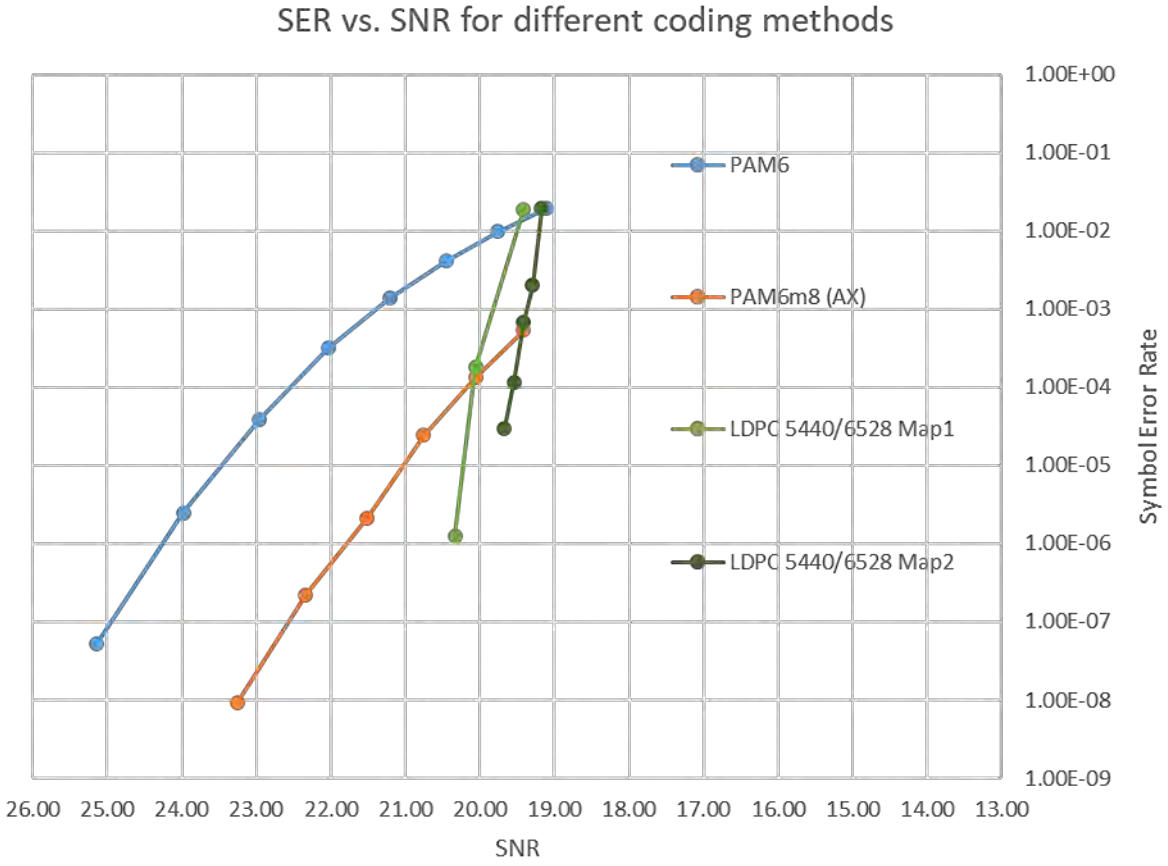
- **Divide each Ideal RX level into 8 smaller intervals**
  - Ideal level in table is -5
  - All 8 of these bins would map to -5 but with different error rates (LLRs)
  - Bins 3 and 4 have minimal error compared to an ideal voltage of -5 (higher LLRs)
  - Bins 0 and 7 also map to -5 but have significant error (lower LLRs)
- **For every bin we have 2 bits that are Inf and one with a finite LLR value.**

Map2 : PAM8 LLR Mapping Table

b2b1b0	Index	Min V	Max V	Bin #	LLR2	LLR1	LLR0
011	2	-3.75	-4	7	Inf	-1.33	(-Inf)
001	1	-4	-4.25	0	Inf	1.20	(-Inf)
001	1	-4.25	-4.5	1	Inf	3.86	(-Inf)
001	1	-4.5	-4.75	2	Inf	6.61	(-Inf)
001	1	-4.75	-5	3	Inf	9.22	(-Inf)
001	1	-5	-5.25	4	Inf	Inf	-9.72
001	1	-5.25	-5.5	5	Inf	Inf	-7.02
001	1	-5.5	-5.75	6	Inf	Inf	-4.23
001	1	-5.75	-6	7	Inf	Inf	-1.52
000	0	-6	-6.25	0	Inf	Inf	1.50

PAM6m8 compared to PAM6

- **Plot SER vs. SNR for**
  - PAM6
  - PAM6m8 AX CC8
    - 2.4 dB coding gain vs. PAM6
  - LDPC Simple LLR Map
    - 2.4 dB coding gain vs. PAM6
  - LDPC Improved LLR Map
    - 3.0 dB coding gain



- **Very steep waterfall for LDPC**

Note: Coding gains taken at SER=1e-4

Summary

- Introduction to PAMXmY modulation
- Introduction to LDPC decoding and its pros and cons relative to high speed Serdes operation
- System architecture and processing steps to enable LDPC operation
- LLR Mapping introduction
- Summary of coding gain results shows 3.0dB coding gain for PAM6m8 LDPC with reasonable LLR Mapping

Thank You