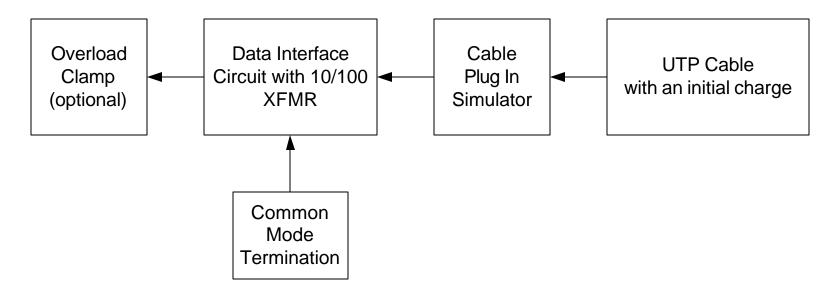
# A Simple Model For a "Cable Discharge Event"

**Rick Brooks** 

ribrooks@nortelnetworks.com

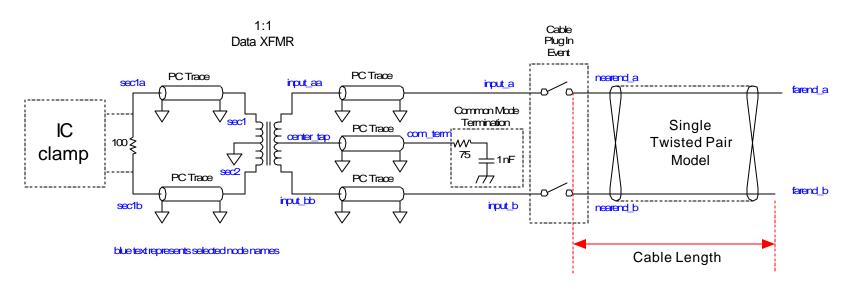
IEEE802.3 Cable Discharge Ad-hoc, March 2001

- A simple model for a cable discharge event is discussed based on a common 10/100/1000 data interface topology
- A single twisted Pair cable was constructed using a 2D+ field solver. The model was converted into a "W" element in Hspice and is referenced in the Spice deck and is shown in detail in the file "cat5\_rlc.rlc" The use of an initial condition allows the cable to be charged to some voltage prior to insertion into the 10/100/1000 data circuit.
- Plugging in the UTP cable is simulated by using a voltage controlled resistor in each line of the twisted pair cable. The two pins do not (and cannot) mate at the exact same time. I have assumed that the two pins are out of perfect alignment by 0.1 mils (fairly accurate) and that the insertion speed is 20 inches per second. These values are not critical, but simply demonstrate that it is easy to obtain a differential voltage into the data transformer. With these values, the two RJ-45 pins mate with an interval of 5 us. That 5 us time is where everything happens.



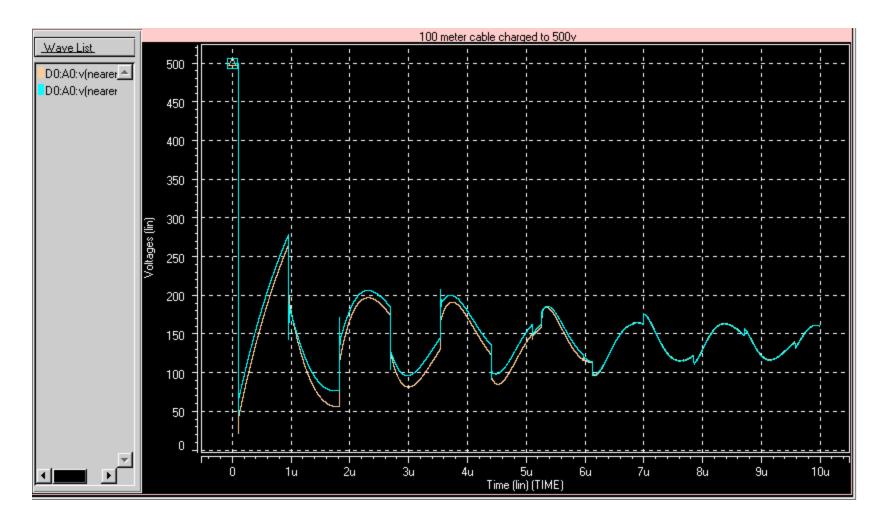
#### • Here is a simplified schematic of the cable discharge model

- The initial voltage on the UTP cable can be set
- The UTP cable length can be set, the model is in inches, so 3937 inched is 100 meters
- The HV cap in the common mode termination is modeled as a series RLC element to accounct for its finite impedance
- PC board traces are modeled as striplines using the "U" model in Hspice (here the length of the trace is in meters, oddly enough)
- The data XFMR is a 1:1 transformer with center taps, including leakage and magnetizing inductance
  - other XFMR models should be tried when available
- The IC energy/voltage clamp is an optional part
  - this will have the largest changes and effects due to how different PHY vendors handle I/O clamps for ESD, etc...
- The Hspice deck contains two VCVS elements to allow probing of the voltage across the primary and secondary of the data transformer. The generated signals are called "diff\_primary" and "diff\_secondary"
- Node names are shown in blue, as noted



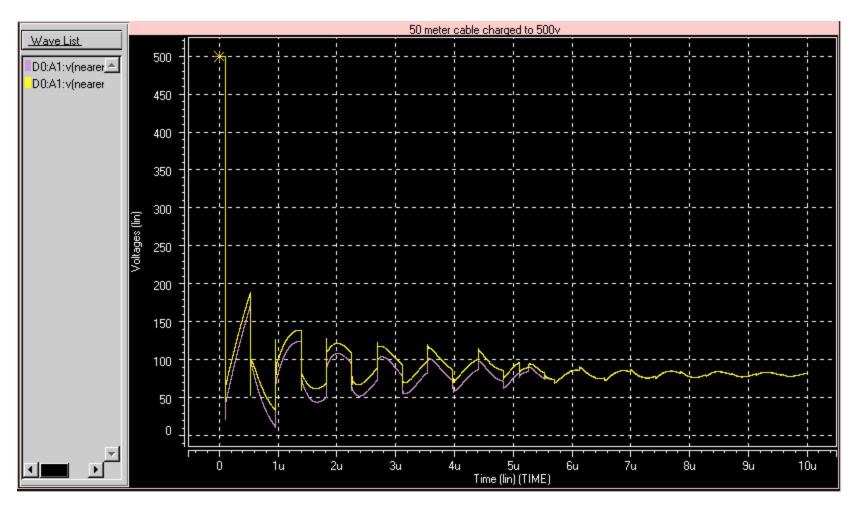
- Results, 100 meter UTP initially charged to 500VDC (no IC voltage clamp present)
  - nearend\_a: tan trace

nearend\_b: light blue trace



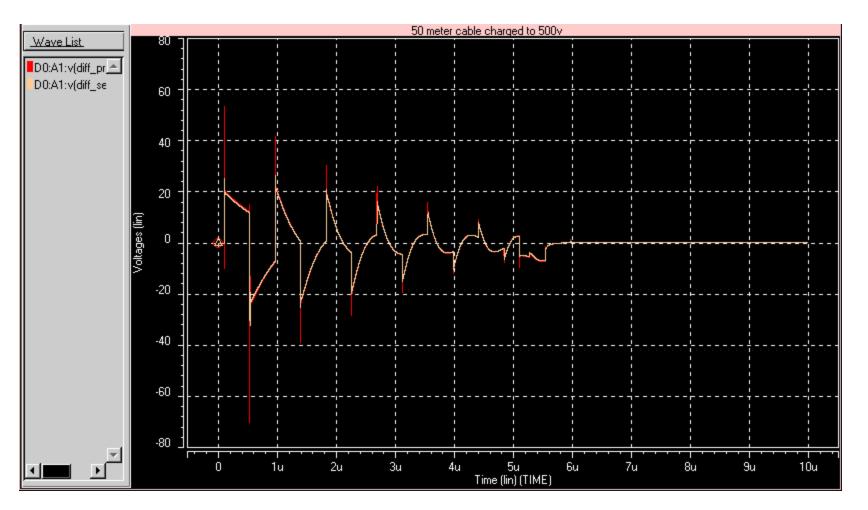
- Results, 100 meter UTP initially charged to 500VDC (no IC voltage clamp present) differential voltage across the primary and secondary of the data transformer
  - 100 meter cable charged to 500v Wave List 80 D0:A0:v(diff\_pr 📥 D0:A0:v(diff\_se 60 40 20 Voltages (lin) 0 -20 -40 -60 -80 Г 5u Time (lin) (TIME) 1u 2u Зu 7u 0 4u 6u 8u 9u 10u
- diff\_primary: green trace diff\_secondary: blue trace

- Results, 50 meter UTP initially charged to 500VDC (no IC voltage clamp present)
  - nearend\_a: violet trace nearend\_b: yellow trace

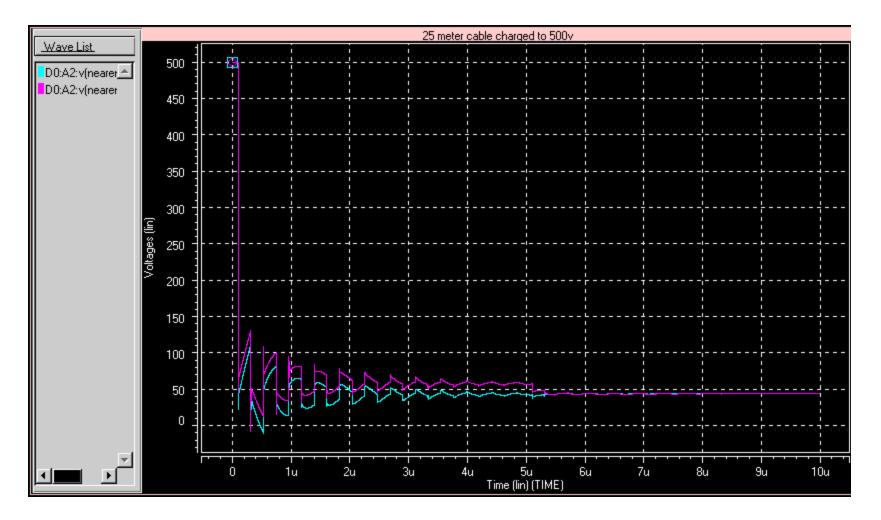


- Results, 50 meter UTP initially charged to 500VDC (no IC voltage clamp present) differential voltage across the primary and secondary of the data transformer
  - diff\_primary: red trace

diff\_secondary: tan trace



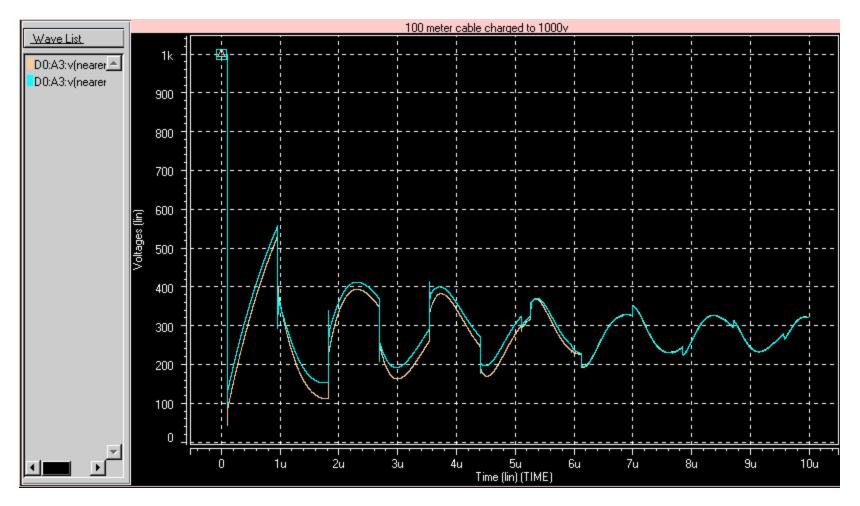
- Results, 25 meter UTP initially charged to 500VDC (no IC voltage clamp present)
  - nearend\_a: light blue trace
    nearend\_b: magenta trace



- Results, 25 meter UTP initially charged to 500VDC (no IC voltage clamp present) differential voltage across the primary and secondary of the data transformer
  - 25 meter cable charged to 500v Wave List 80 D0:A2:v(diff\_pr\_ D0:A2:v(diff\_se 60 40 20 Voltages (lin) 0 -20 -40 -60 -80 2u 5u Time (lin) (TIME) 7u 10u 0 1u Зu 4u 6u 8u 9u
- diff\_primary: yellow trace diff\_

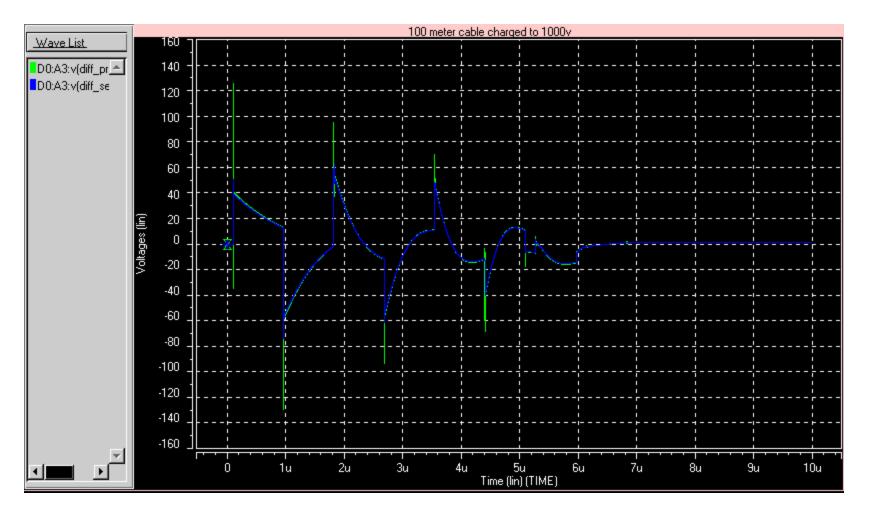
diff\_secondary: red trace

- Results, 100 meter UTP initially charged to 1000VDC (no IC voltage clamp present)
  - nearend\_a: tan trace
    nearend\_b: light blue trace

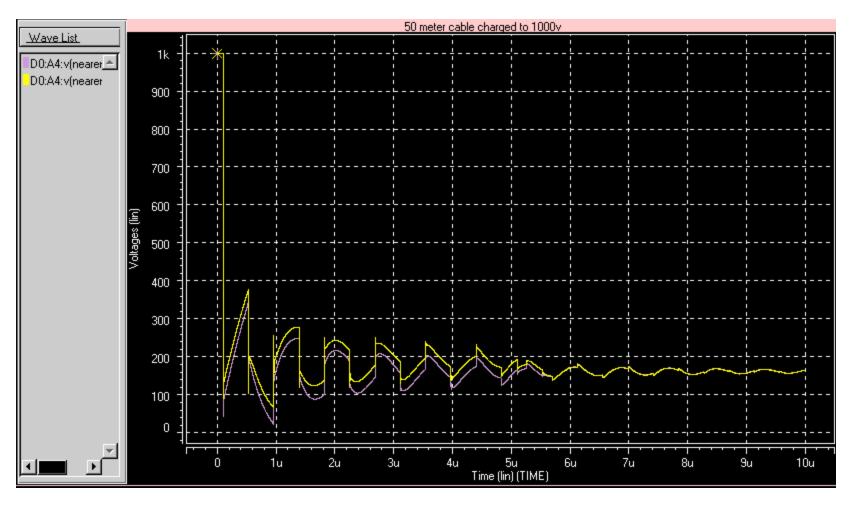


- Results, 100 meter UTP initially charged to 1000VDC (no IC voltage clamp present) differential voltage across the primary and secondary of the data transformer
  - diff\_primary: green trace

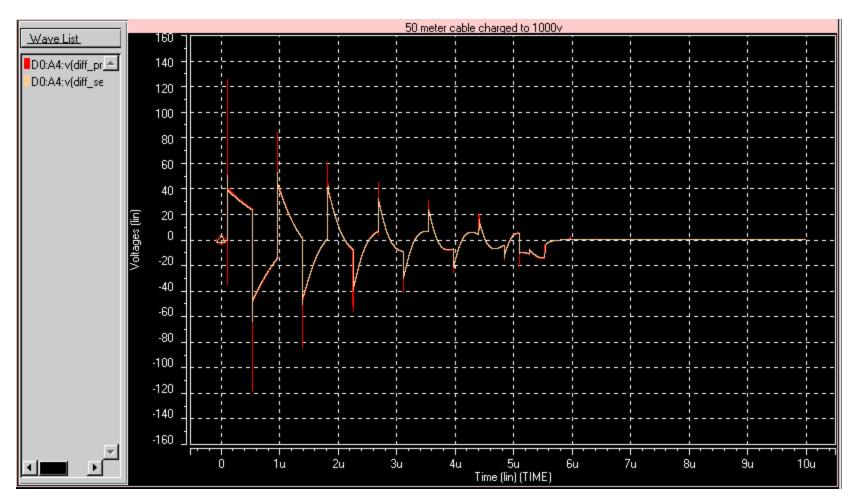
diff\_secondary: blue trace



- Results, 50 meter UTP initially charged to 1000VDC (no IC voltage clamp present)
  - nearend\_a: violet trace nearend\_b: yellow trace



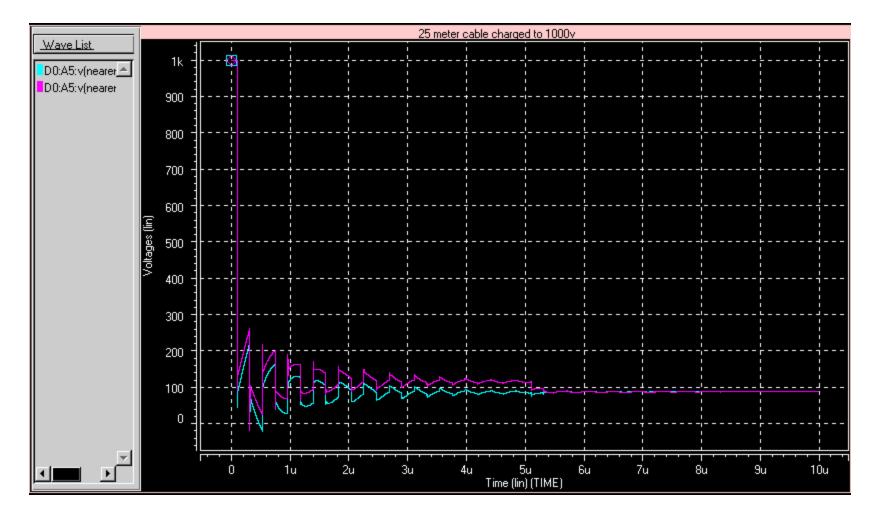
• Results, 50 meter UTP initially charged to 1000VDC (no IC voltage clamp present) differential voltage across the primary and secondary of the data transformer



diff\_primary: red trace

diff\_secondary: tan trace

- Results, 25 meter UTP initially charged to 1000VDC (no IC voltage clamp present)
  - nearend\_a: light blue trace
    nearend\_b: magenta trace



- Results, 25 meter UTP initially charged to 1000VDC (no IC voltage clamp present) differential voltage across the primary and secondary of the data transformer
  - 25 meter cable charged to 1000v Wave List 160140 D0:A5:v(diff\_pr 📥 D0:A5:∨(diff\_se 120 100 80 60 40 20 Voltages (lin) 0 -20 -40 -60 -80 -100 -120 -140 -160 5u Time (lin) (TIME) 0 1u 2u Зu 4u 6u 7u 8u 9u 10u
- diff\_primary: yellow trace diff\_se

diff\_secondary: red trace

- Conclusions
  - The available voltage on the UTP cable is the largest unknown
    - there will always be a voltage that if artificially generated on the cable, will damage the circuits and/or PHY
  - This is a simple model that uses a single UTP pair, if and when better cable models are available, more simulations should be tried including the effects of pair to pair coupling
  - Other transformer configurations and models should be tried
  - Common Mode static charge on the cable translates into a differential voltage when the cable is connected. It is this energy that causes damage in the PHY
  - The magnitude of the voltage that gets through the data transformer depends on the nature of the common mode termination circuit
  - Cable Discharge Events have a rather low driving impedance
  - The frequency range of Cable Discharge Events tend to go right through the data transformer since they are in the 10/100 band.
- Reference Files:
  - Hspice deck file
    - cable\_discharge\_100m.sp
  - Hspice W Model created in Apsim RLGC field solver
    - cat5\_rlc.rlc