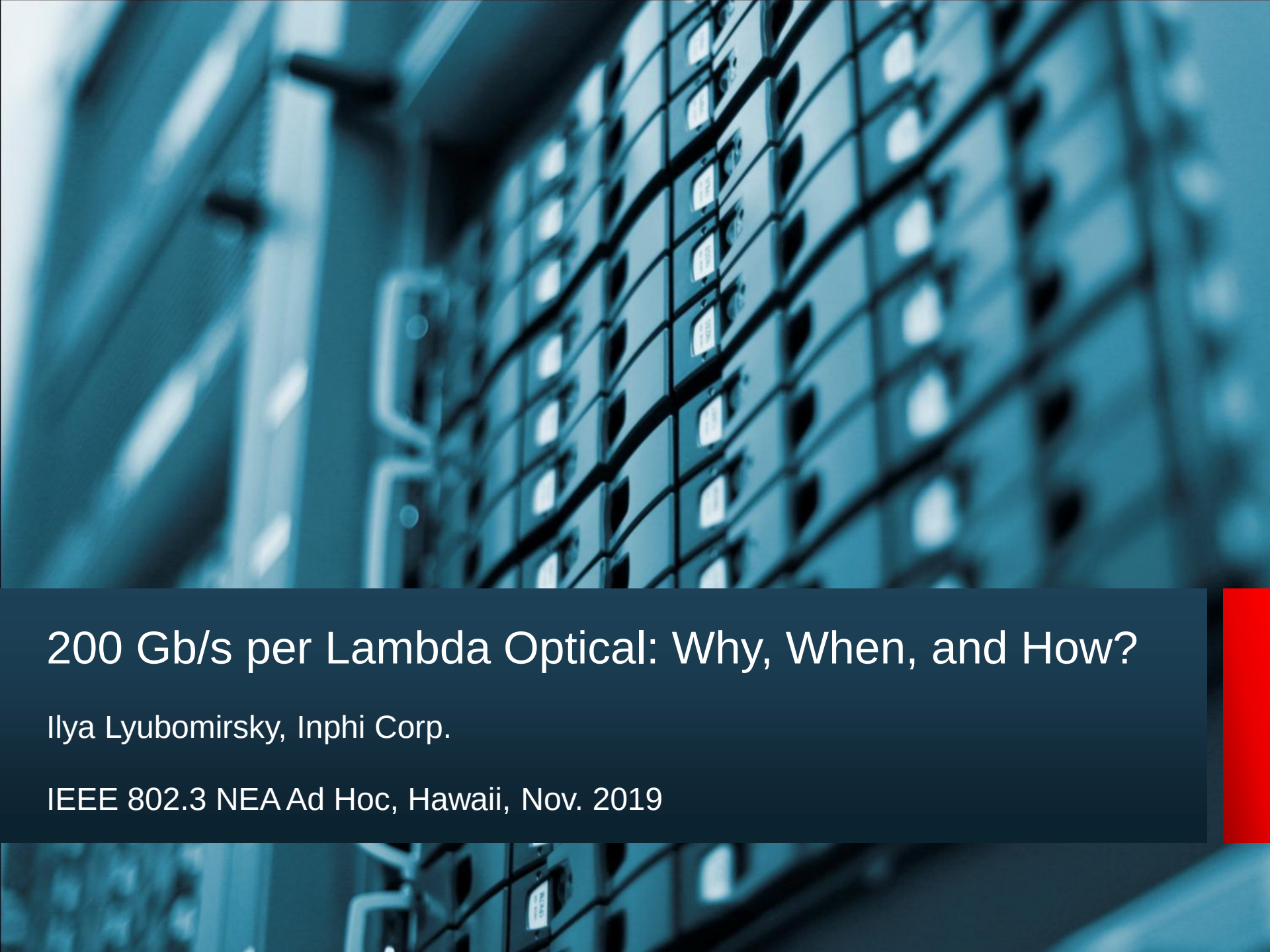


200 Gb/s per Lambda Optical: Why, When, and How?

Ilya Lyubomirsky, Inphi Corp.

IEEE 802.3 NEA Ad Hoc, Hawaii, Nov. 2019

Supporter

- Xiang Zhou, Google

Introduction

- 200 Gb/s per Lambda optical modules will be needed in 3-4 years
- Applications will include 800G FR4 and 800G DR4
- Lower optical module cost is a major driver for 4x200G vs. 8x100G
- Advancements in DAC/ADC, DSP, and optical component technology are on pace to support 200G per lane

Why?: To Meet DCN Bandwidth Growth Needs

Google server traffic growth

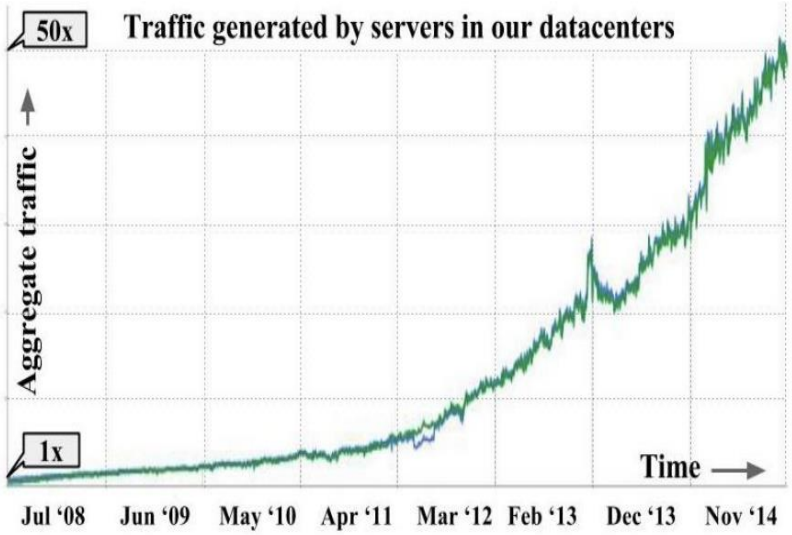
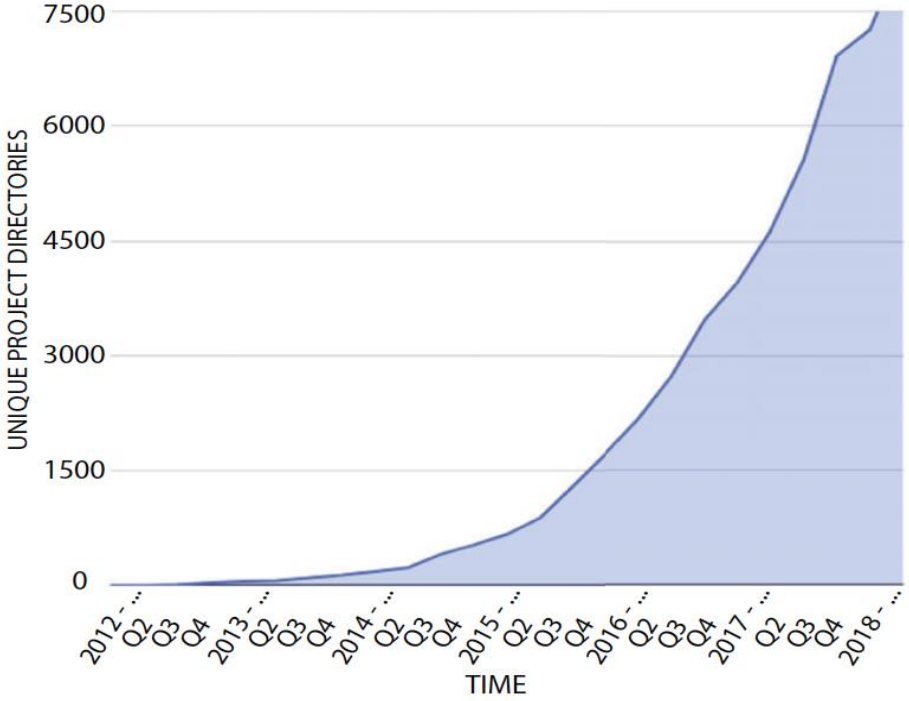


Figure 1: Aggregate server traffic in our datacenter fleet.

Ref: Arjun Singh et al, SIGCOMM '15 August 17-21, 2015, London, United Kingdom

Google ML applications



Ref: "The Datacenter as a Computer", 3nd edition, Luiz Barroso, etc.

- Aggregate Google server traffic increased 50x from 2008 to 2014
- Exponential growth of emerging ML applications further increases DCN bandwidth

Why?: To lower 800Gb/s optical module cost

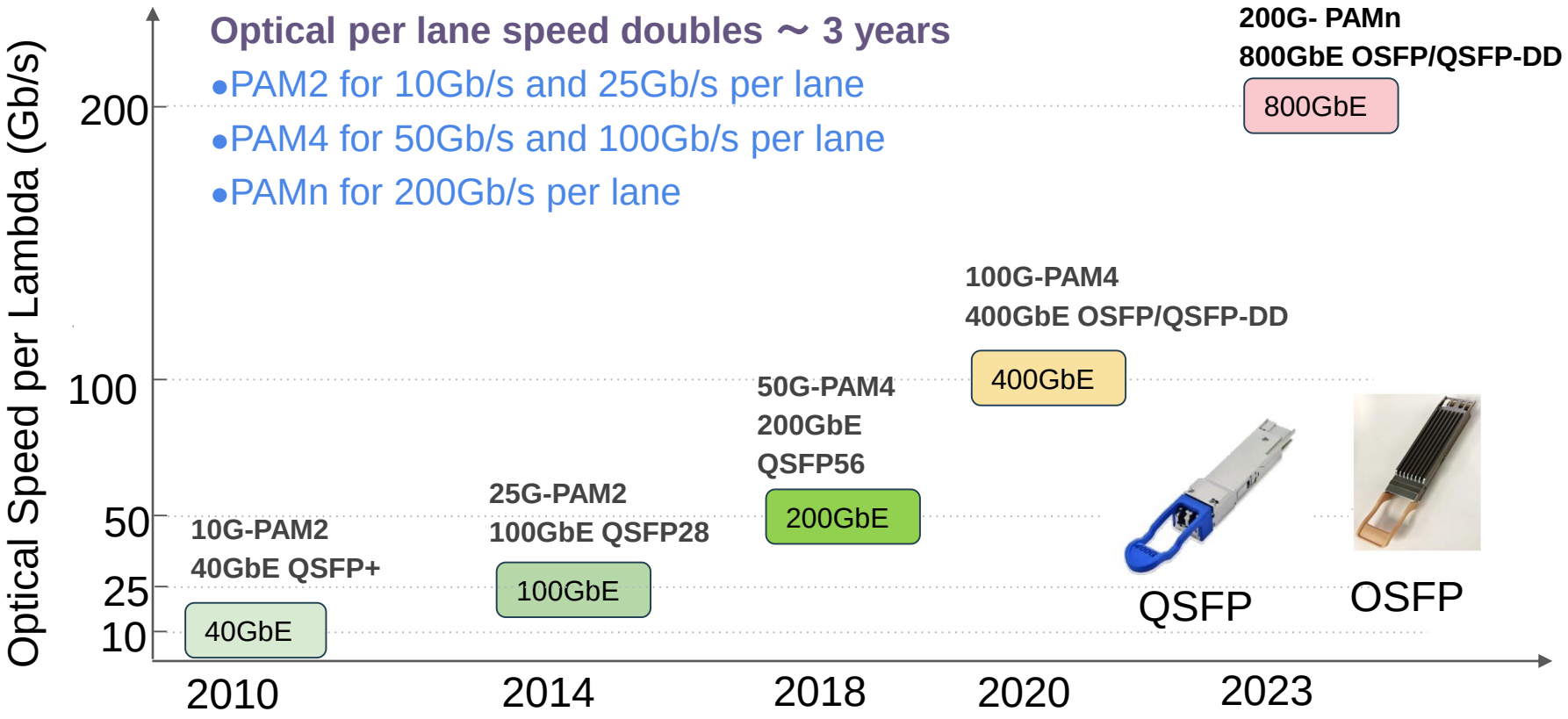
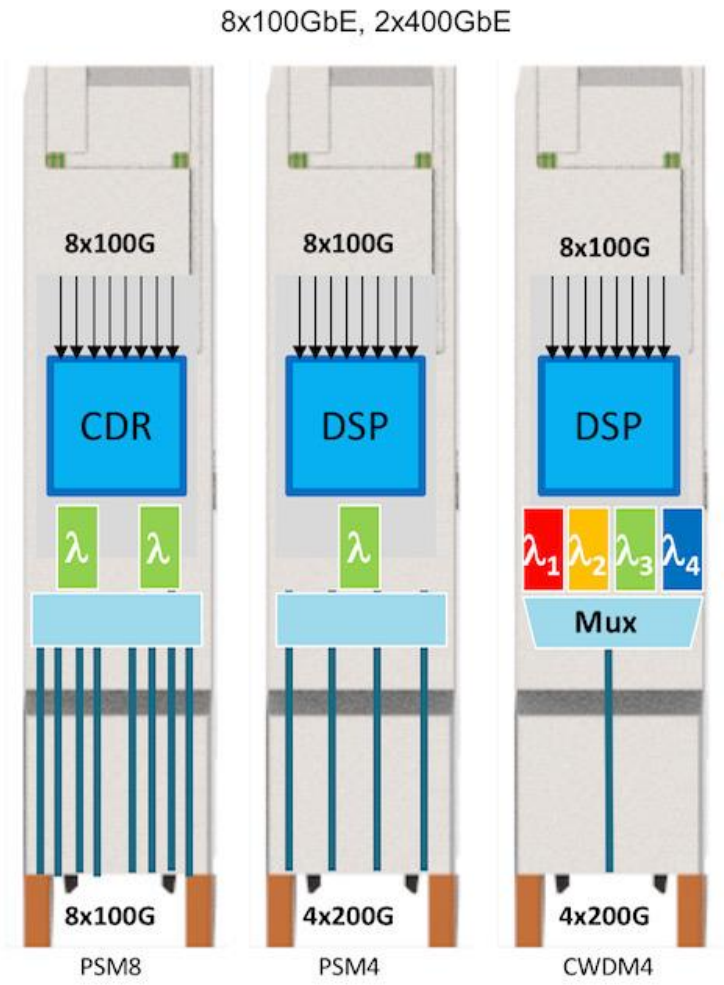


Figure courtesy of Xiang Zhou, Google

- 200Gb/s PAMn technology enables lower-cost 800Gb/s optical modules
  - Half optical components compared to 100Gb/s PAM

800G MSA

Source: http://www.gazettabyte.com/home/2019/9/18/companies-gear-up-to-make-800-gig-modules-a-reality.html



"The MSA members believe that for 25.6Tbps and 51.2Tbps switching silicon, 800-gigabit interconnects are required to deliver the required footprint and density," says Maxim Kuschnerov, a spokesperson for the 800G Pluggable MSA.

When?

LightCounting Mega Datacenter Optics report suggests that Cloud companies will need 800G modules by 2023-2024 in order to keep up with bandwidth growth inside their datacenters. We also expect that 51Tbps switching ASICs will be available by that time.

Source:https://www.lightcounting.com/News_091019.cfm

How?

- State-of-art DAC/ADC bandwidth ~ 45 GHz is sufficient for 200G based on higher order PAM
- Experimental research published in ECOC/OFC 2019 demonstrate technical feasibility for 200G per lane
- Low latency/low power higher gain FEC

ADC/DAC Technology (OECC 2019)

ADC/DAC and ASIC technology trends

Tomislav Drenski[(1)], Jens C. Rasmussen[(2)]
(1) Socionext Europe GmbH, 3 Concorde Park, Concorde Road, Maidenhead, SL6 FJ4, UK
(2) Socionext Europe GmbH, Pittlerstr. 47, 63225 Langen, Germany

Source: Optoelectronics and Communications Conference, Fukuoka, Japan, 2019

Year	2010	2012	2014	2016-17	2018-19	2020-21
			ADC/ DAC PARAMETERS		Next Generations	
POWER (MAX)	<2W/channel	<1.5W/channel	~1W/channel	<1W/channel	<<1W/channel	TBC
RESOLUTION	8-bit	8-bit	8-bit	6-8-bit	6-10 bit	6-10 bit
CONVERSION RATE	56GSa/s	55-65GSa/s	55-92GSa/s	34-128GSa/s	34 to >140GSa/s	34 to >160GSa/s
ENOB	5.5	>5.7	>6	5.5 to 6.5	5.5 to > 8.5	5.5 to >8.5
BW	>16GHz	>19GHz	>26GHz	>35GHz	>42GHz	>49GHz
			ASIC RELATED			
TECHNOLOGY*	65nm CMOS	40nm CMOS	28nm CMOS	16nm FinFET	7nm FinFET	5nm FinFET
DIGITAL GATES (DSP)	>50M	>70M	>200M	>400M	>1000M	>1500M
ADDED FEATURES	-	-	1/2 & 1/4 rate, ASV	1/2 & 1/4 rate, ASV	1/2 & 1/4 rate, ASV, others	1/2 & 1/4 rate, ASV, others
PACKAGE SIZE	35x35mm	37.5x37.5mm	37.5x37.5m	25x25mm	≤25x25mm	≤25x25mm
COHERENT APPLICATION	100Gbps	200Gbps	400Gbps	1Tbps	2Tbps	≥2Tbps

Technology*: CMOS = complementary metal-oxide-semiconductor // FinFET = Fin Field Effect Transistor

High Speed EML Technology (ECOC 2019)

High Speed InP Lasers for 400GbE

Kazuhiko Naoe

Lumentum Japan, Inc., Datacom Business Unit
4-1-55 Oyama, Chuo-ku, Sagamihara, Kanagawa, 252-5250, Japan

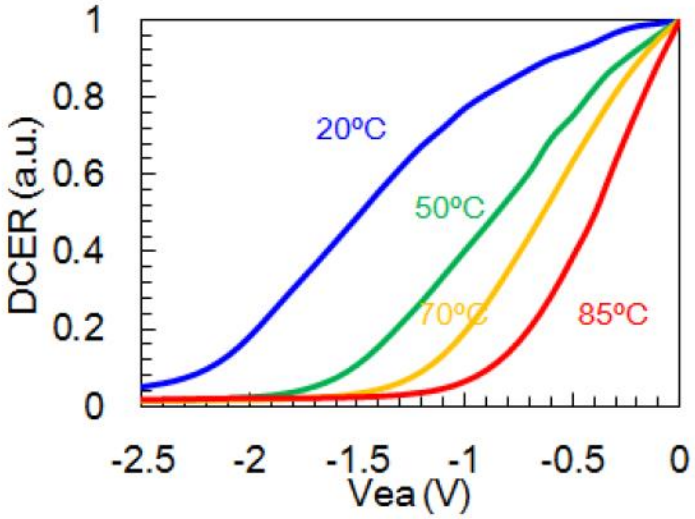


Fig. 2 DC extinction curves from 20°C to 85°C

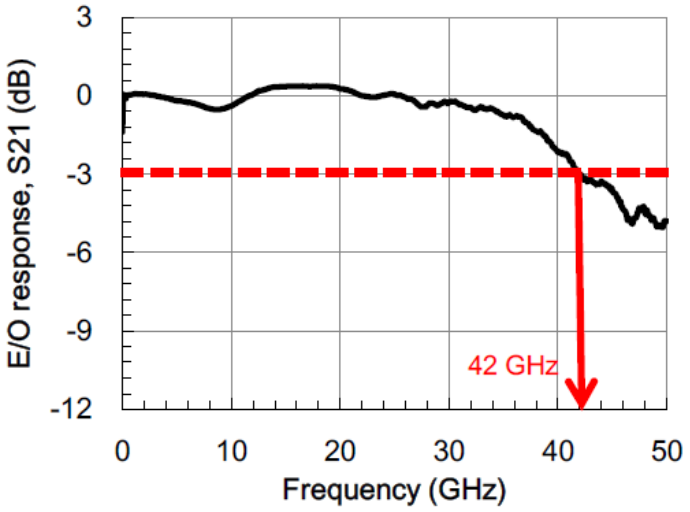


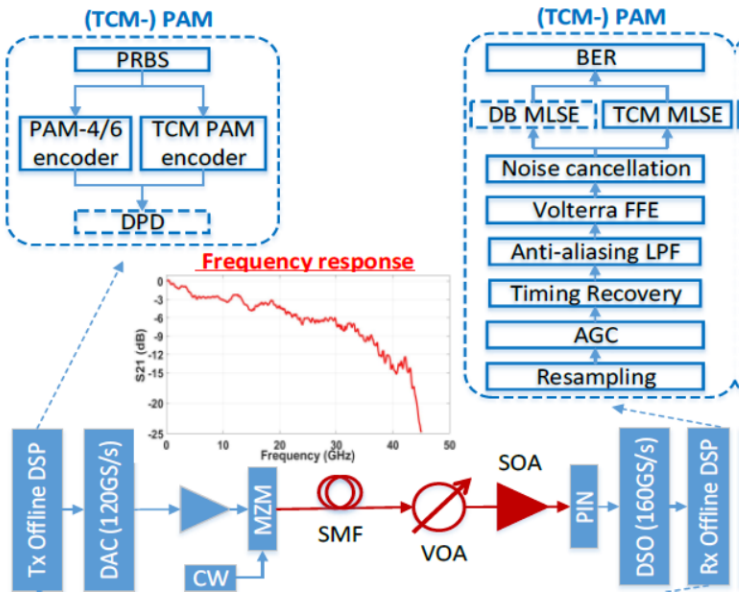
Fig. 3 E/O response at 50°C, EA bias of -1.0 V

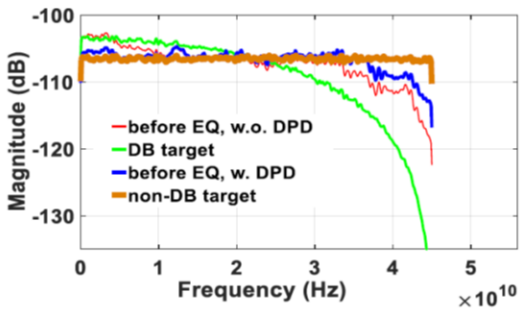
200G PAM System Demonstration (ECOC 2019)

EXPERIMENTAL COMPARISON OF MODULATION FORMATS FOR 200 G/λ IMDD DATA CENTRE NETWORKS

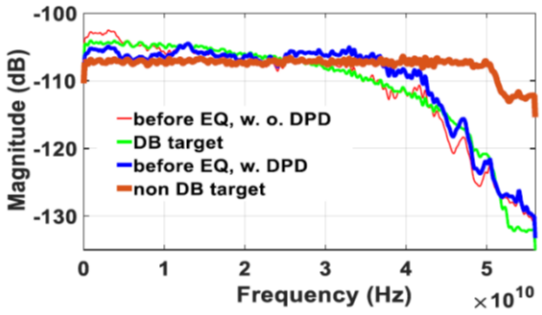
Jinlong Wei[1], Nebojsa Stojanovic[1], Liang Zhang[1], Stefano Calabrò[1], Talha Rahman[1], Changsong Xie[1], and Gabriel Charlet[2]*

[1]Huawei Technologies, European Research Center, Riesstraße 25, 80992 Munich, Germany
[2]Huawei Technologies French Research Center, 20 quai du point du jour, 92100, Boulogne-Billancourt, France





(b) PAM-6



(a) PAM-4

200G PAM System Demonstration (continued)

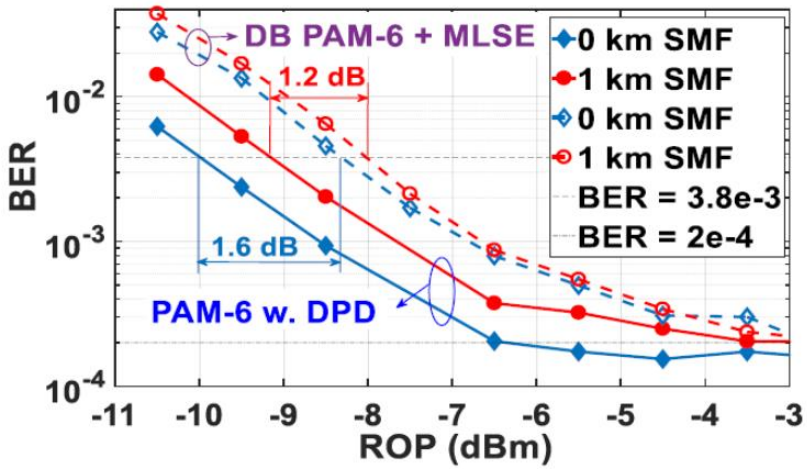
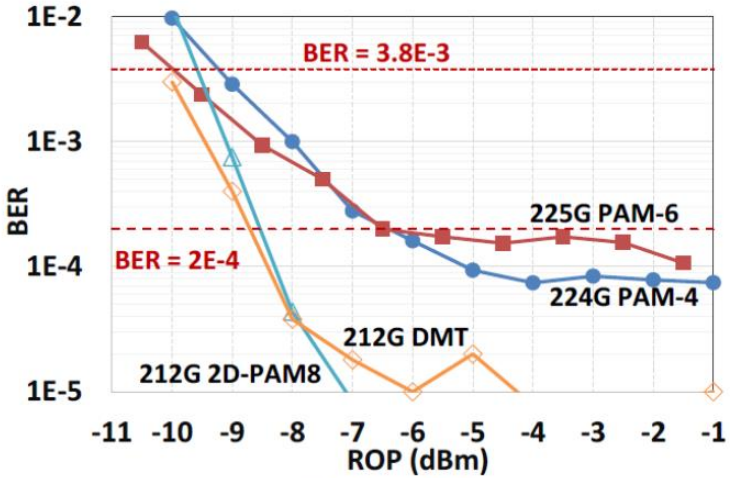


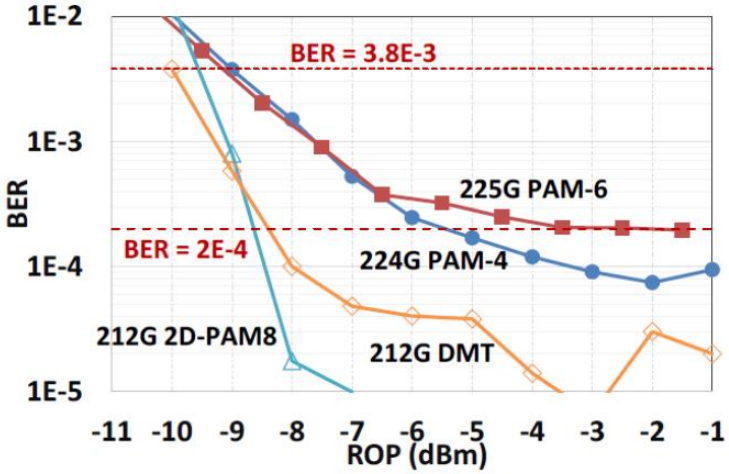
Fig. 3 BER versus receiver optical power (ROP) for 90-Gbaud PAM-6 system.

Table 1 Summary of performance and FEC/DSP requirement

Format	224G DB PAM-4	225G PAM-6	212G 2D-PAM8	212G DMT
1 km ROP sensitivity	-9 dBm	-9 dBm	-8.6 dBm	-8.4 dBm
FEC OH	12%	12%	5.9%	5.9%
DSP	DPD DB FFE, DB-MLSE	DPD, FFE	DPD, FFE, TCM	IFFT/FFT FFE, TCM



(a) Optical BtB

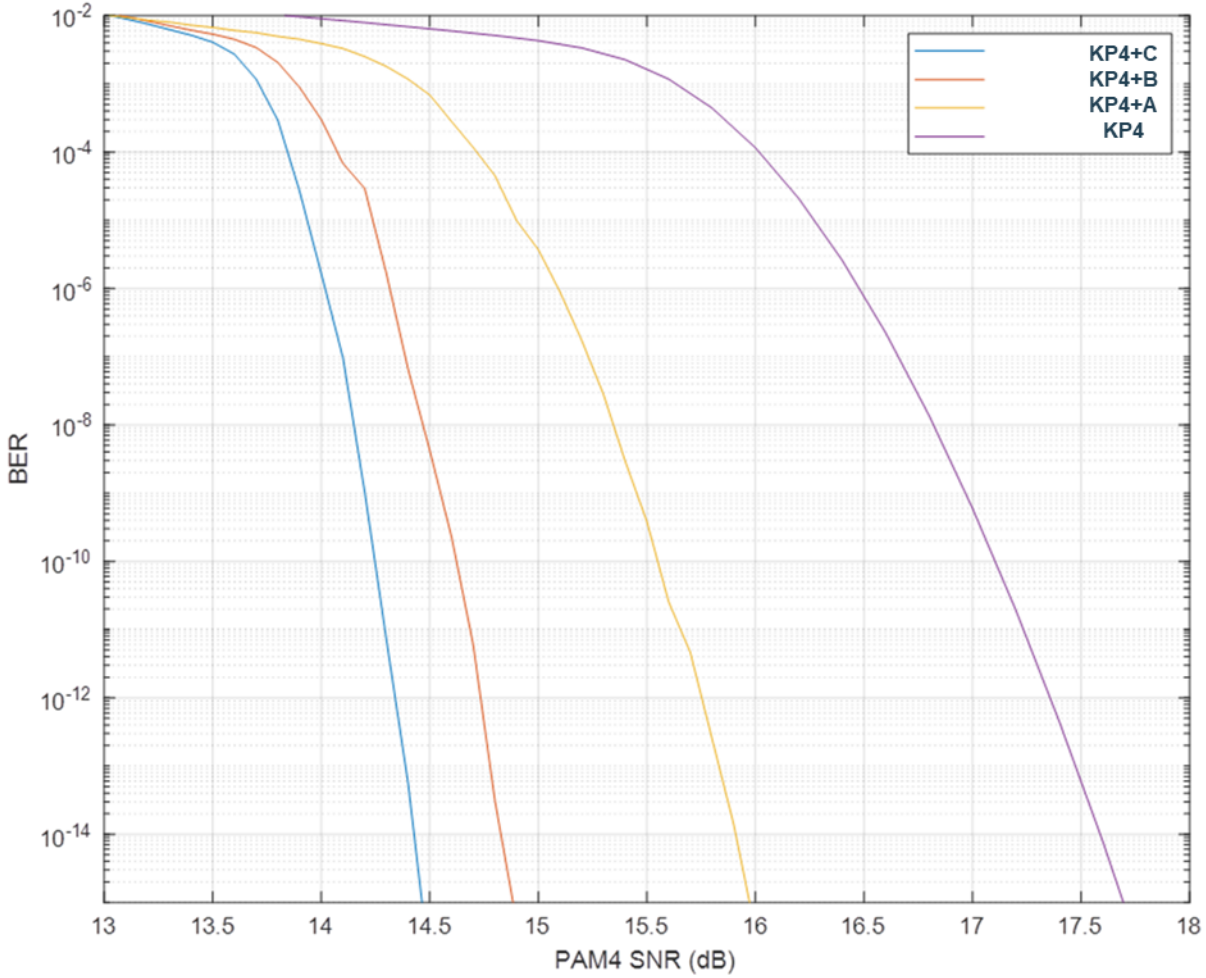


(b) After 1 km SMF

Fig. 4 BER versus ROP of each scheme for the (a) optical BtB, and (b) 1 km SMF cases.

Low Latency/Low Power Higher Gain FEC

Source: B. Smith, V. Shvydun, J. Riani, and I. Lyubomirsky, “Next Generation PON and Data Center Interconnect: Exploring Synergies on FEC,” IEEE Summer Topical, July, 2019



Conclusions

- Market demand in US and Asia exists for 800G optical modules in 2023-24, as evidenced by exponential growth in bandwidth demands for server and ML applications
- 200G per lane optics will be the lowest cost solution for 800G
- Advancements in ~ 100 Gs/s ADC/DAC and optical component technology will enable 200G based on higher order PAM